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# L1Topo: The Level-1 Topological Processor for ATLAS Phase-I upgrade and its firmware evolution for use within the Phase-II Global Trigger

*Friday 19 July 2024 11:15 (15 minutes)*

The ATLAS Trigger, upgraded for the increased instantaneous luminosity of the LHC in Run 3, includes a topological trigger system (L1Topo) that performs complex multi-object trigger calculations within a very small processing time of 75 ns. L1Topo is based on 6 Xilinx Ultrascale+ 9P FPGAs for massively parallel and fully synchronous computation using 2.5M LUTs per FPGA. Its firmware is composed of a large number of sort/select, decision, and multiplicity algorithms, automatically assembled and configured based on the trigger menu. An overview of the L1Topo hardware, firmware, commissioning challenges and performance results is presented.

For the HL-LHC, L1Topo will be replaced by a Global Trigger, a time-multiplexed system, concentrating the data of a full event into a single FPGA. An overview of the new topological firmware, redesigned from the Run 3 building blocks to match the larger available processing time (1.2 us) and a much tighter resource budget (100k LUTs), is presented.

## Alternate track

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Yes

**Authors:**   MEUSER, Emanuel (Johannes Gutenberg Universitaet Mainz (DE));  ZHU, Junjie (University of Michigan (US))

**Presenter:**   MEUSER, Emanuel (Johannes Gutenberg Universitaet Mainz (DE))

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