

The CMS Muon System Upgrade for High Luminosity LHC ICHEP 2024 : 42nd International Conference on High Energy Physics 17-24 July 2024, Prague

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CMS Muon System

- Four detectors based on different gaseous detector technologies to achieve excellent Muon identification, measurement & triggering
- Drift Tubes: DT
- Resistive plate chamber: RPC
- Cathode Strip Chamber: CSC
- Gas Electron Multiplier: GEM

Upgrade Overview

- Barrel: The upgrade is mainly on electronics
- 4 DT stations
- 4 RPC stations
- End-cap: The upgrade is on electronics and on the installation of new detectors
 - 4 CSC stations (Electronics)
- 4 RPC stations (Electronics + New Detectors)
- 1 GEM station GE1/1 (New Installation 2019-2020)

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- New detectors: - MEO & GE2/1 (GEMs) - RE3/1 & RE4/1 (iRPC)



High Luminosity LHC (HL-LHC) schedule

- HL-LHC program will start by 2029
- Muon system upgrades to be done in technical stops or Long Shutdown (LS) 3



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Challenging conditions expected at HL-LHC

	LHC	HL-I
Instantaneous lumi (cm ⁻² s ⁻¹)	2x10 ³⁴	(5-7.5)
ntegrated Lumi (fb ⁻¹)	300	3000
Pile Up	50	140 (
	CMS Phase	1 P
L1 trigger (kHz)	100	
L1 latency (µs)	3.6	

Goal: to maintain the excellent performance of the CMS Muon System within large geometrical acceptance in challenging and more harsh data-taking conditions

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CMS Drift Tubes (DT) Upgrade

- Located in the barrel region of CMS, DTs are responsible for identifying, measuring & triggering muons
- DT upgrade focused on the Front-end (FE) & the Back-end (BE) electronics







Front-end : Minicrate structures attached to the DT chambers embed the new on detector electronics (**OBDT**)

Back-end : Two types of backend for "Timing" and Detector Control" (Serenity boards) and for "Trigger and Readout" (Barrel Muon Trigger Layer 1 (BMT L1 boards))

Monitor and Safety (MONSA) system for monitoring the OBDT status, connected to CMS detector safety system (DSS)

η 1.2	θ° 33.5°
1.3	30.5°
1.4	27.7°
1.5	25.2°
1.6	22.8°
1.7	20.7°
1.8	18.8°
1.9	17.0°
2.0	15.4°
2.1 2.2 2.3 2.4 2.5	14.0° 12.6° 11.5° 10.4° 9.4°

4.0 2.1 5.0 0.77

DT Upgrade : S12 Slice Test (Sector 12 of Wheel +2)

• **Goal :** to test the upgrade electronics with realistic conditions in CMS environment

Sector 12 Slice Test

- 13 early prototypes of OBDT (v1) boards installed during LS2 (same OBDT boards for Theta & Phi superlayers)
- The legacy electronics chain & and the upgrade chain register the same event splitted
- Extensive data-taking during cosmic and collision runs to test the soundness of DT electronics, the upgrade strategy & data fully integrated in CMS

OBDT Prototype v1.0

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As Phase 2 chain has more bandwidth capability, readout window in early data was kept ~5 times wider than in the legacy

Difference between trigger primitive's time and the offline reconstructed segment time

DT Upgrade : S1 Slice Test (Sector 1 of Wheel +2)

• Goal: to test the latest version of upgrade electronics with realistic conditions in CMS environment

Sector 1 Slice Test

- 9 later stage OBDT PHI & 2 OBDT THETA boards with final technology installed during Year End Technical Shutdown (YETS) 2022-23
- To test the final electronics, integration with clock, timing, Monsa safety system

DT Upgrade schedule is on track and the new electronics will be installed in **LS3**

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- Time measurement distribution (top) and occupancy distribution (bottom) for second station (MB2) from the new OBDT electronics at S1 Slice Test
- Beam structure is visible in the time distribution of the hits (5 bunch trains of 12 colliding bunches each plus two single colliding bunches), while the Occupancy distribution shows that the system does work as expected, apart from some known issues which will be investigated in next YETS
- No trigger was applied, all hits were streamed & collected asynchronously through the internal memories of the BMTL1 board

Cathode Strip Chamber (CSC) Upgrade

• On-detector Front-End (FE) electronics

- Can't cope with longer trigger latency and increased data transfer rates in phase-2 & needed upgrade for :
- CFEBs (Cathode Front End Board) for stations 2-4 of Ring 1 (ME234/1)
- All ALCT (Anode Local Charged Track board) mezzanines except for ME4/2
- ALCT mezzanines/ DCFEB in ME11

• Backend (BE) electronics upgrade

- Due to the increase of particle rates & trigger latency at HL-LHC, the CSC backend electronics will face:
 - Memory overflows & readout inefficiencies
 - Expected event losses
- Upgrade of CSC FED (Front end driver) is needed for phase-2

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Off-detector FE electronics

- Increased data-transfer rates of phase-2 will require higher band width for the chambers closer to the beam pipe (e.g. chambers in all the stations 1-4 of Ring 1 (ME1234/1))
- The (O)DMBs (optical data motherboards) are VME boards that read out the CSC muon chambers and will be upgraded for phase-2 for chambers in ME1234/1

CSC Upgrade Overview

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- Due to LS3 constraints, major part of the CSC upgrades were done in LS2 e.g. on-detector FE electronics upgrade, Trigger motherboard upgrade (TMB) and improved High Voltage (HV) & Low Voltage (LV) to handle phase-2 occupancy
- In LS3, CSC upgrade will focus on off-detector upgrade, replacing ODMB with new version boards (ODMB7 for ME1/1 & ODMB5 for ME2,3,4/1) and BE upgraded FED (Advanced Telecommunications Computing Architecture (ATCA) FED)

CSC Upgrade Status

• **ODMB5/7**

- 72 ODMB7 boards for ME1/1 & 108 ODMB5 boards for ME234/1
- Pre-production boards have been designed, produced, and tested

- After going through various irradiation tests of different components, ODMB7/5 design is finalised and production order sent out
- Testing procedure is set-up at UCSB (University of California), once the production will be ready
- Boards will arrive at CERN in early spring 2025, followed by 2nd round of testing. Also planning for Run 3 demonstrator/ commissioning

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Backend DAQ ATCA FED

• Main functions are DAQ readout / error reporting / trigger throttling

CSC FED system Overview

- 2 ATCA crates
 - 5 backend cards per crate for FED
 - DTH400 + 3 DAQ800 per crate
 - Dedicated X2O for TTC (timing, trigger & control) per FED
- Recent version X20 v3 tested & validated in May 2024
- Tentative plan is to be ready for assembly in December 2024 and to complete assembly & testing of all boards in mid April 2025 at CERN & external sites

Resistive Plate Chambers (RPC) Upgrade

- New Link System:
 - Improve Trigger hit time resolution from 25 ns to 1.56 ns
 - Data transmission speed up to

10.24 Gbps

efficiency > 95%

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• iRPC are able to sustain high expected rates of up to **2 kHz/cm2**, with hit

New RPC Link System Upgrade Overview

- The present RPC Link system will be replaced with the new Link System in LS3
- The main goal is to replace present electronics with brand-new highperformance ones

Key Features of new Link System

- **14 Layer** PCB , 40 × 28 cm2
- FPGAs are KINTEX-7, XC7K160T Industrial Version
- Muon hit time, TDC timing Resolution : **1.56 ns**
- Master Link board output data rate : **10.24 Gbps**
- Control Board communication with RPC Backend electronics: **4.8 Gbps**
- The irradiation tests of the different components and FPGAs of new link system are completed and the electronics meet the HL-LHC radiation condition with high safety factors
- A demonstrator installed at CMS experiment in Feb. 2024 to monitor the behaviour of the system in realistic conditions
 - System has been working continuously and reliably for five months without any change on performance and stability
- Pilot production is foreseen in **September 2024** & delivery to CERN by the **end of 2024**

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New Link System (left) and present Link System (right) at CMS experimental cavern (UXC)

iRPC Upgrade Overview

Production & Quality Control

- First step of Quality Control performed in the original sites of components assembly
- Second step of quality control tests is performed in detector assembly sites (CERN & Ghent University)
- Quality control results for a RE4/1 chamber type with portable FEB v2.3 using cosmic data

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- 4 demonstrator chambers were installed in CMS in the end of the Long Shutdown 2 (2021)
- <1 Hz/cm2 of noise and stable operation with CMS grounding, water cooling and magnetic field of 3.8 T
- First 2 chambers of final production, installed and commissioned last December 2023 in CMS, chamber construction expected to be completed by the end of 2024, installation planned during next YETS access time

More details are in talk by S. Buontempo

Gas Electron Multiplier (GEM) Upgrade

- 3 projects based on Gas Electron Multiplier (GEM) Technology
 - GE1/1, GE2/1: complementing CSC in forward region (Station 1 & 2 for Ring 1)
 - **MEO**: Extending muon system acceptance in very forward region
- Both GE1/1 & GE2/1 based on same mechanical design principle
- 2 triple GEM detectors per Super Chamber (SC)
- **GE1/1**:72 SC (36 per endcap)
 - 10° in ϕ from 1.6< $|\eta| < 2.1$
- **GE2/1:** 36 SC (18 per endcap)
 - 20° in ϕ from 1.6< $|\eta| < 2.4$

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• **MEO**: Extending CMS Muon System acceptance up to $|\eta| < 2.8$

18 MEO stack per endcap, each made of six layers of triple-GEM detector for efficient tagging of muon tracks

GE1/1 & GE2/1 Upgrade Overview

- The main motivation is to improve trigger efficiency and avoid large increases in trigger rate expected at HL-LHC
- GE1/1 chambers installed during LS2 and running since the beginning of Run 3
 - Detailed performance with Run 3 data shown in the talk by G. Pugliese

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- Up to now, 3 GE2/1 chambers installed and integrated in CMS Data Acquisition system (DAQ) / Detector Control System (DCS)
 - The goal is to gain operational experience and for other conformity checks (occupancy, noise, Dead channel, Cross talk)
 - Efficiency shows the expected performance
- GE2/1 chambers are in production phase (detailed validation & performance results of production chambers shown in Poster by T. Elkafrawy)

MEO Upgrade Overview

Horizontal GEM foil Radial GEM foil segmentation w.r. to beam line segmentation w.r. to beam line **CMS** *Phase-2 Simulation Preliminary* CMS Phase-2 Simulation Preliminary (cm) y (cm) Rate (MHz) 140 \geq 130 130 120 article 120 110F 110F 100 100 90 | 90 F 80 80 F 70 | 70 -20 10 20 -10 -20 -10 20 10 0 x (cm) x (cm)

- Highly uneven background as a function of distance from beam line
- Highly uneven voltage drop

- Equalises the background rate across all segments
- Uniform gain drop

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- **Requirements** :

- 97% module efficiency
- < 500 μ rad resolution
- 8-10 ns time resolution
- ≤ 15% gain uniformity
- Work in high-rate environment: 150 kHz/cm2
- Survive harsh radiation environment: 7.9 C/cm2
- Discharge rate that does not impede performance or operation
- MEO design validated in test beams, also with high background (more details in T. Sheokand talk)
- Preproduction started, installation schedules in early LS3

MEO stack prototype in GEM Lab at CERN B904. Prototypes for all front-end and back-end electronics tested successfully

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90

.85

1.80

1.75

1.70

1.65

1.60

1.55

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Summary

- In preparation to meet the challenges expected during HL-LHC & to keep the ongoing in parallel to Run 3

expected performance of CMS Muon system, several upgrades are planned and

• Present detectors (DT, CSC & RPC) which will continue operating until the end of LHC operations (stable performance measured in extensive longevity studies), are going for the electronics upgrade to sustain the challenging phase-2 conditions

• Moreover, active progress is being made in the development of new muon stations (GE2/1, MEO, RE3/1, RE4/1) to expand η coverage. This initiative not only improves

redundancy but also fine-tunes pT measurement accuracy at high trigger rates

