How to upgrade a pixel detector

lessons from Phase-1 being applied to Phase-2 CMS Pixel Upgrade

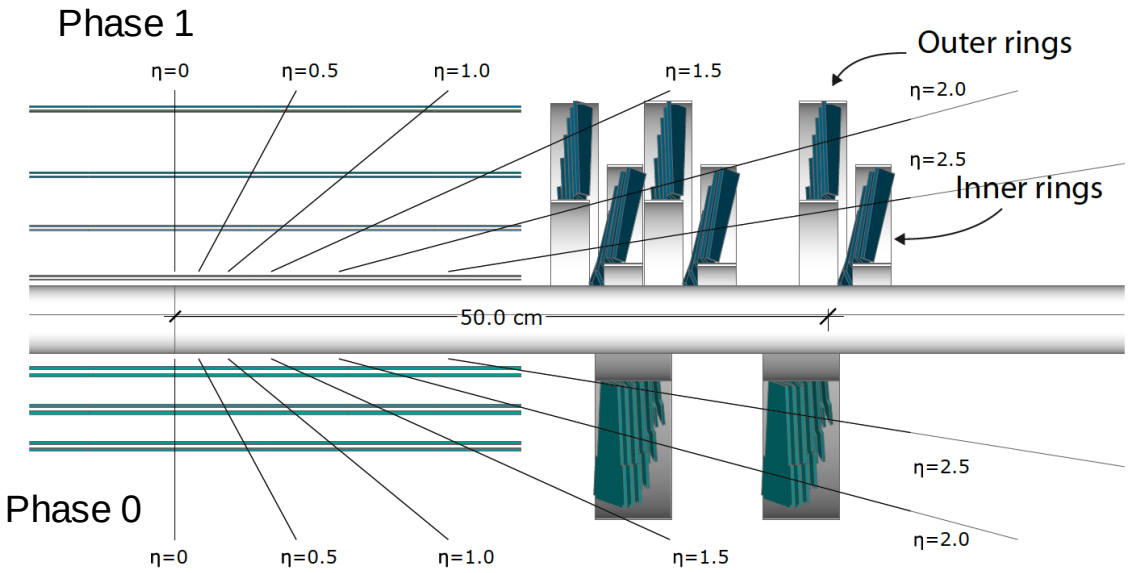
Rachel Bartek
on behalf of the CMS Collaboration

THE CATHOLIC UNIVERSITY OF AMERICA

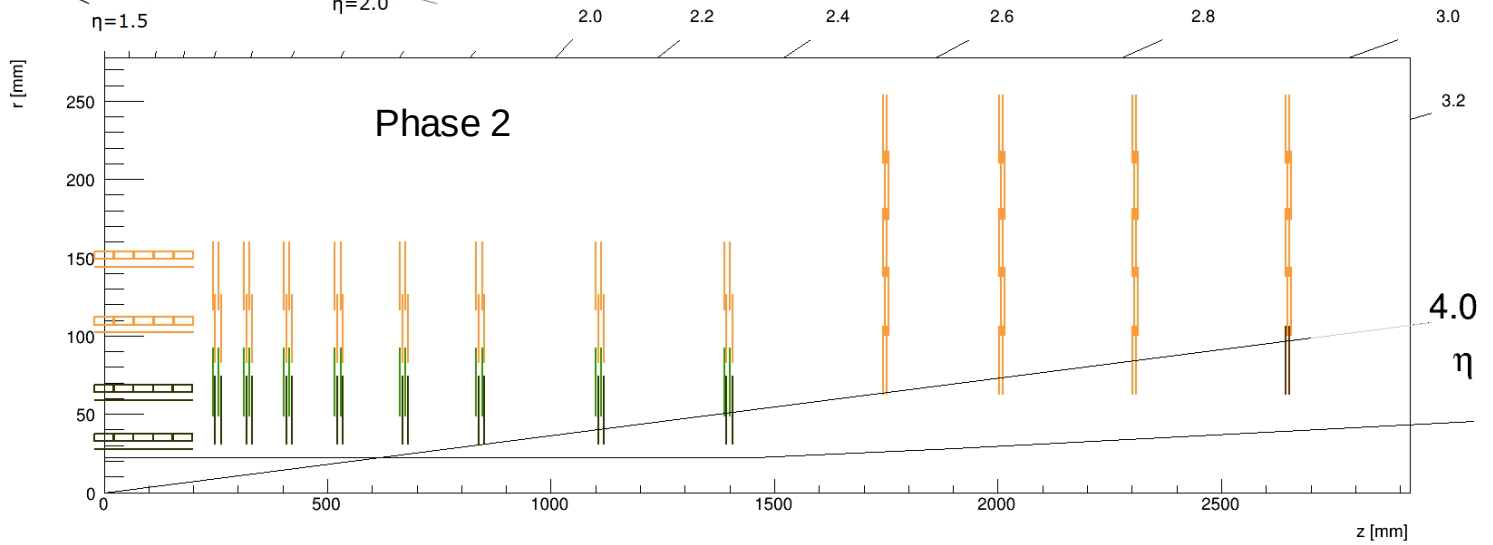
So many lessons

- Stability is hard to come by
  - *Layer 1 soft error recovery storms*
- DC-DC converter saga
  - *Put reset on everything*
  - *Radiation test everything*
  - *A new operation mode without testing is ill advised*
- Timing is everything
  - *Two chips one offset*
- Don’t let sparks fly
  - *Spark protection is important*

CMS Pixel upgraded in two phases

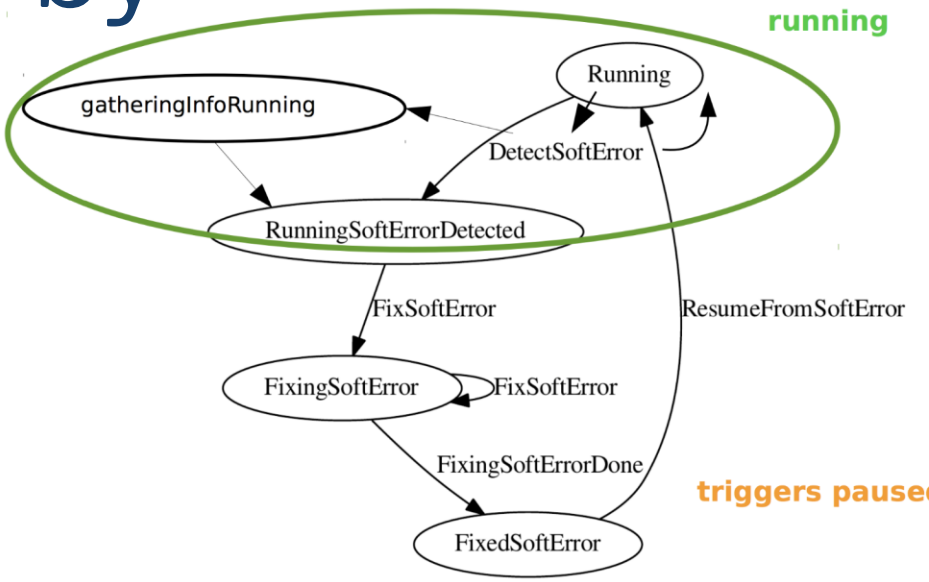


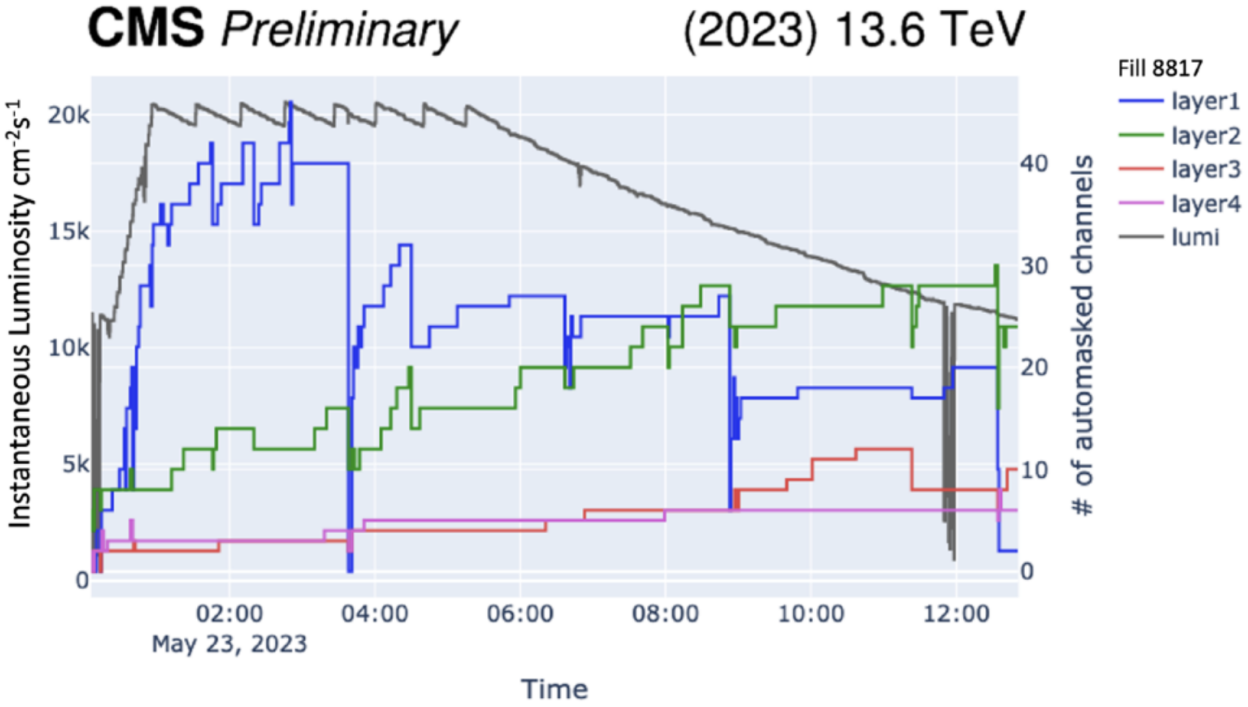
	Number of pixels	Number of modules
Phase 0	66 million	1440
Phase 1	124 million	1856
Phase 2	2 Billion	3892

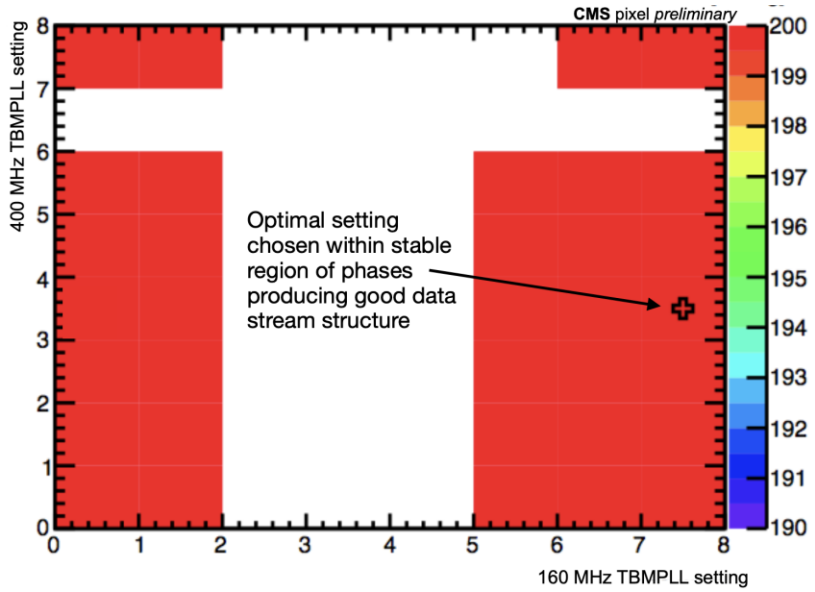


Stability is hard to come by

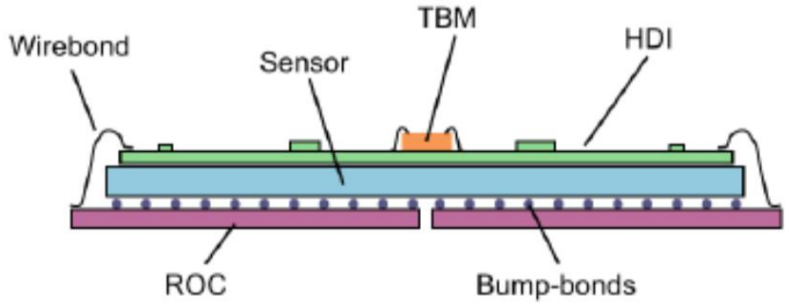
- Soft Error Recovery refreshes configuration
  - *Recoverys port cards and front end chips*
- Experiences Soft Error Recovery “storms” PU > 60
- Adjust 400 MHz and 160 MHz TBM phases





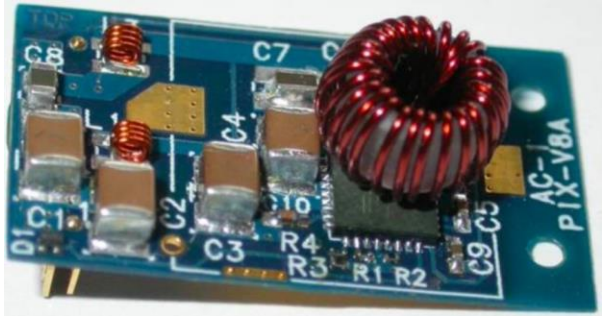


DC-DC converter saga (1 of 4)



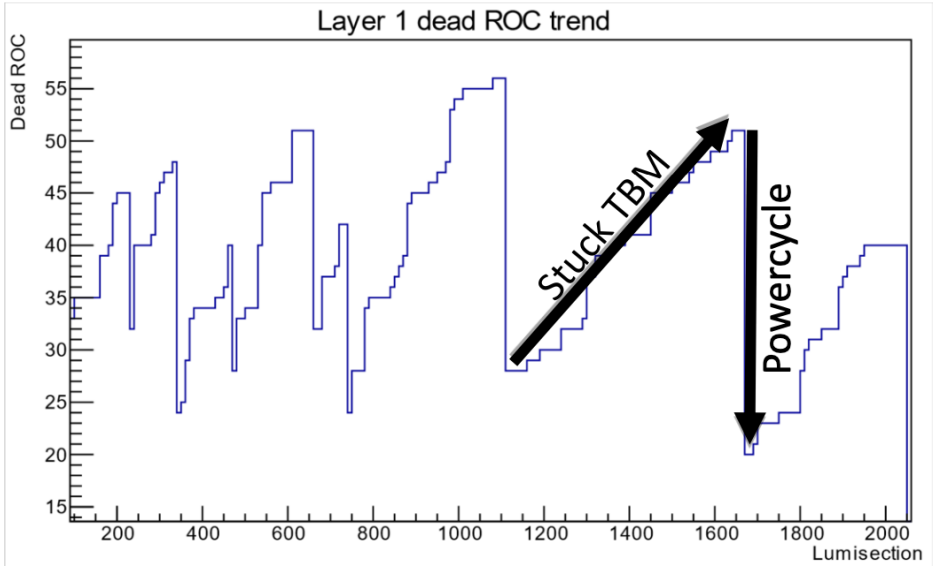
- Put a reset on everything
- Test everything in radiation
- A logic mistake allows for a possible locking of the phase 1 TBM circuit
  - *No way to reset except to power cycle*
- Power cycles clear the TBM lock
  - *Power cycling pixel is a very heavy procedure*
  - *Luckily we have a mechanism to power off/on smaller granularity DC-DC converters . . .*

DC-DC converter saga (2 of 4)



- Phase-1 has many more modules than Phase-0, therefore needs more power, but the number of cables was fixes
- Use DC-DC converters to step from 10V to 3V
- 1184 converters based on rad-hard FEAST2 ASIC from CERN
- Used enable/disable in FEAST2 chip to power cycle stuck TBM modules
- After about 30 fb^{-1} DC-DC converters start to break at power cycle
  - *At end of 2017 5% converters broken*
  - *Over 40 fb^{-1} for this year as of last week*
  - *DC-DC converters used in phase 2*
    - Insert panic here

Run 303838 Sep. 2017



DC-DC converter saga (3 of 4)

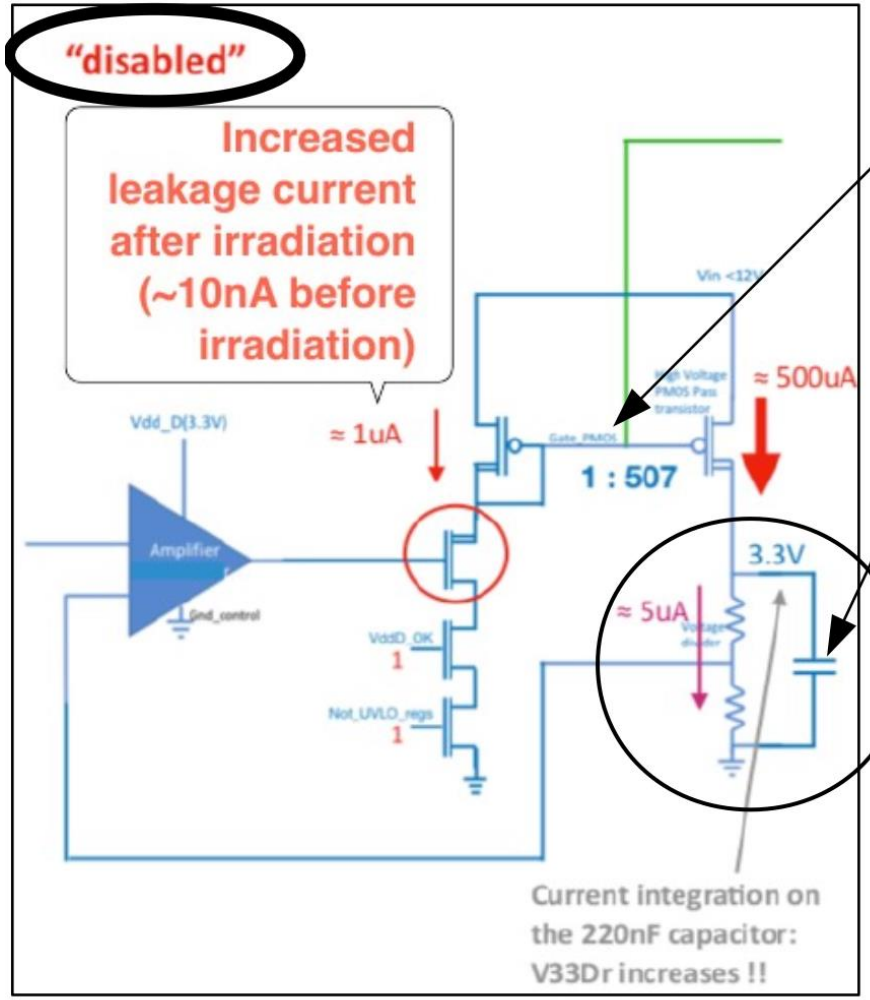


figure by Federico Faccio

amplifying current mirror

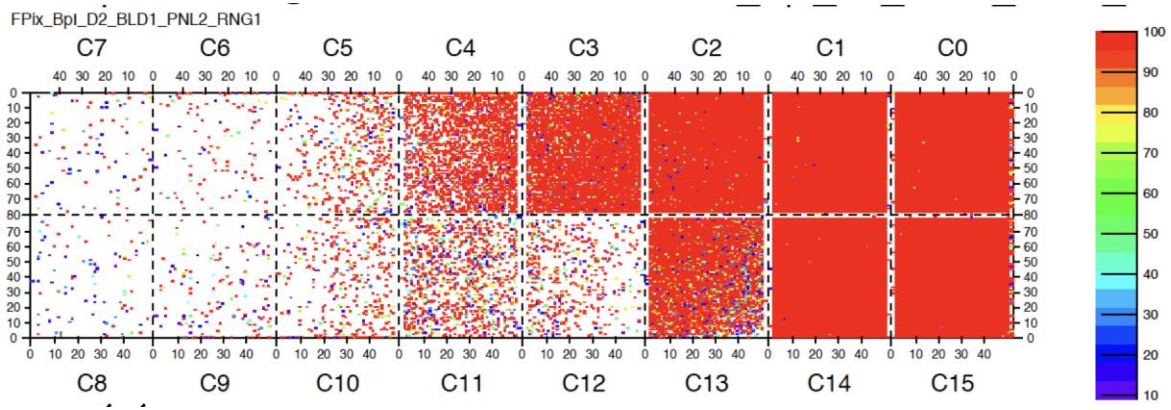
capacitor charging up in the disabled state causing voltage spikes well beyond 3.3V

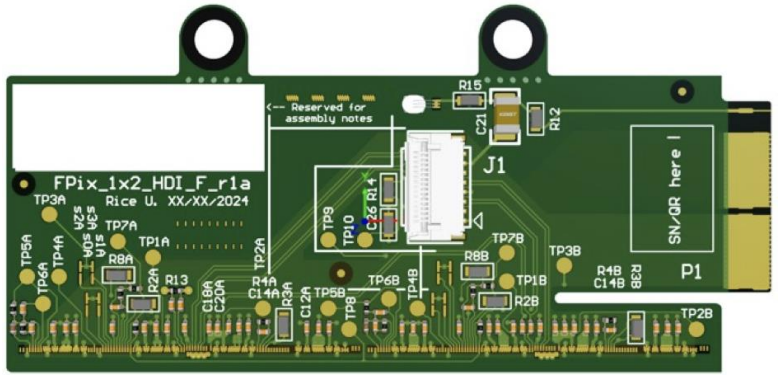
part providing current to the drivers of the power transistors

- All 1200 DC-DC converters replaced in YETS 2017/2018
  - *65 broken*
  - *333 high current*
- Work around in 2018: power cycle from the power supply
  - *Reduce to 9V so currents smaller during on/off sequence*
- Permanent fix FEAST chip new version

DC-DC converter saga (4 of 4)

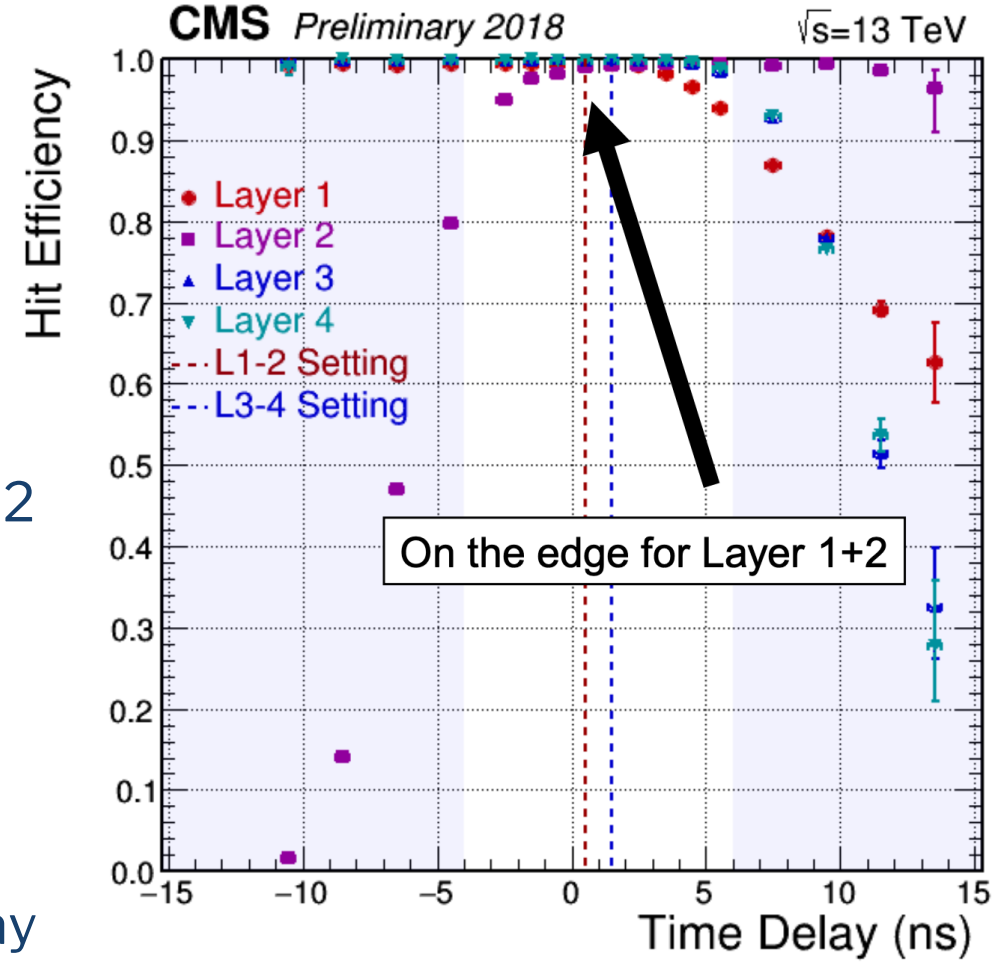
- All DC-DC converters replaced during LS2 with new chip
- Some modules permanently damaged
  - *HV on LV off was not a considered running configuration*
- Fixed the TBM problem. The new layer 1 installed during LS2 does not have the stuck TBM problem
- No TBM for phase 2



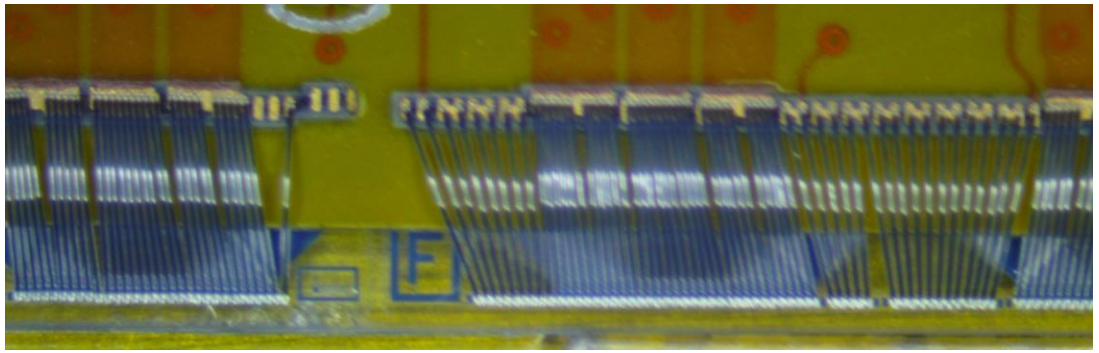


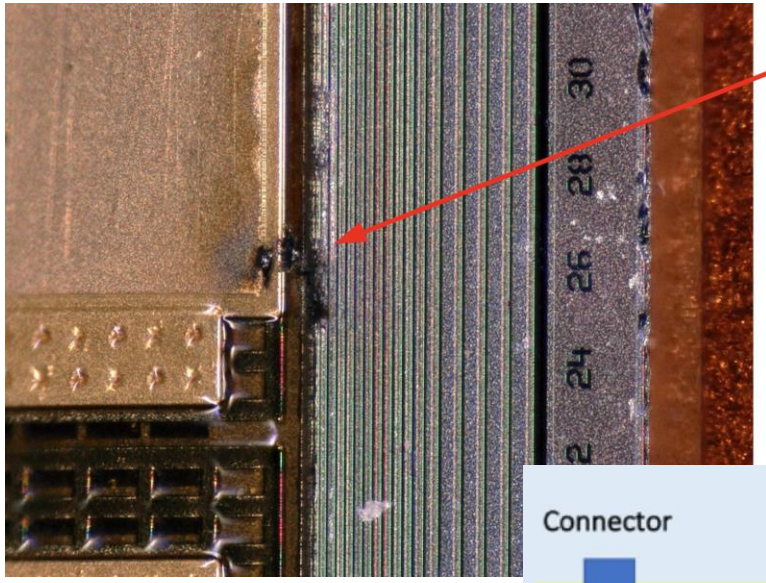
Timing is everything

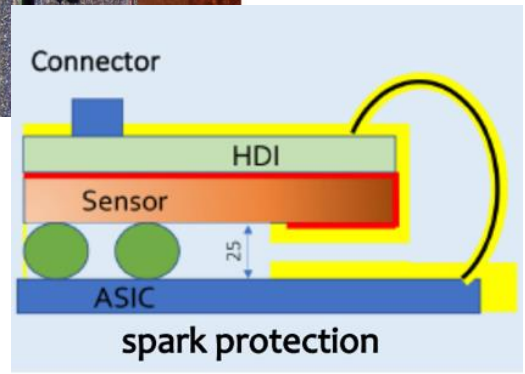
- Layer 1 shifted by ~12 ns with respect to layer 2
  - *Cannot adjust upstream because layers 1 and 2 are on the same clock line*
  - *Layer 1 uses PROC600 while layer 2 uses PSI46dig*
    - PROC is faster
- The new layer 1 installed during LS2 has a delay register in the new TBM to compensate for the differences in PSI46dig and PROC600 timing



Don’t let sparks fly



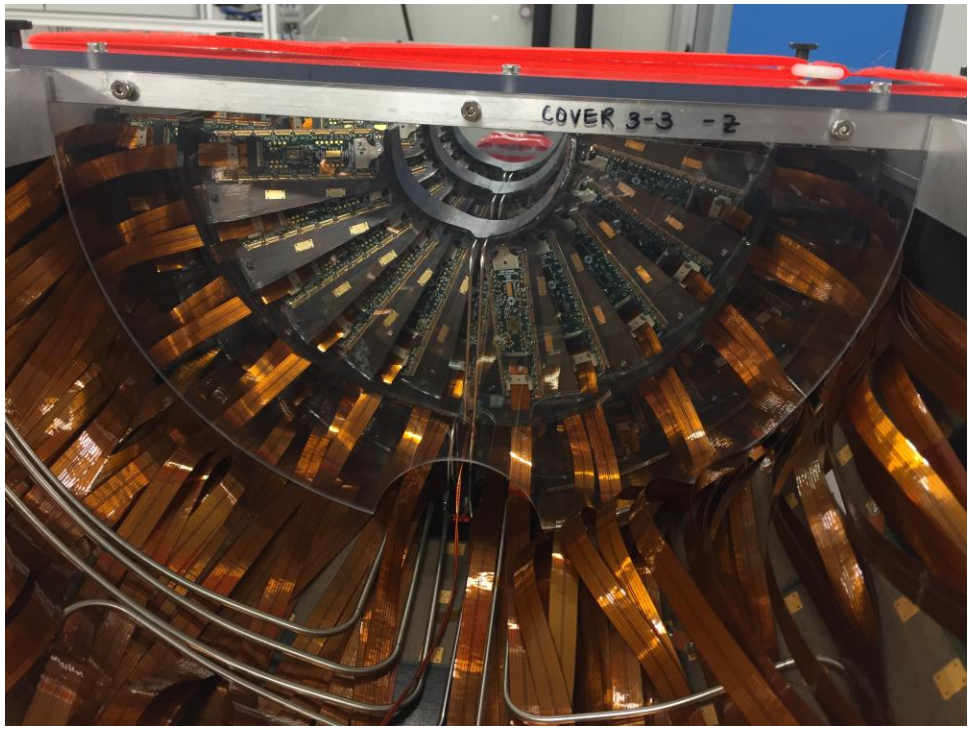




- Two layer 1 modules damaged in 2018 during 600V test
  - *For the rest of 2018 we ran at 450V*
- Sylguard encapsulation of FPix provides spark protection
- When layer 1 replace during LS2 HDI edge increased by 3 times enabling L1 to run at 800V during run 3
- For Phase-2 we are Parylene coating modules

Conclusions

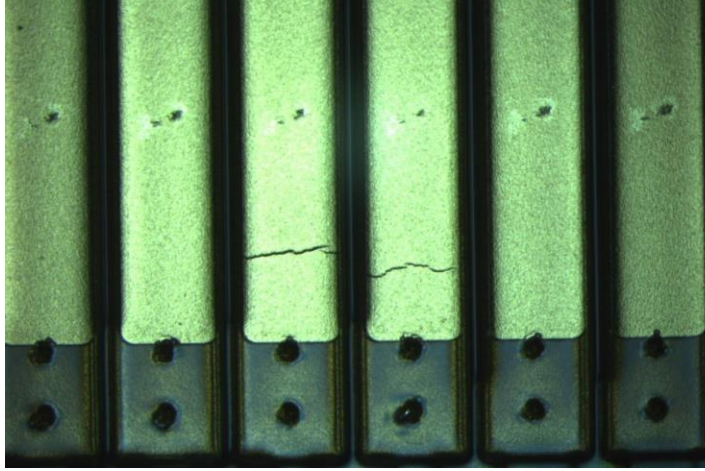
- Experts should remain engaged after detector delivered
- More resources during early operation advisable



Backup

THE CATHOLIC UNIVERSITY OF AMERICA

You get what you pay for



- Phase 1 FPix HDI had lots of problems: over/under etching, shorts between bonds, poor bondablility
- For Phase 2 we are spending more for the HDIs but the saving labor on iterating with vendor and visual inspection