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ATLAS Level-1 Trigger Menu Testing

The ATLAS experiment, located on LHC at CERN, requires a flexible and comprehensive Level-1 (L1) Trigger configuration to meet its diverse scientific goals. A robust framework validates this configuration throughout every year of data-taking. The L1 Central Trigger system (L1CT), integral for the detector trigger, is software-programmable and relies on machine-readable files for L1 Trigger item mapping. Testing involves simulation and a hardware replica of the L1CT itself. With the advanced monitoring capabilities of the system, we can compare the results from the hardware (including intermediate stages) with those from the simulation to cross-check the mapping test. This presentation covers testing methods and challenges due to the ATLAS detector's complexity and introduces a new user interface for the testing framework.

L1 Central Trigger

The ATLAS L1CT is the first stage of **selecting the signal events** of collision events in the LHC. The system is based on custom electronics, and its configuration needs to be tested after any change of the **physics selection** requirements (L1 Trigger Menu).

The test ensures that a particular input fires the expected trigger item, so their mapping is correct. It also validates the hardware replica configuration and simulation software. The connection to the trigger database is tested implicitly.

The parts that need to be tested or otherwise participate in the test:

- Central Trigger Processor (**CTP**)
  - **CTPCORE+**, a processor board which issues the L1 Accept decision (**L1A**)
  - **CTPOUT**, the trigger, timing, and control signal (**TTC**) distribution module
  - **CTPIN**, a trigger input module
- Muon-to-CTP Interface (**MUCTPI**)
- ATLAS Local Trigger Interface (**ALTI**), provides the clock to MUCTPI

Every new L1 Trigger Menu must be **compiled** to produce binary **configuration files** readable by the L1CT electronics.

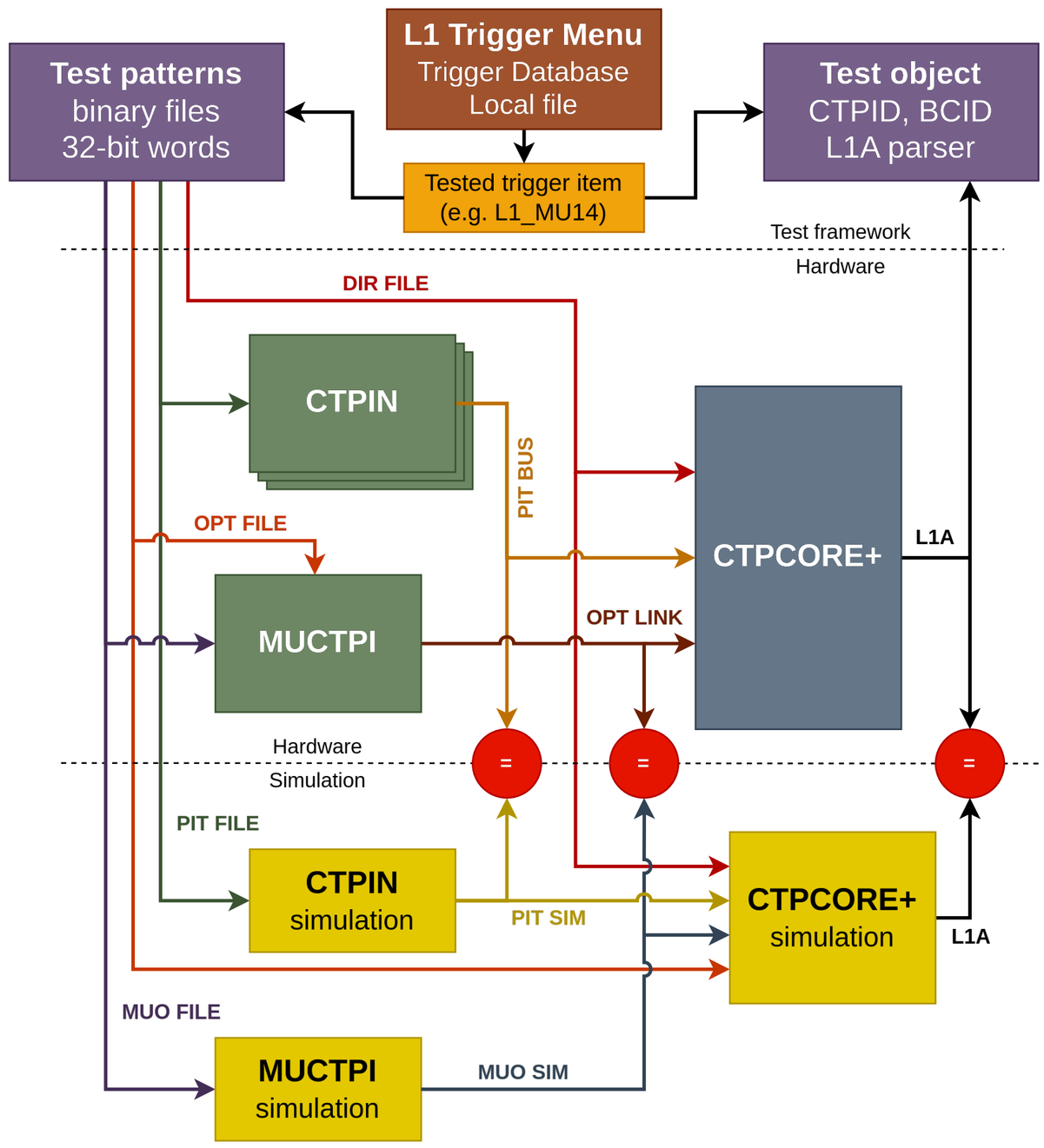
The electronic components that are configured by the files:

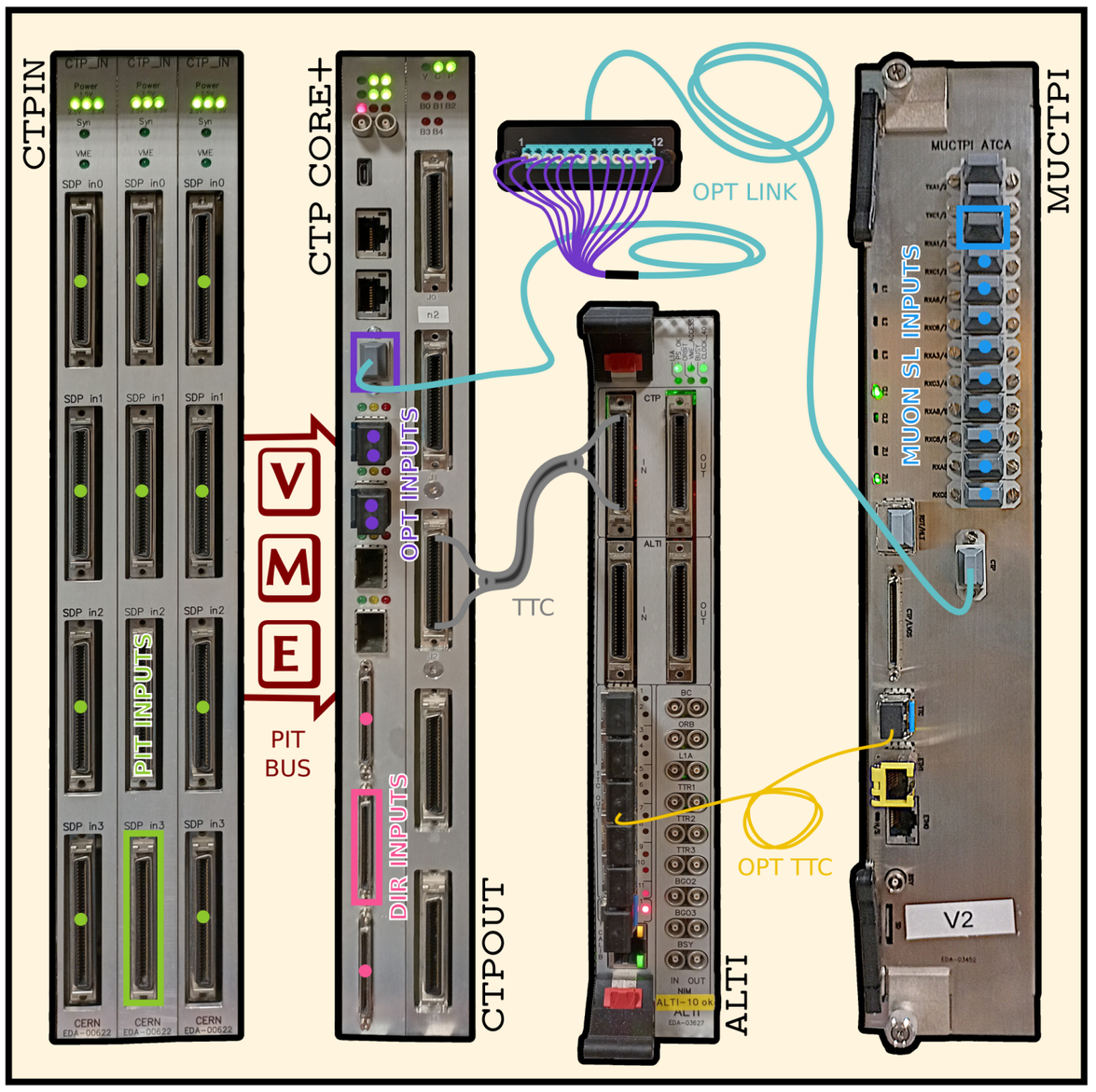
- Content Addressable Memory (**CAM**)
  - CTPCORE+
- Look-Up Tables (**LUT**s)
  - CTPCORE+
  - MUCTPI (one file for the Barrel and one for the End-Caps)
- Switch Matrices (**SMX**s)
  - CTPCORE+
  - CTPIN (SMX for each module)

Inputs and their emulation

- **Direct electrical** (**DIR**) input is tested using input diagnostic memories of the CTPCORE+.
- CTPIN electrical inputs are transferred to CTPCORE+ over the **Pattern-In-Time** bus (**PIT**) in the VME crate (electronics housing device), playback memories of the CTPIN are utilized in this case.
- **Direct optical** (**OPT**) input is emulated using the Trigger Readout Processor (TRP) of the MUCTPI serving as a pattern generator.
- **Muon** (**MUO**) signal in the MUCTPI sector logic (**SL**) is sent from snap-shot memories at the input of its Muon Sector Processor. The signal goes throughout the board, the MUCTPI is therefore thoroughly tested.

Test Framework Outline and Hardware Setup





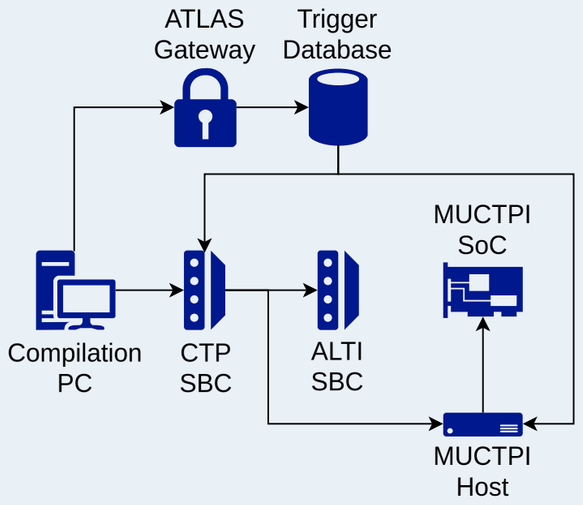
Test Workflow

1) After the **compilation**, the resulting files are stored in the trigger database located at the experiment (LHC Point 1). It is protected by the **ATLAS Gateway**, the access manager for the experiment's internal network.

2) The menu is processed once again to produce the **testing pattern** files. Words (32bit) in those binary files represent individual tests of all trigger items in the menu.

3) The test is first run in the **software simulation** mode.

4) The **hardware test** begins with restarting the CTPCORE+, configuring necessary parameters, and loading all configuration files from the database (validation of the previous upload). This has to be done from a single-board computer (**SBC**) connected to the same VME crate as the CTP. Depending on the test type (DIR, PIT, OPT, or MUO), the testing pattern is loaded to the corresponding **memory** in the L1CT hardware. The last two tests utilize the MUCTPI, which demands extra configuration steps, and setup of the corresponding ALTI module. The former is accessed through the **MUCTPI Host** computer, a gateway to the MUCTPI System on Chip (**SoC**). The latter has its own SBC. The IT-level description of the computer network involved in the test is depicted below.



5) Finally the L1A word is captured, parsed, and compared with the simulation word and the software **Test object**. The object contains all properties and IDs of the trigger item:

- trigger item ID (**CTPID**),
- expected bunch-crossing (**BCID**),
- physics object **multiplicity**,
- trigger type, and input **origin**.

A detailed printout of all tests as well as a summary table are printed at the end of the test execution in a new python-based user interface.

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