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From software to hardware: An easy guide to accelerate algorithms for the HL-LHC upgrades of CMS trigger system

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At the LHC, the vast amount of data from the experiments demands both sophisticated algorithms and substantial computational power for efficient processing. Hardware acceleration is an essential advancement for HEP data processing, focusing specifically on the application of High-Level Synthesis (HLS) to bridge the gap between complex software algorithms and their hardware implementation. We will explore how HLS facilitates the direct implementation of software algorithms into hardware platforms such as FPGAs to enable real-time data analysis. We will use the case study of a track-finding algorithm for muon reconstruction with the CMS experiment, demonstrating HLS's role in translating algorithms into high-speed, low-latency hardware solutions that improve the accuracy and speed of particle detection. Key techniques in HLS, including parallel processing, pipelining, and memory optimization, will be discussed, illustrating how they contribute to the efficient acceleration of algorithms.

Alternate track

I read the instructions above

Yes

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