The W-Si High Precision Preshower Detector of the FASER Experiment at the LHC

Andrea Pizarro Medina, on behalf of the FASER collaboration

FASER

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UNIVERSITÉ DE GENÈVE

Introduction & Outline

Today's talk:

- FASER experiment overview
- Upgrade of preshower
- Monolithic silicon pixel ASIC

Other talks on the FASER experiment :

- Jack MacDonald: *New Physics Results from the FASER Experiment* (20/07, 16:45)
- Sergey Dmitrievsky: *Results from TeV Neutrinos at the FASER Experiment* (18/07)
- Alan Barr: *The Forward Physics Facility and its experiments* (19/07)

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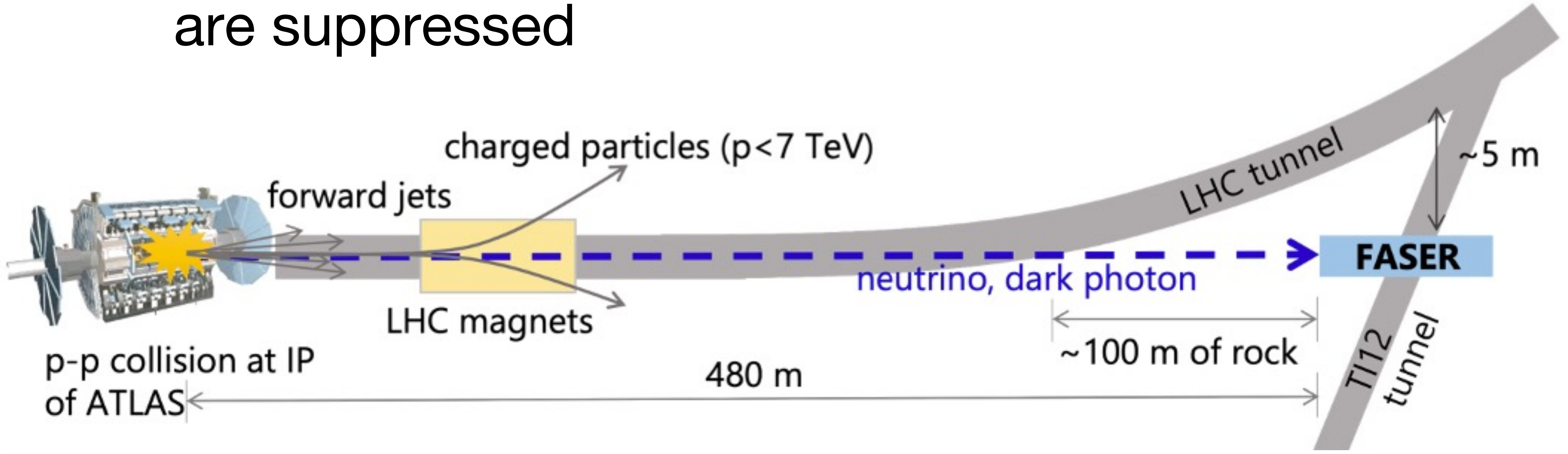
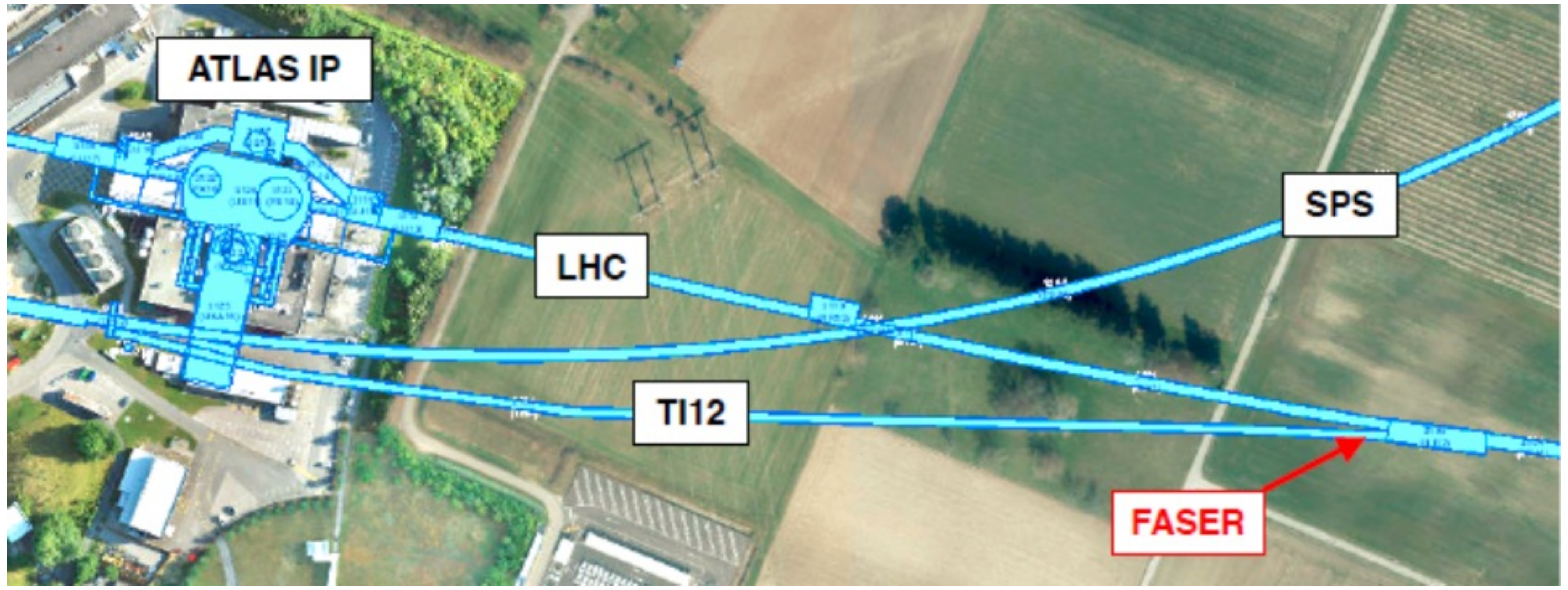
The ForwArd Search ExpeRiment at the LHC

Search for light, weakly interacting (LLP) new particles

↪ Originating from rare meson decays (π, η, K, D, B ...) in very forward ATLAS region ($\theta \sim$ mrad)

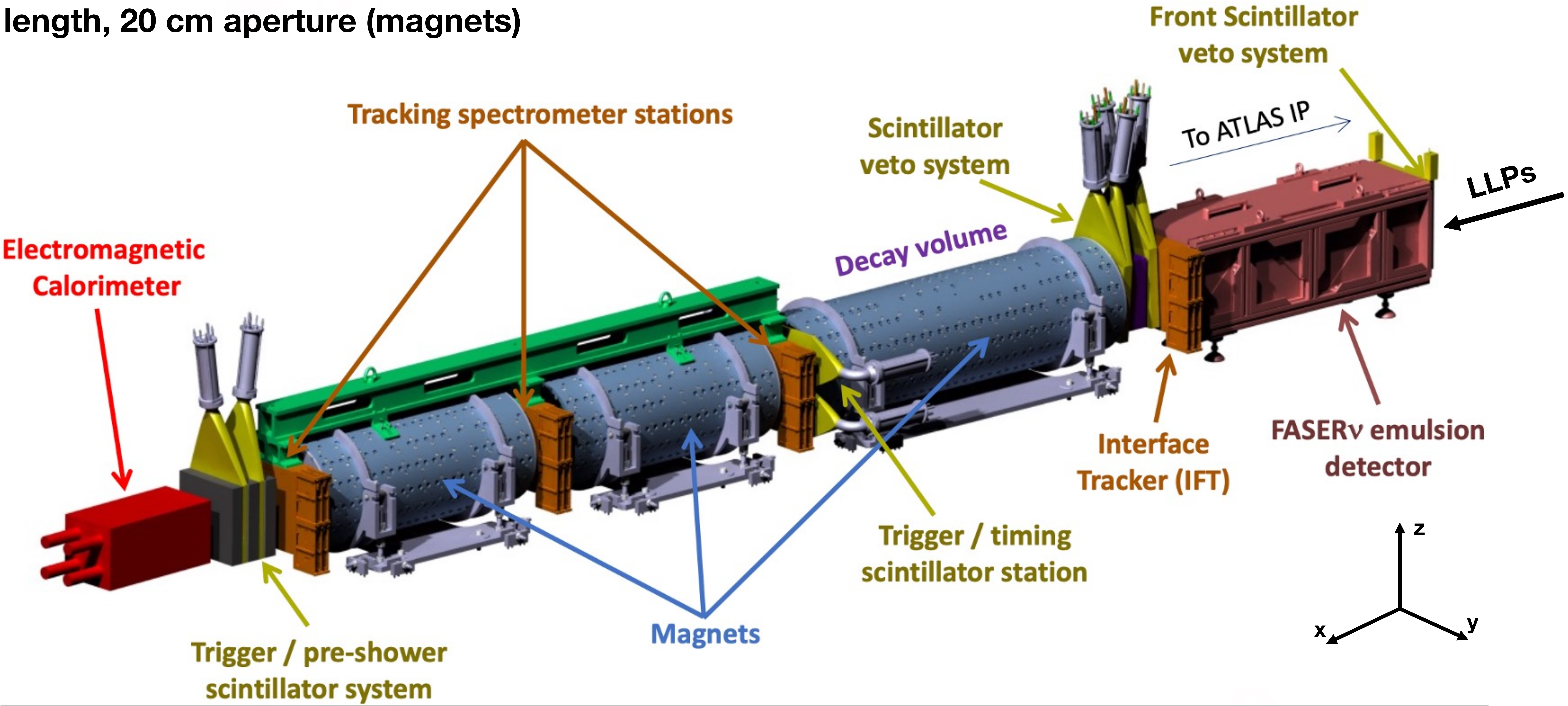
↪ Fluxes of high-energy SM particles reaching FASER are suppressed





The FASER experiment

≃ 7 m length, 20 cm aperture (magnets)



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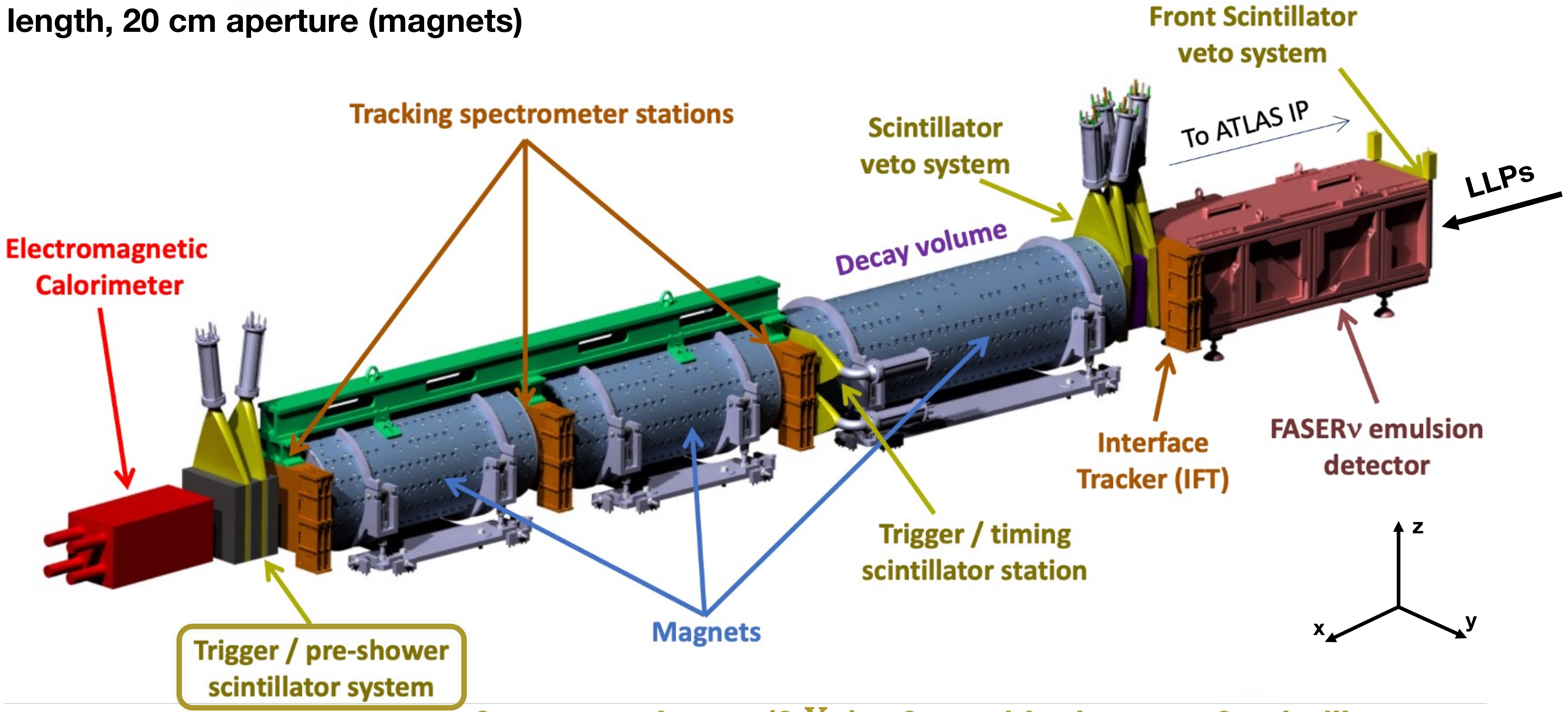
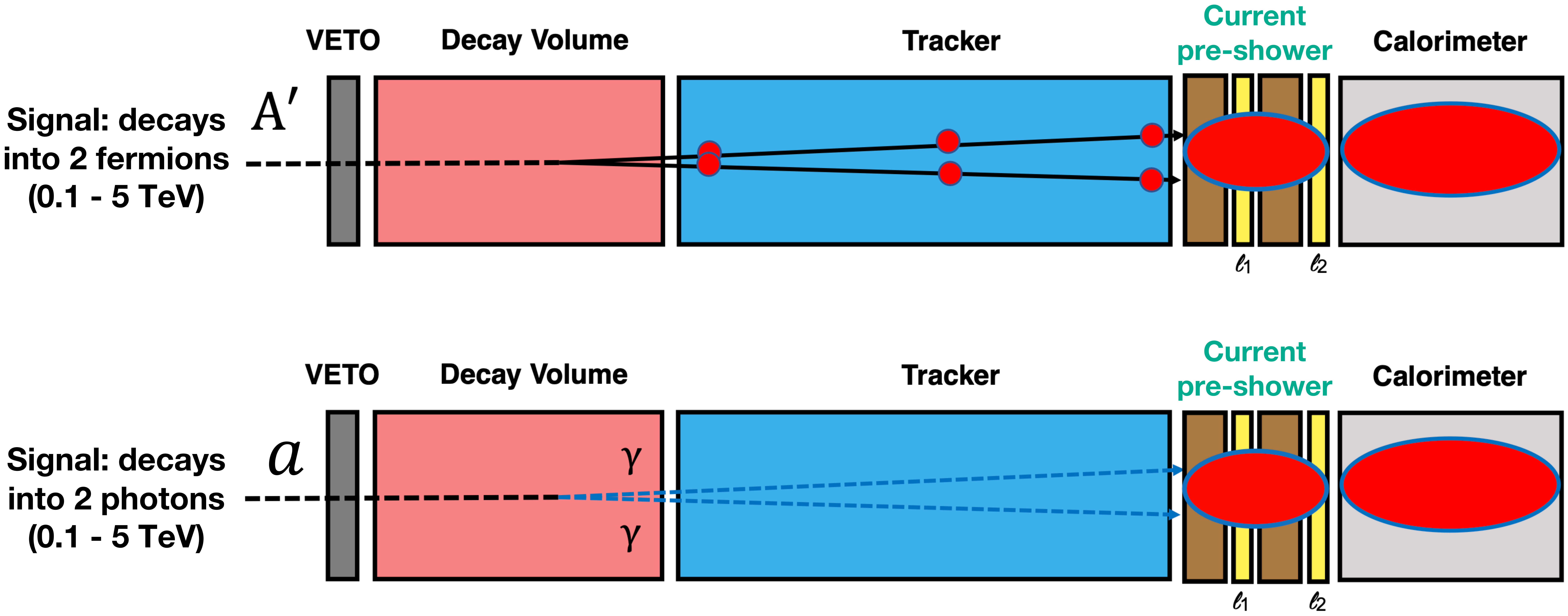


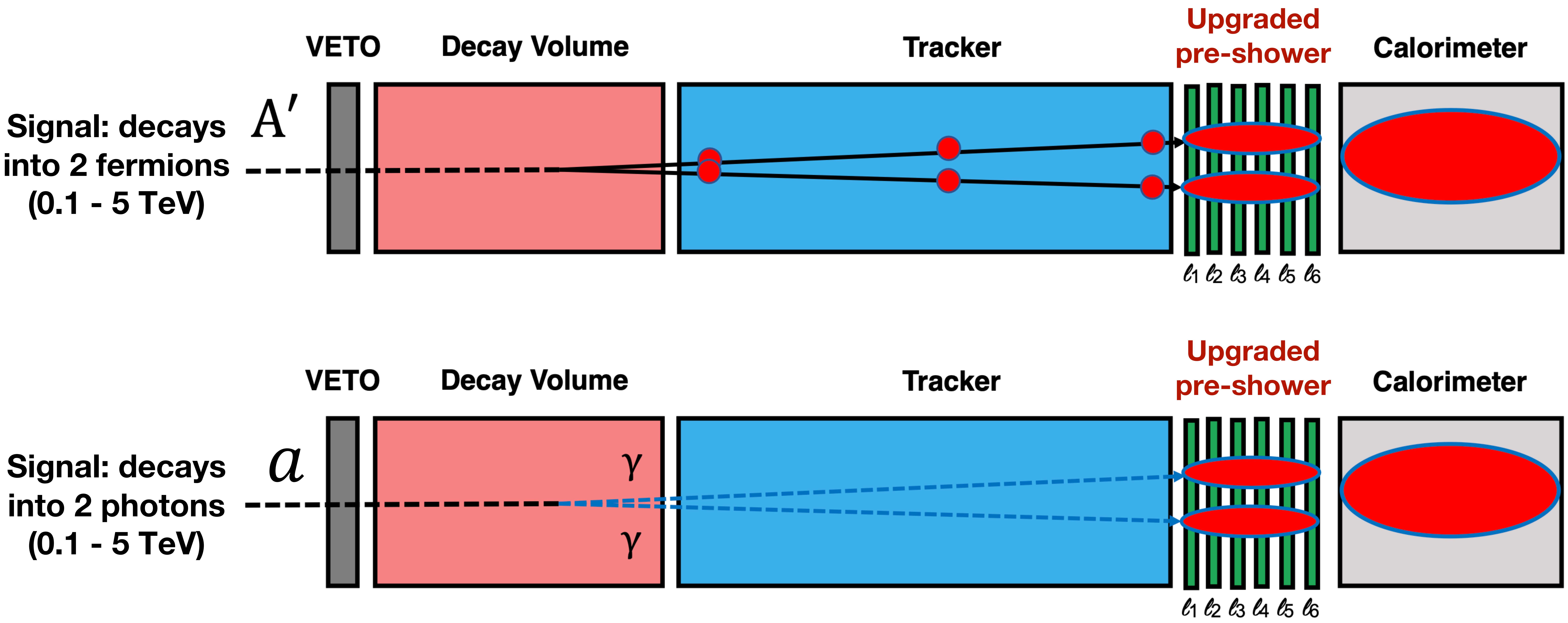
2 tungsten layers (2 X_0) + 2 graphite layers + 2 scintillators

Current Detection Capabilities: Two Fermions

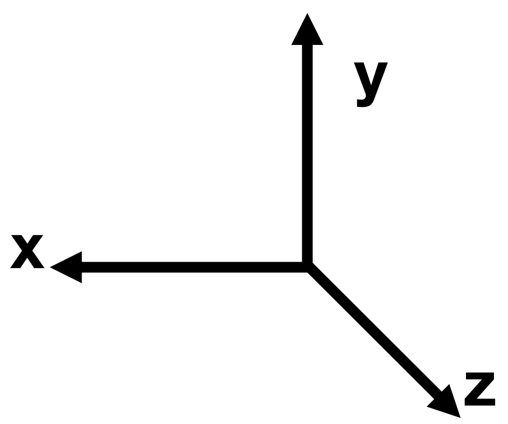


No X-Y granularity: unable to resolve di-photon events !

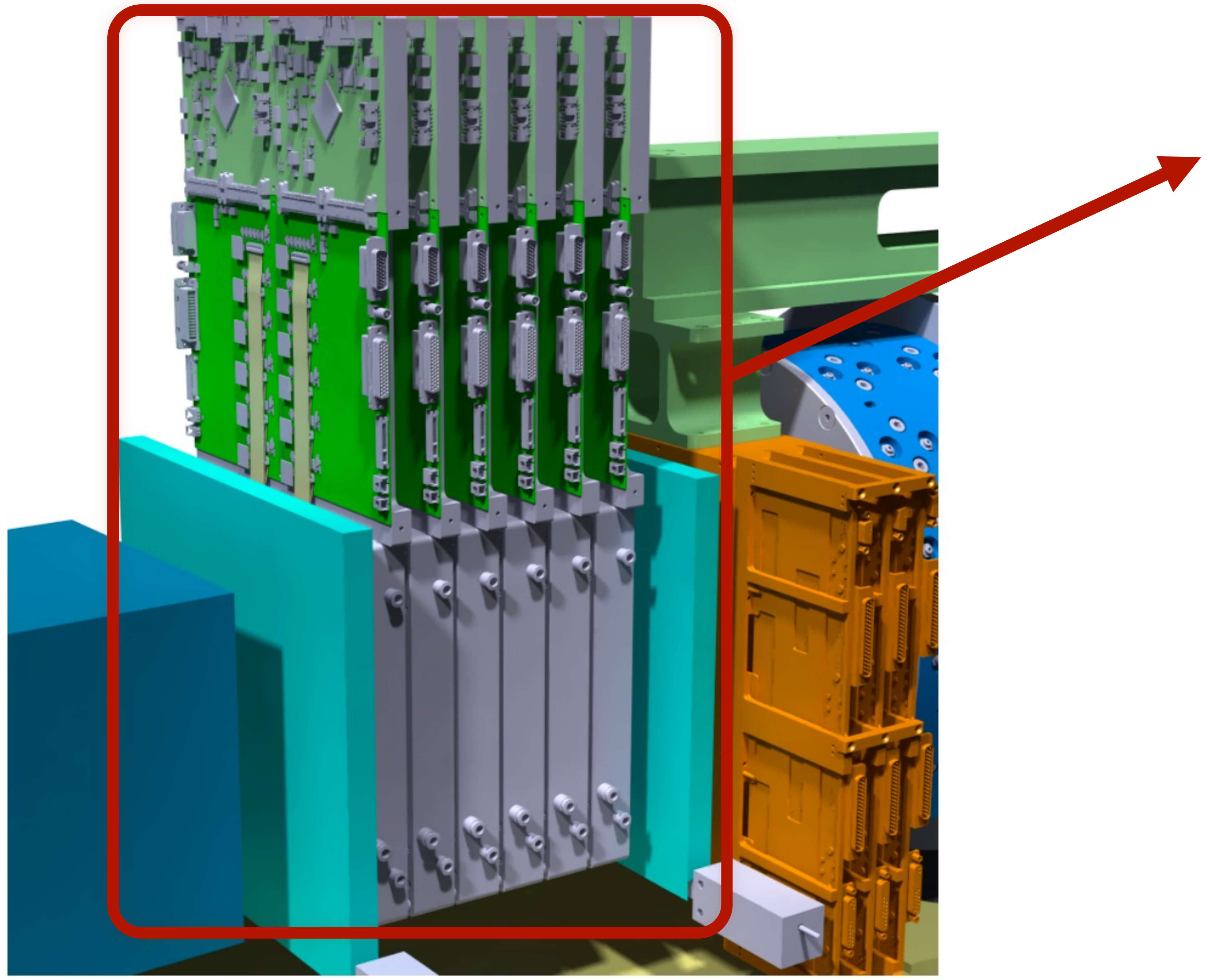
Desired Detection Capabilities: Two Fermions / Photons

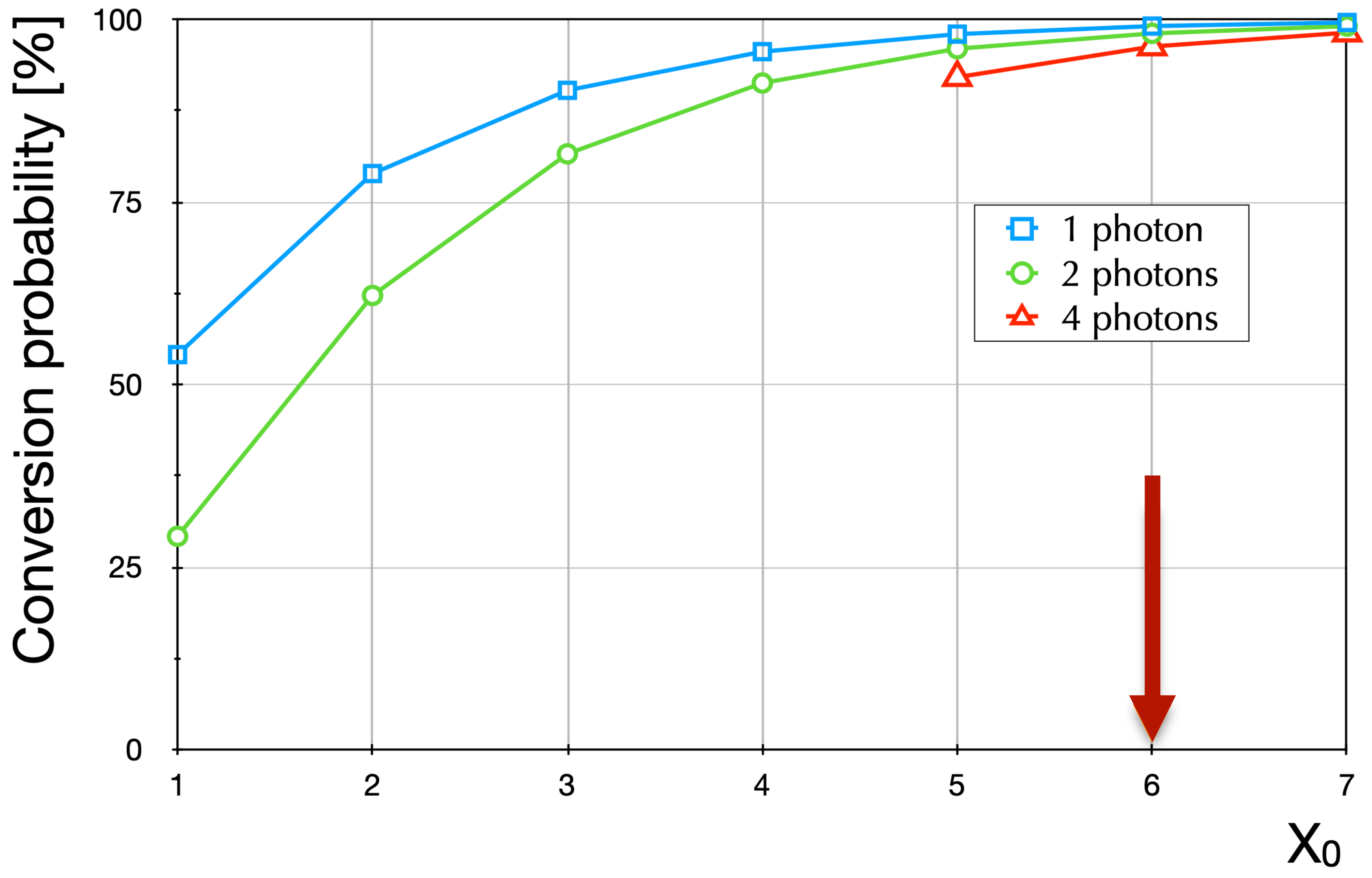


Fine X-Y granularity, high dynamic range



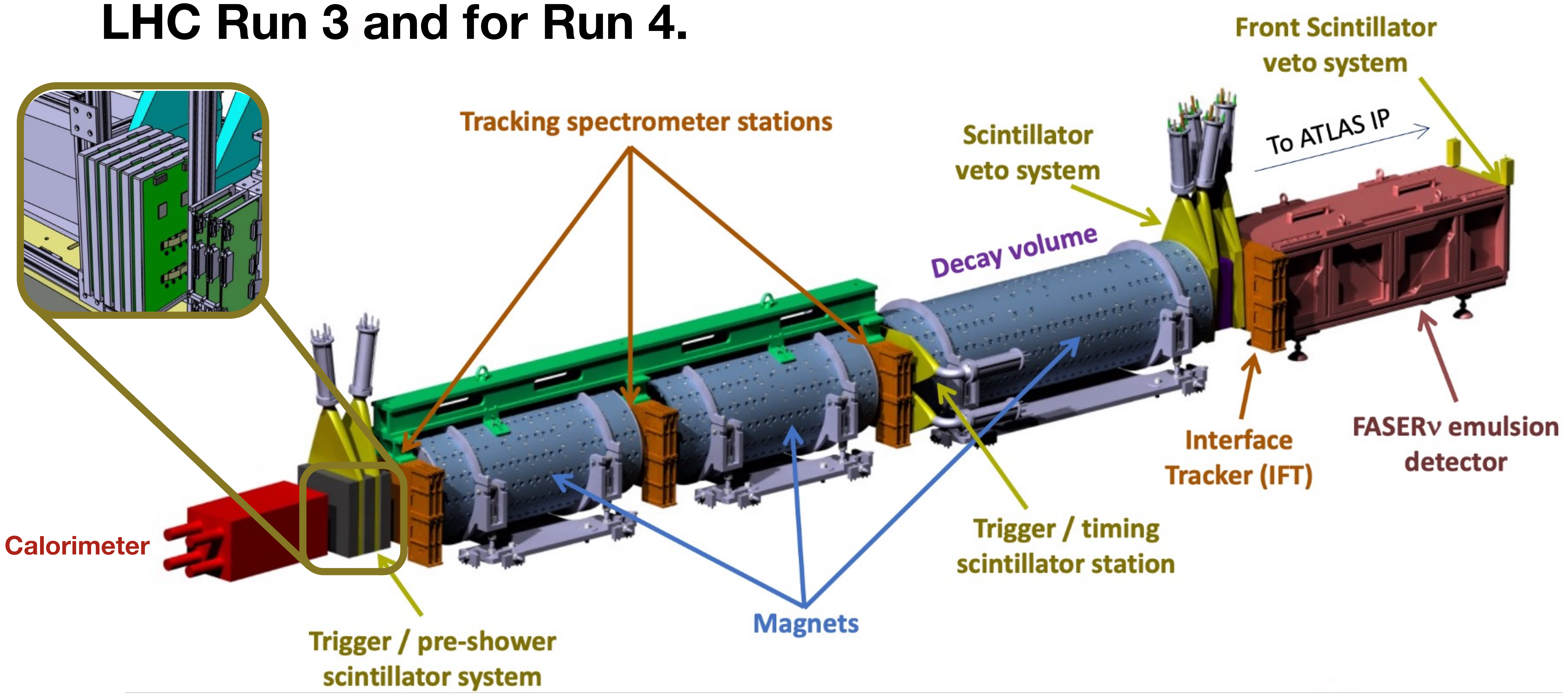
New Preshower detector





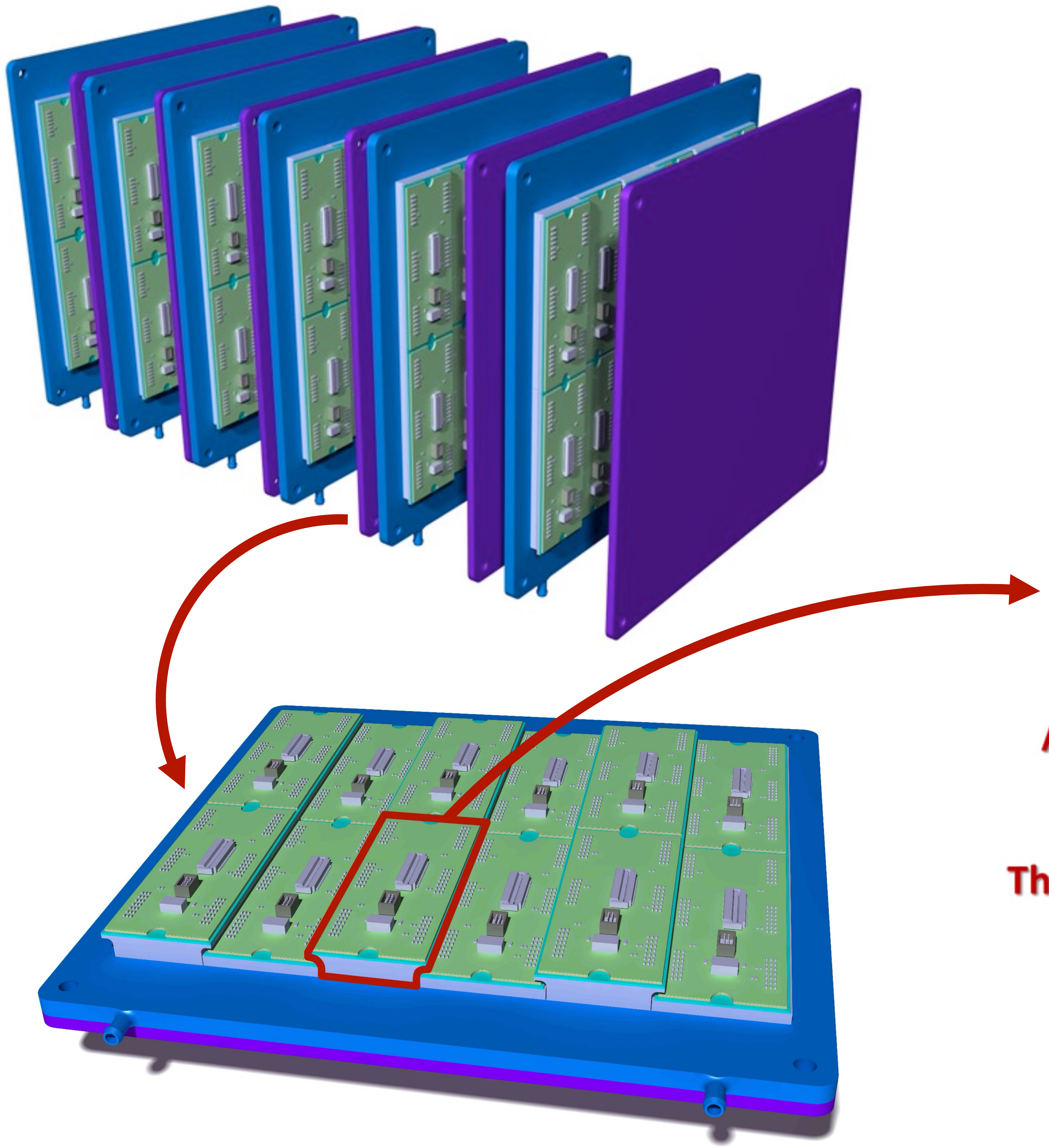
Upgraded preshower detector:

- 6 detector planes + 2 scintillators
  - ↪ $2 \times (1.70\ X_0$ of W + Si plane$) + 4 \times (0.65\ X_0$ of W + Si plane$)$
- Project approved by CERN:
  - ↪ CERN-LHCC-2022-006 (Technical proposal)
- Targeting installation in **December 2024**, run during **last year of LHC Run 3 and for Run 4.**



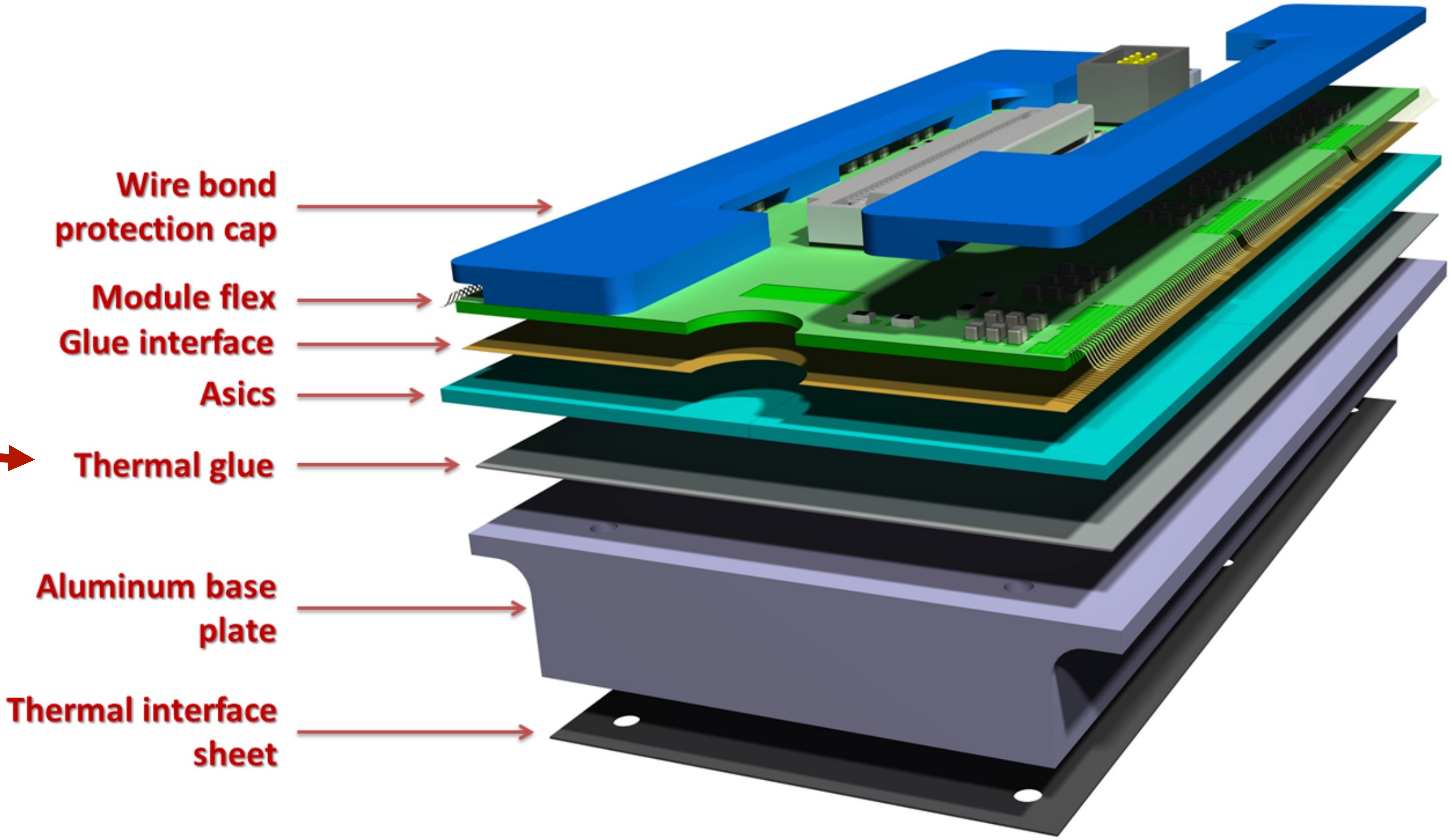
New Preshower detector

6 planes in total (silicon + W plate)



6 ASICs per module, 208x128 pixels each

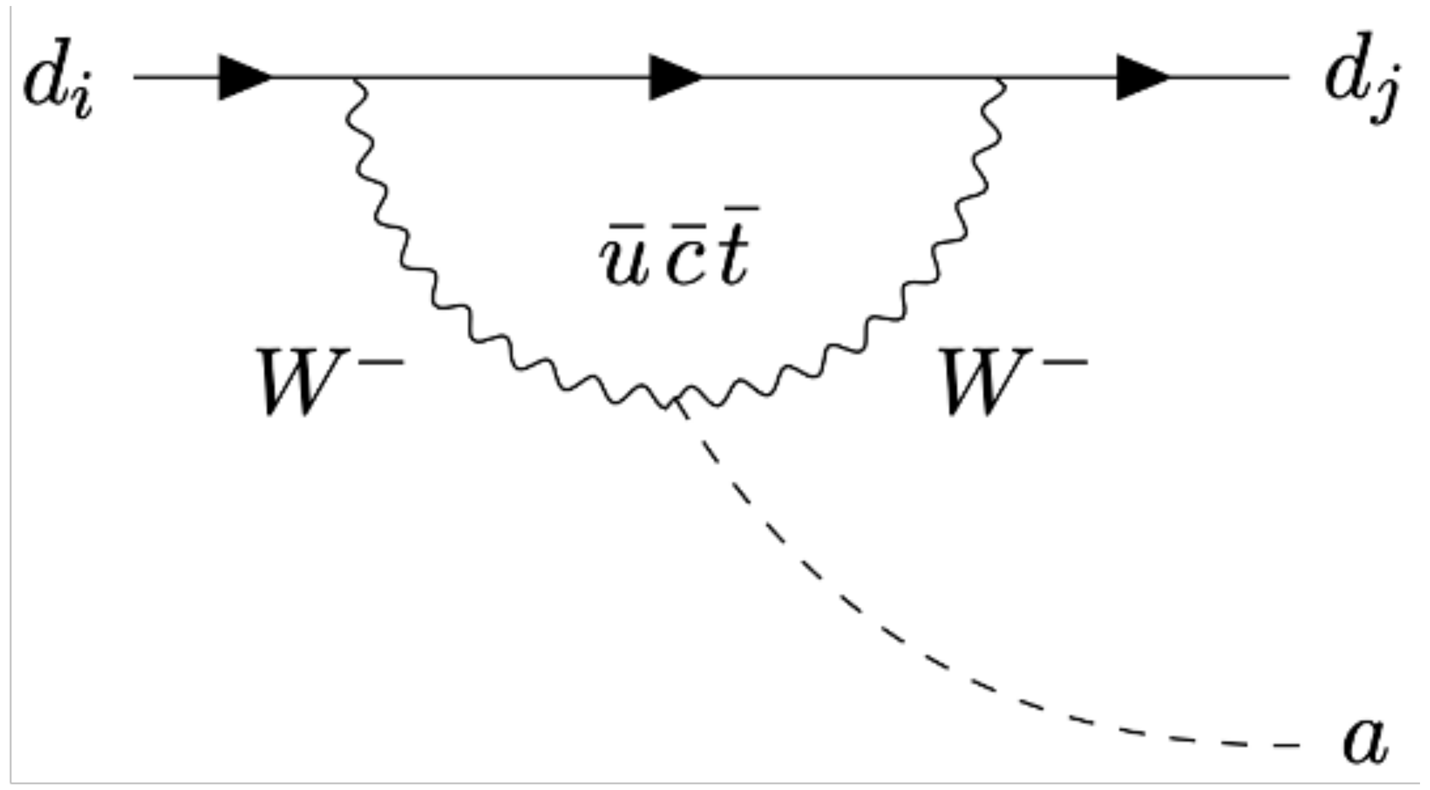
↳ 100 µm pitch hexagonal pixels



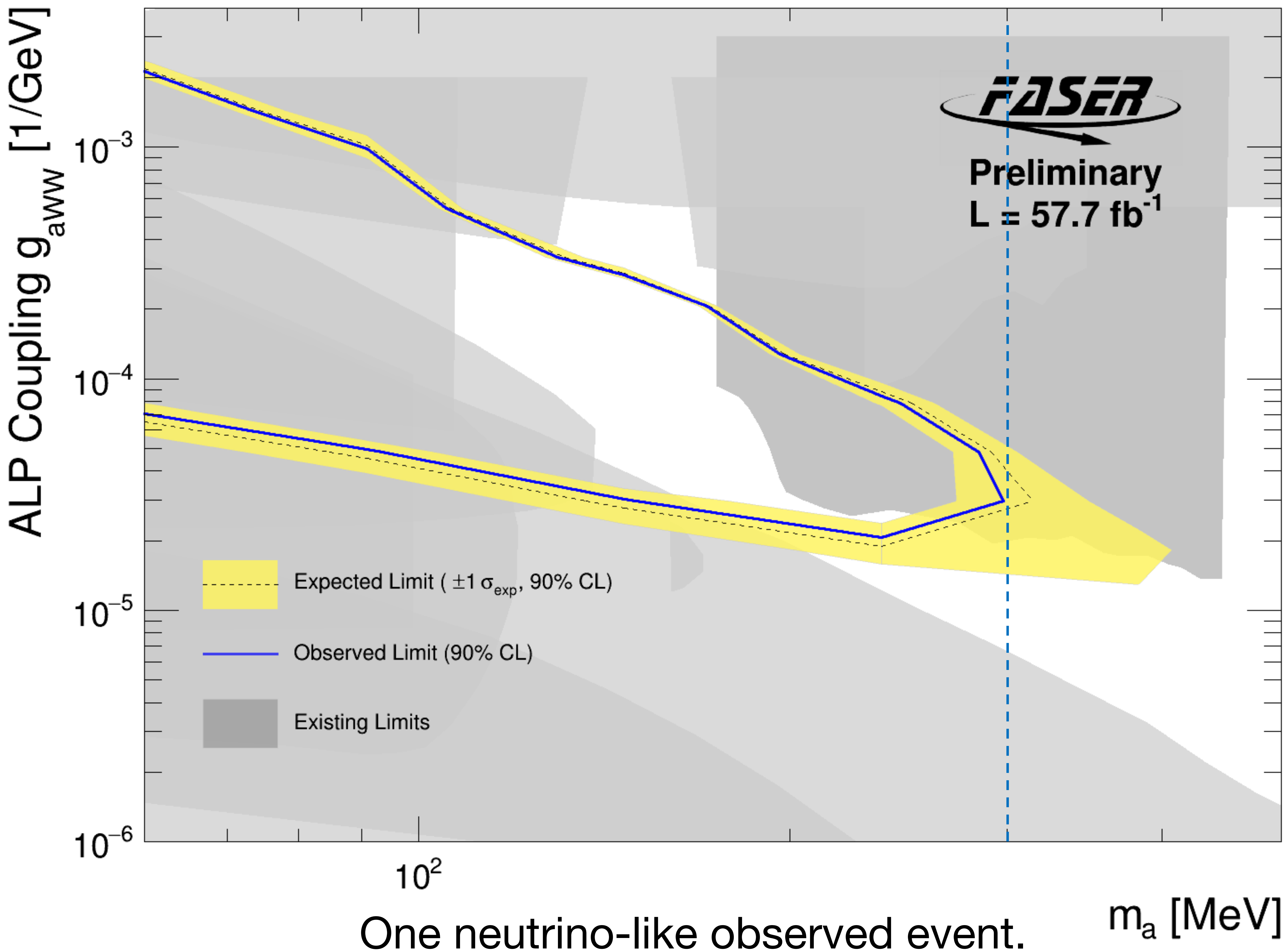
Motivation for upgrade

➡️ FASER can probe Axion-Like-Particles (ALPs) models.

- May be produced at LHC thanks to $(SU2)_L$ coupling with W.
- In this model ALPs decay exclusively into a photon pair.



More details on this benchmark model



One neutrino-like observed event.

More details on the current search for ALPs in FASER

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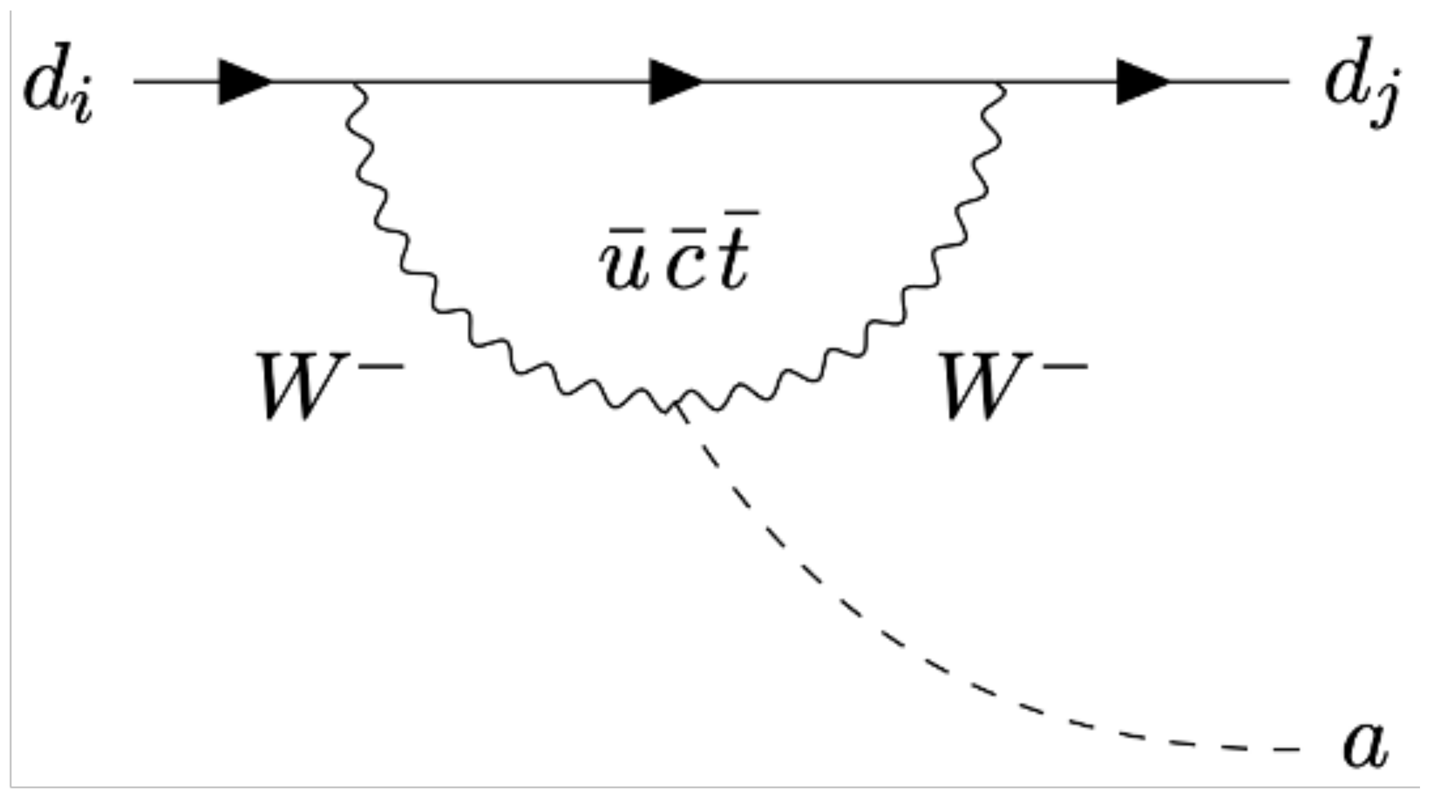
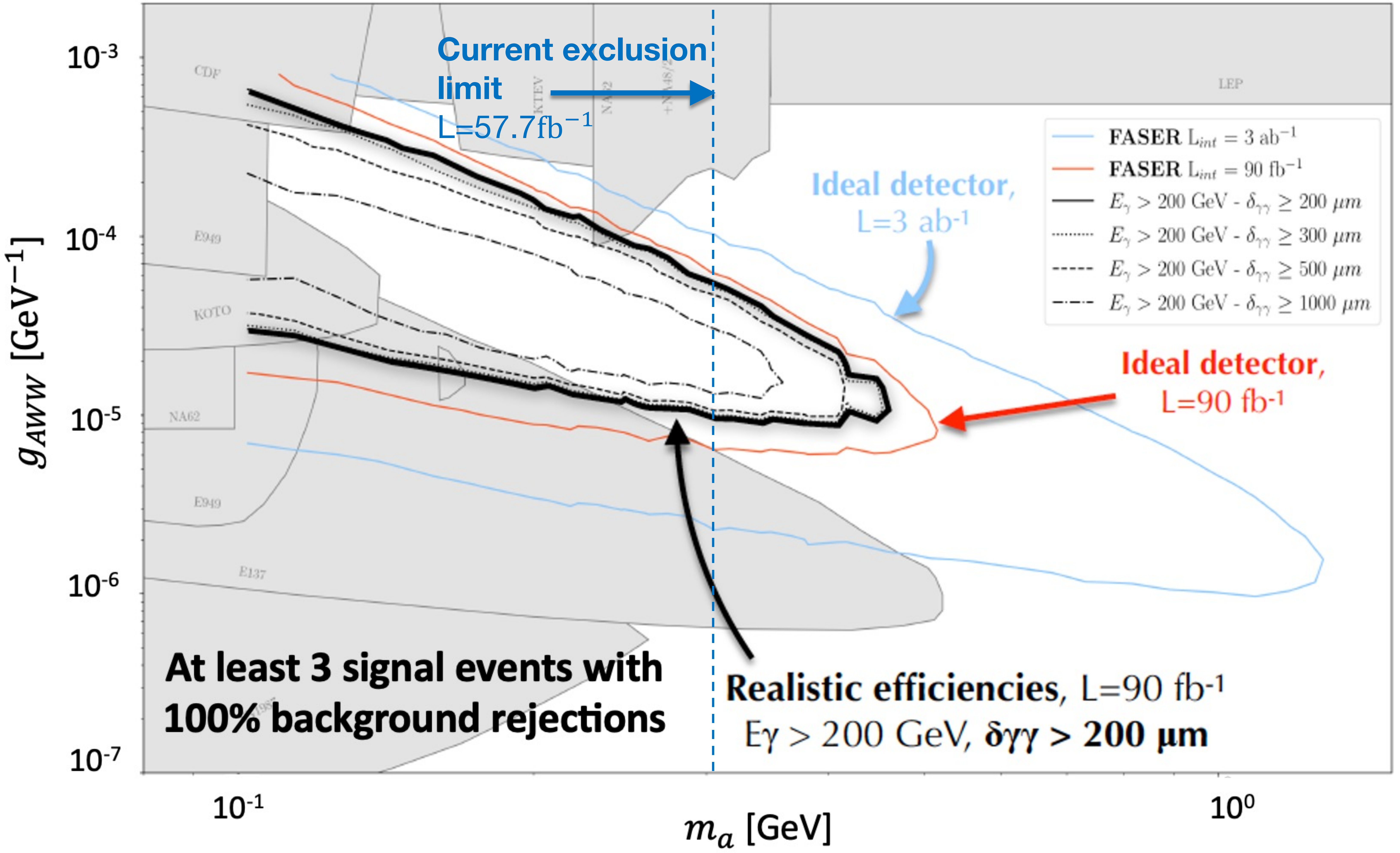


More details on this benchmark model

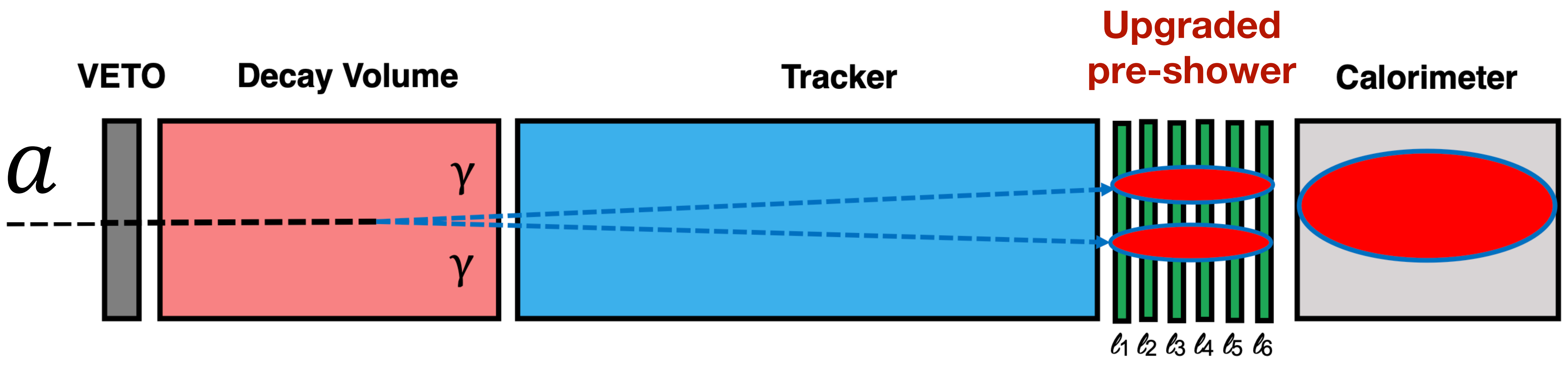
Discovery Potential

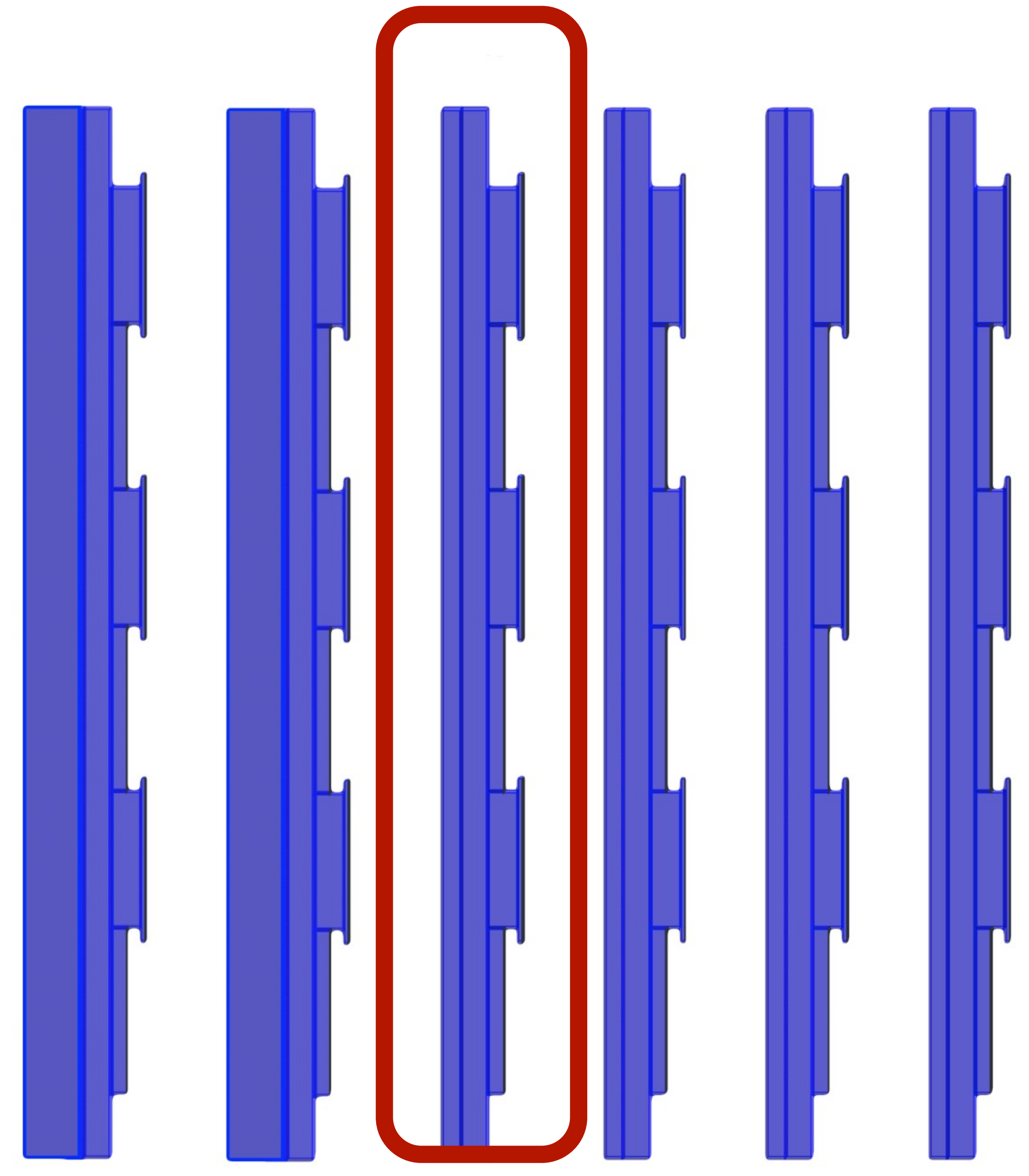


More details on the current search for ALPs in FASER

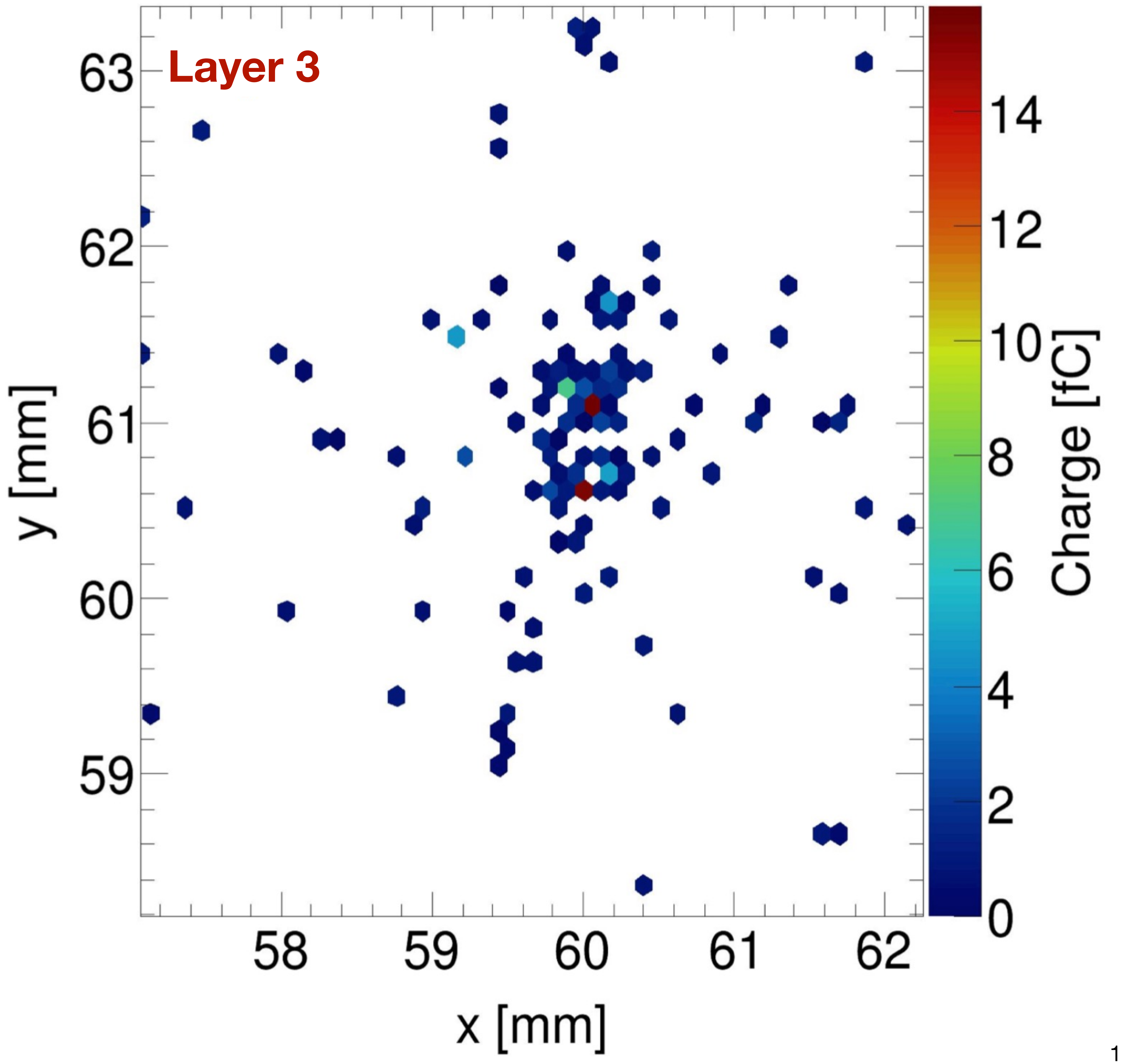
Preshower simulation: Di-photon signature

Why 6 planes ? Why pixelated sensor ?





E_{γ_1} = 1 TeV
E_{γ_2} = 1 TeV
d = 500 μm



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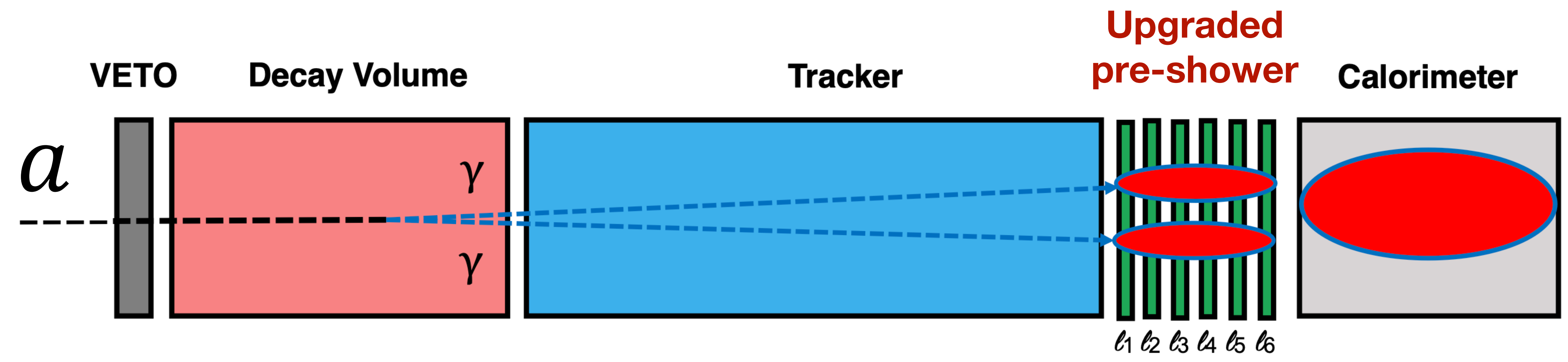

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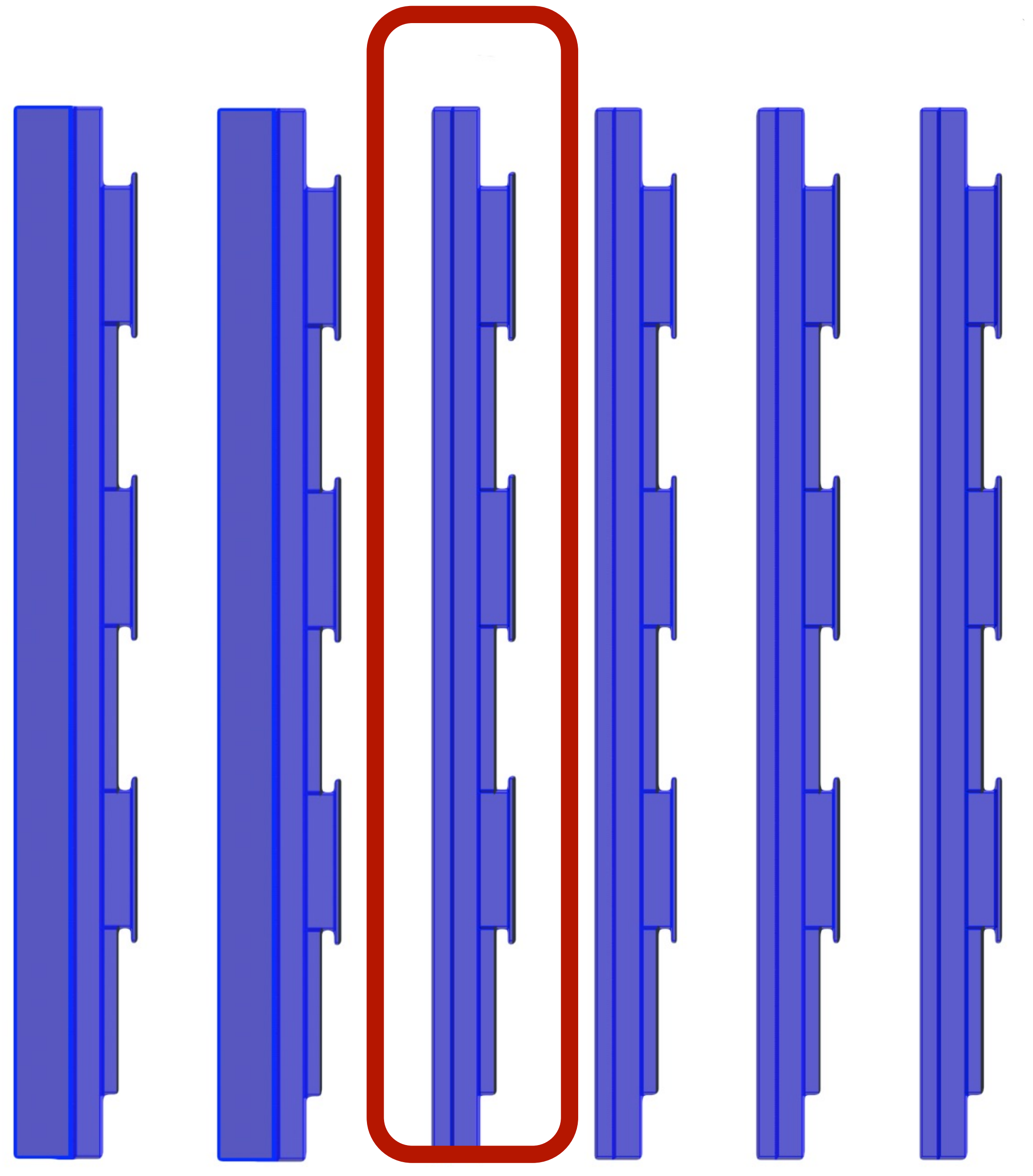

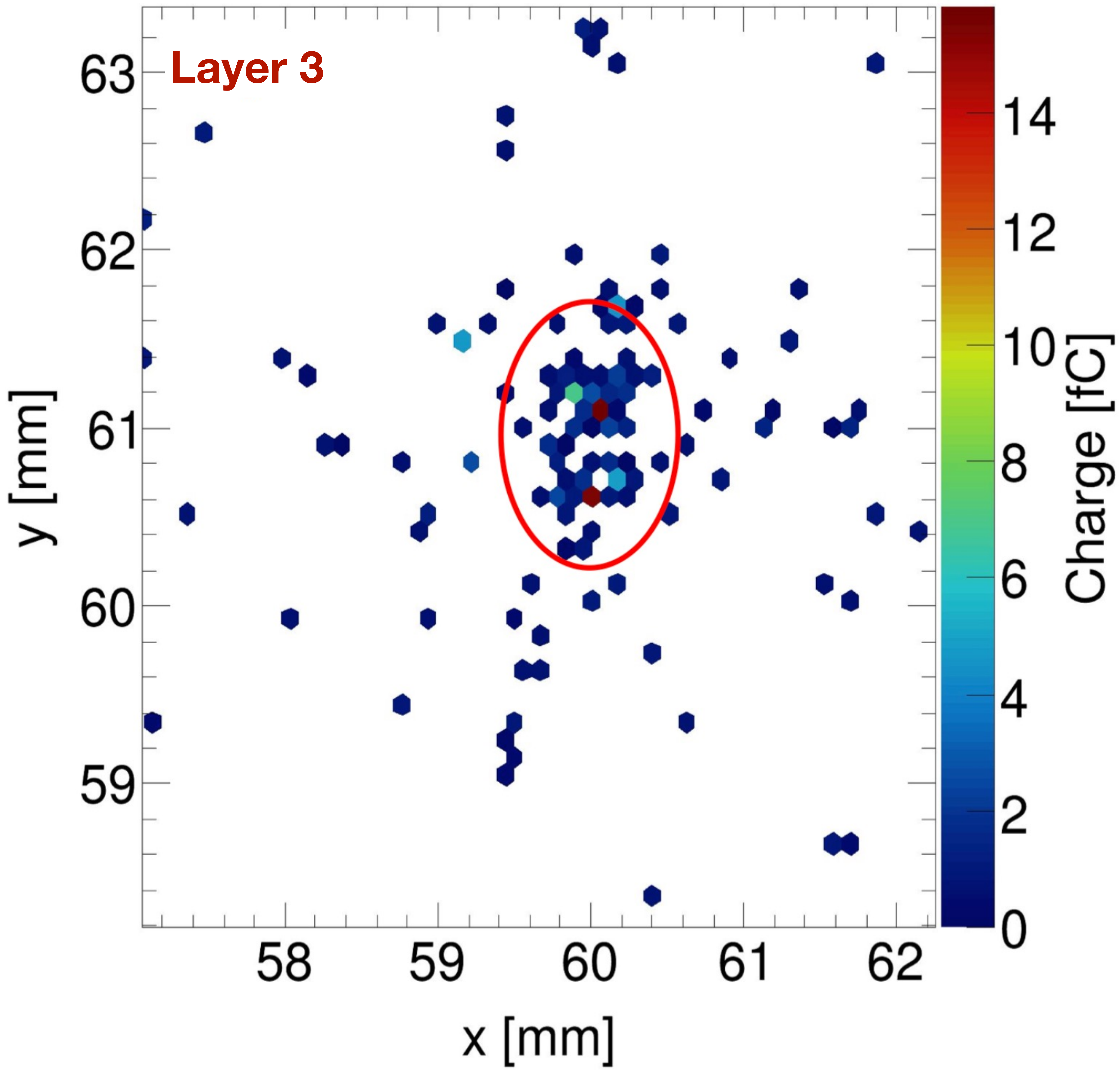

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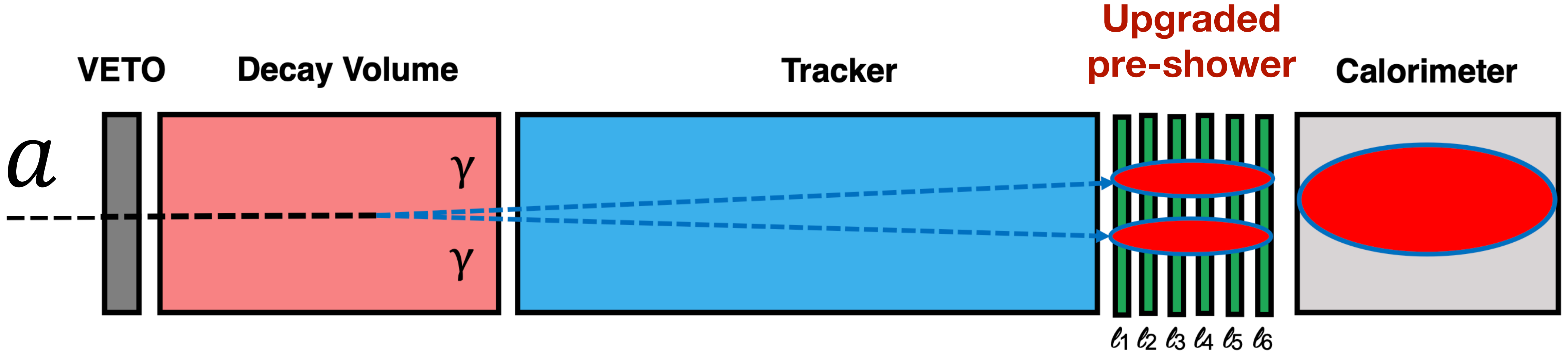

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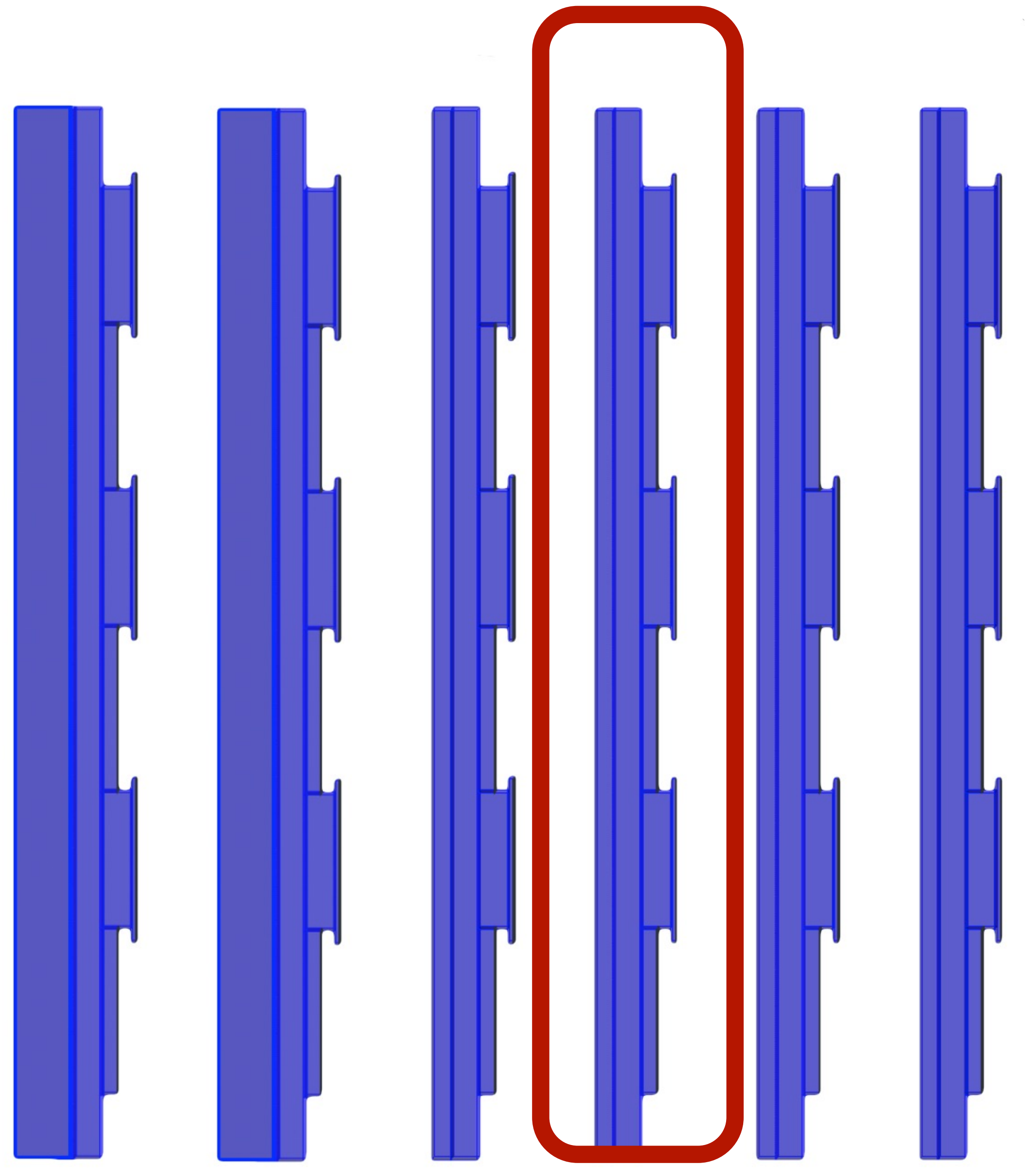

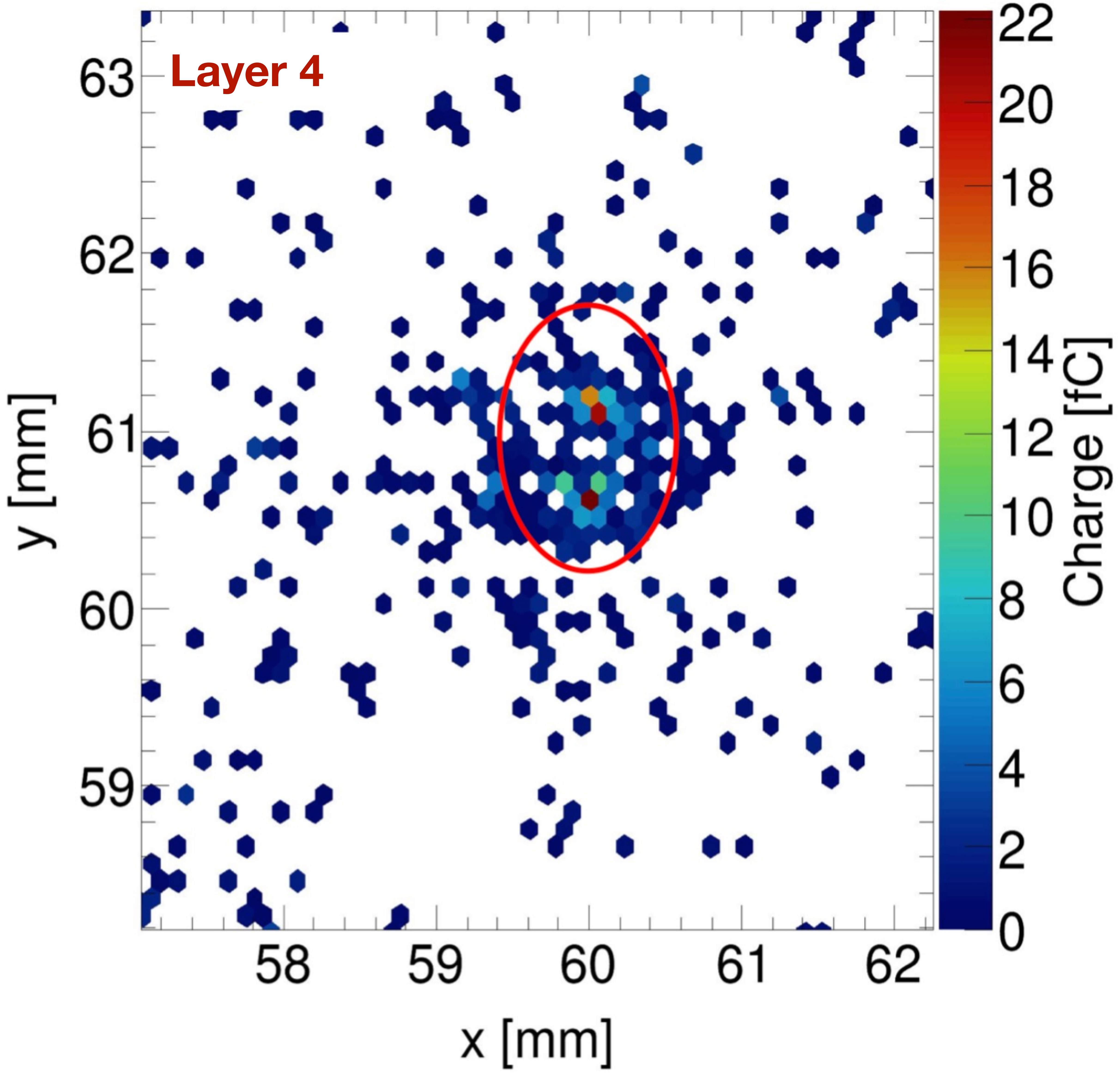

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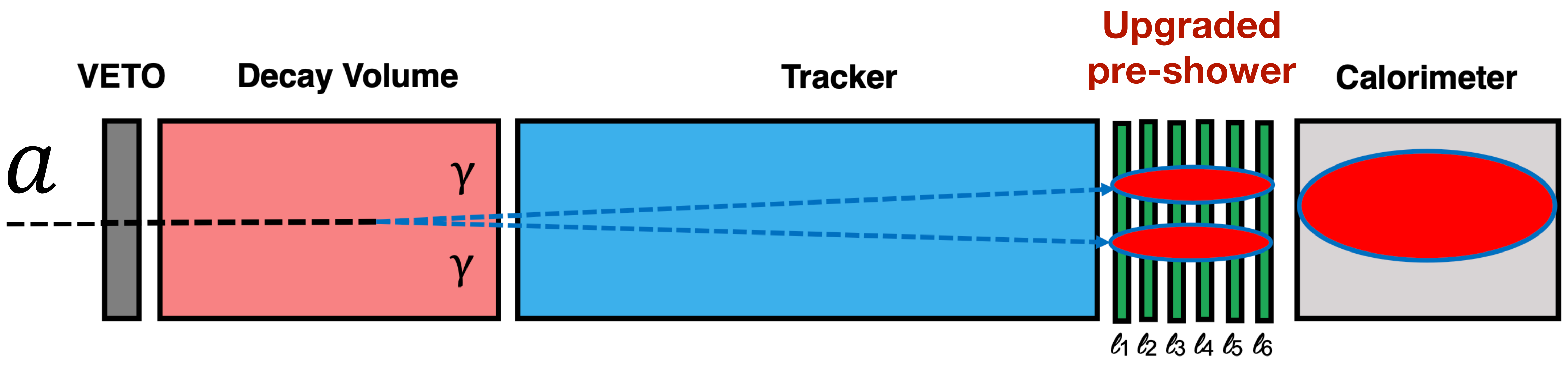

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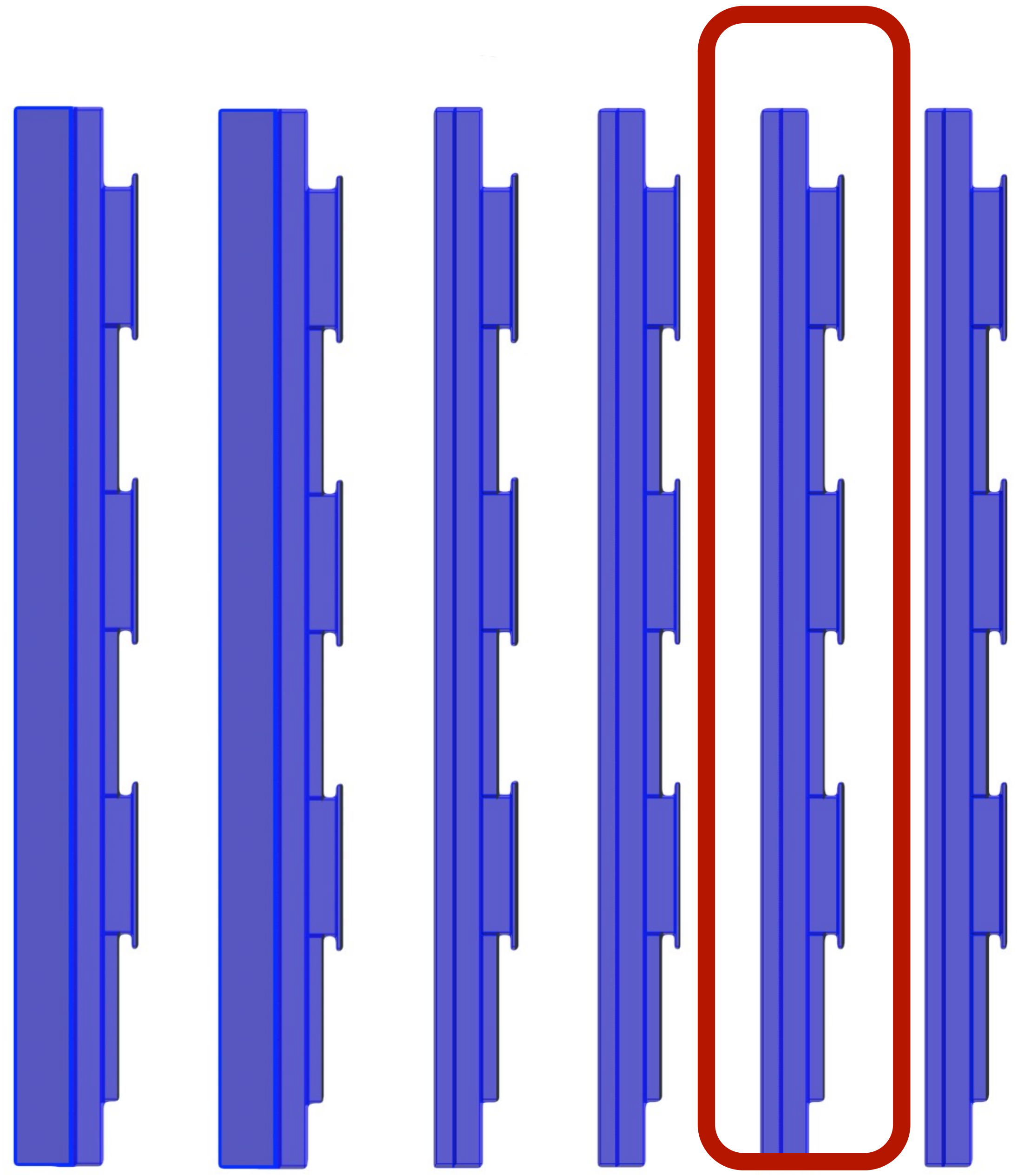

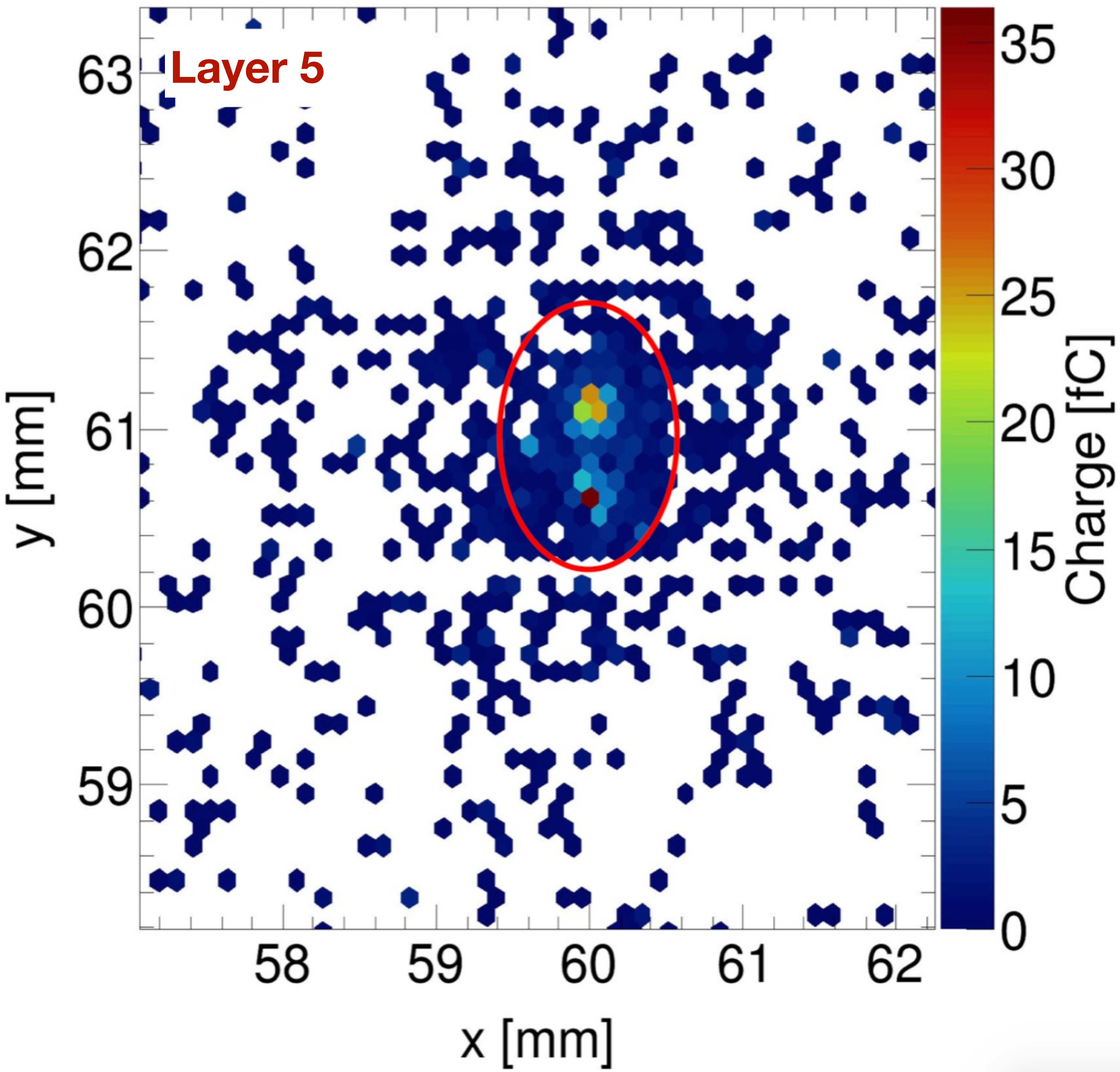

Preshower simulation: Di-photon signature

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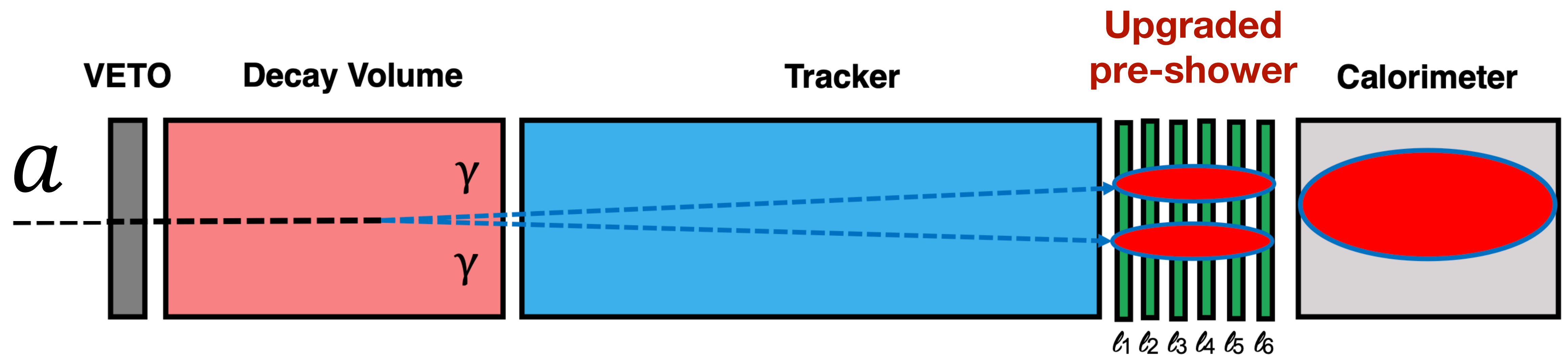

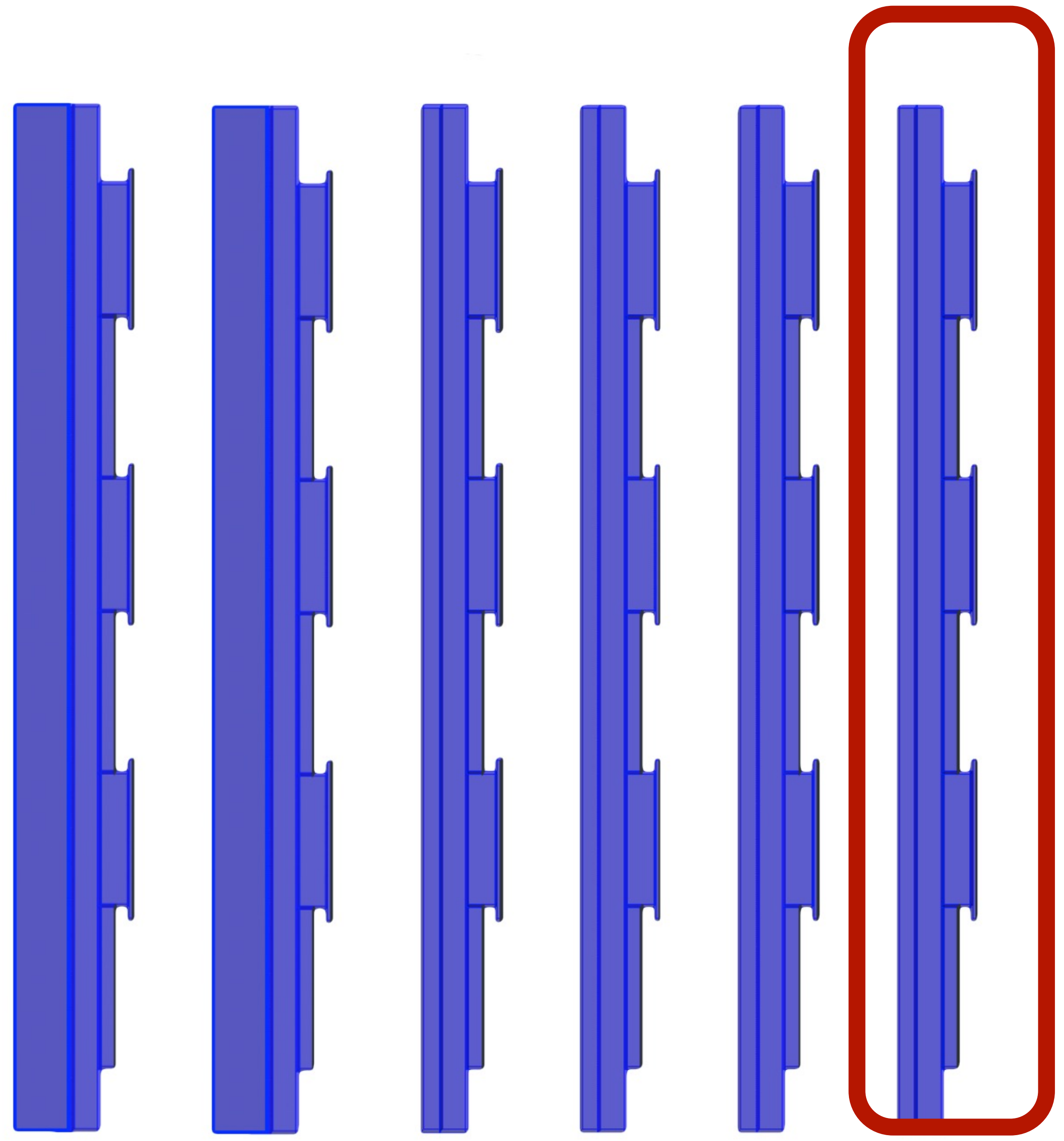

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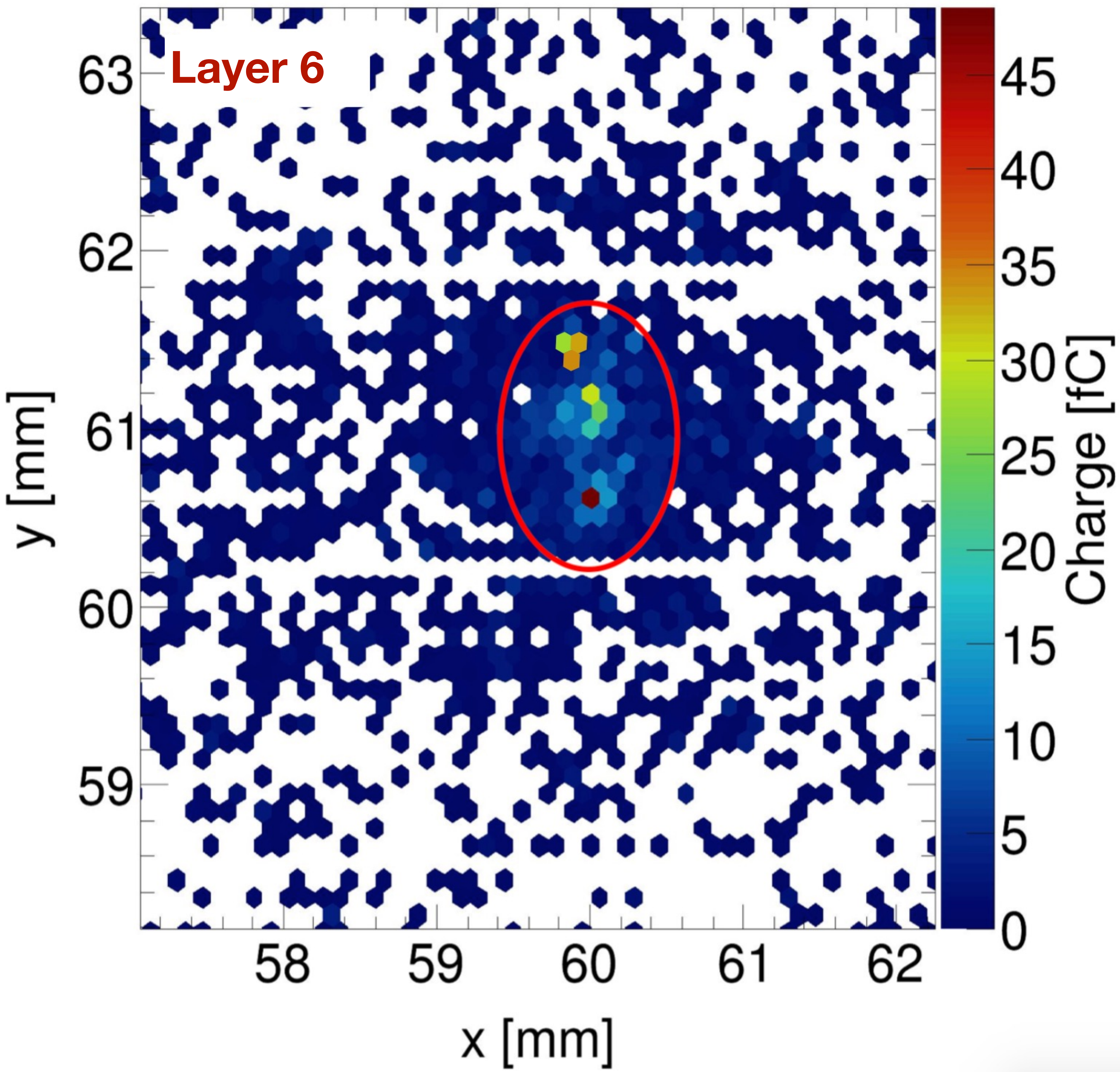

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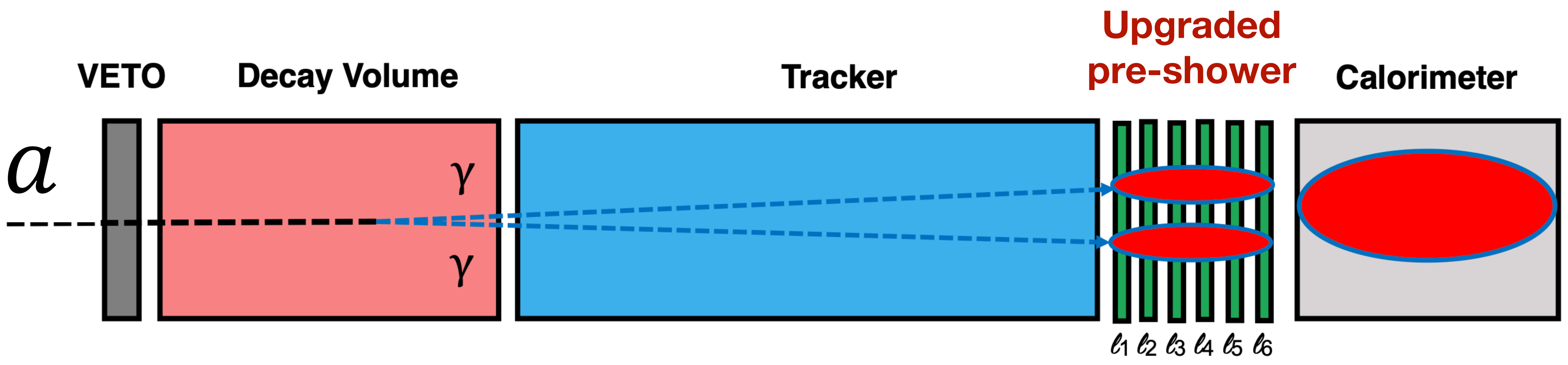

ap²
allpix squared

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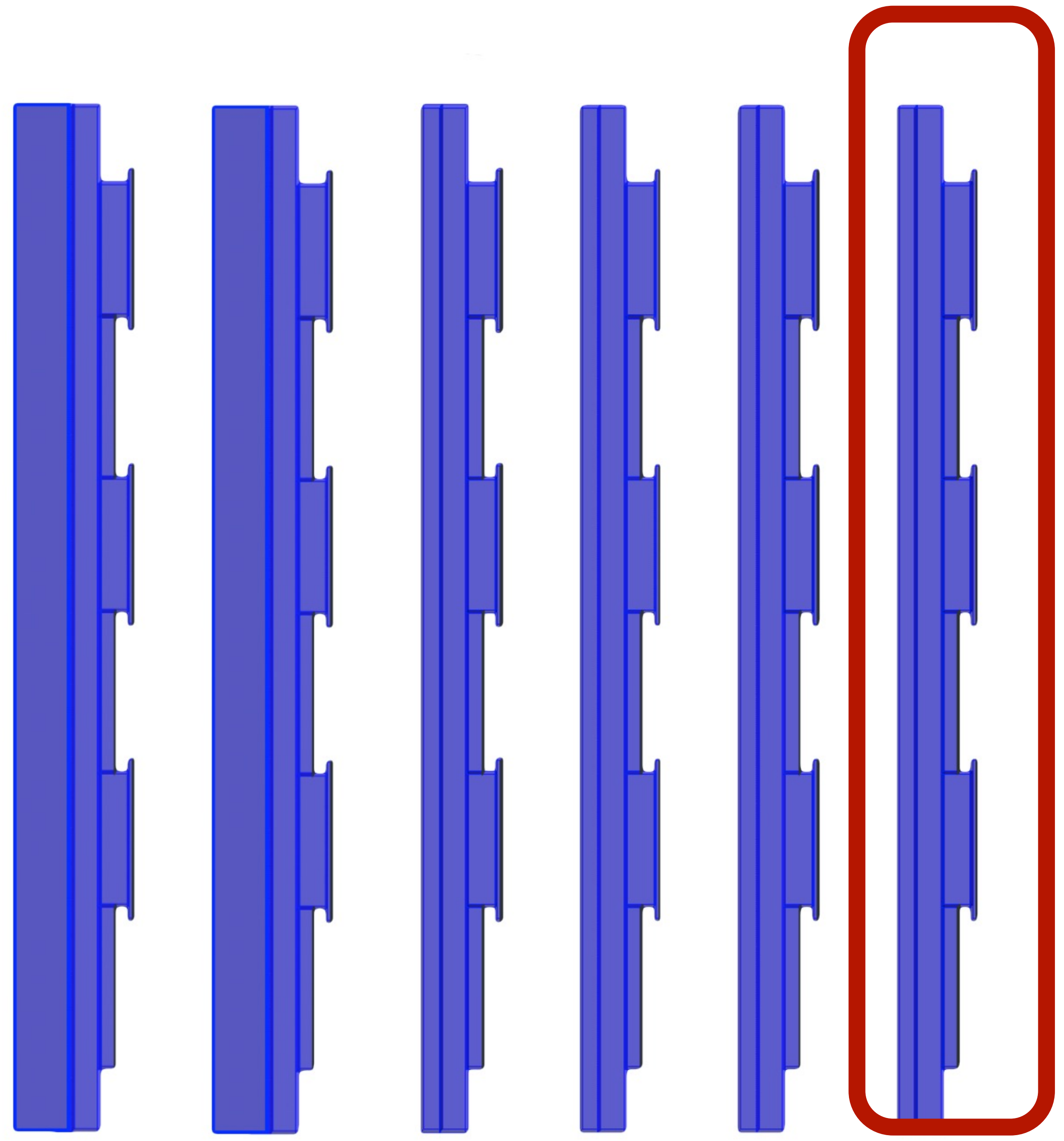
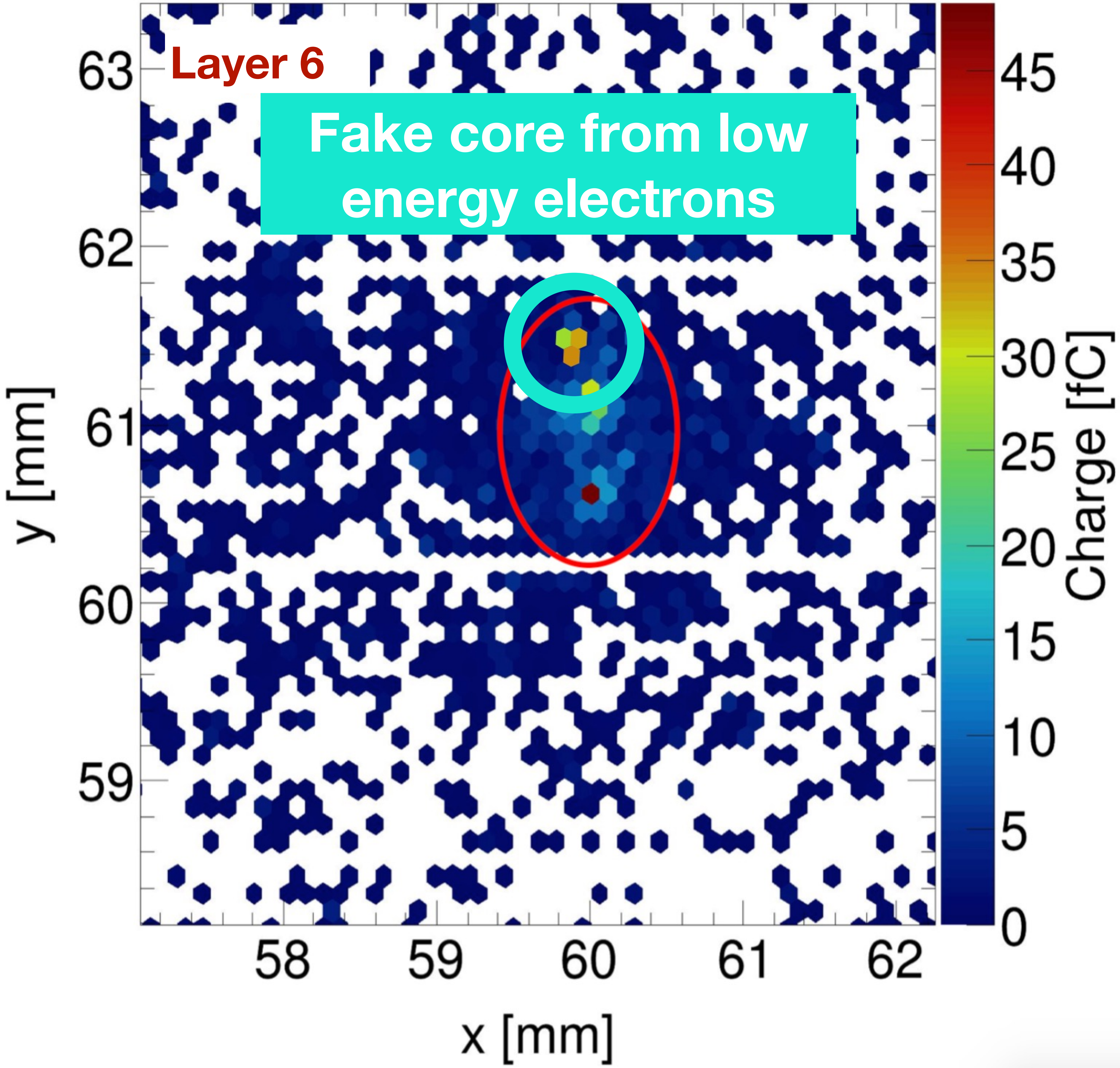
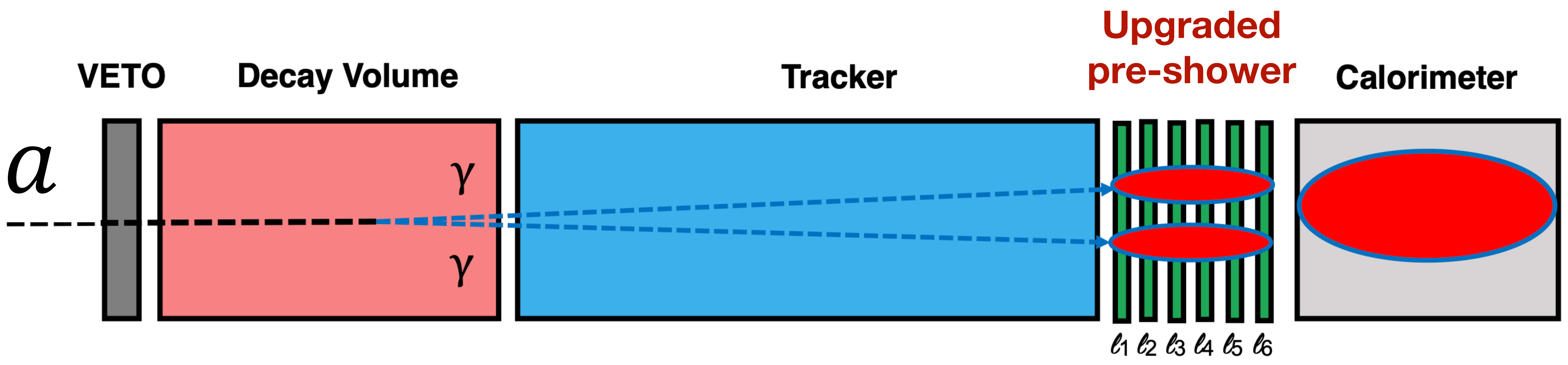




Preshower simulation: Di-photon signature

Very large occupancy

High dynamic range for charge measurement



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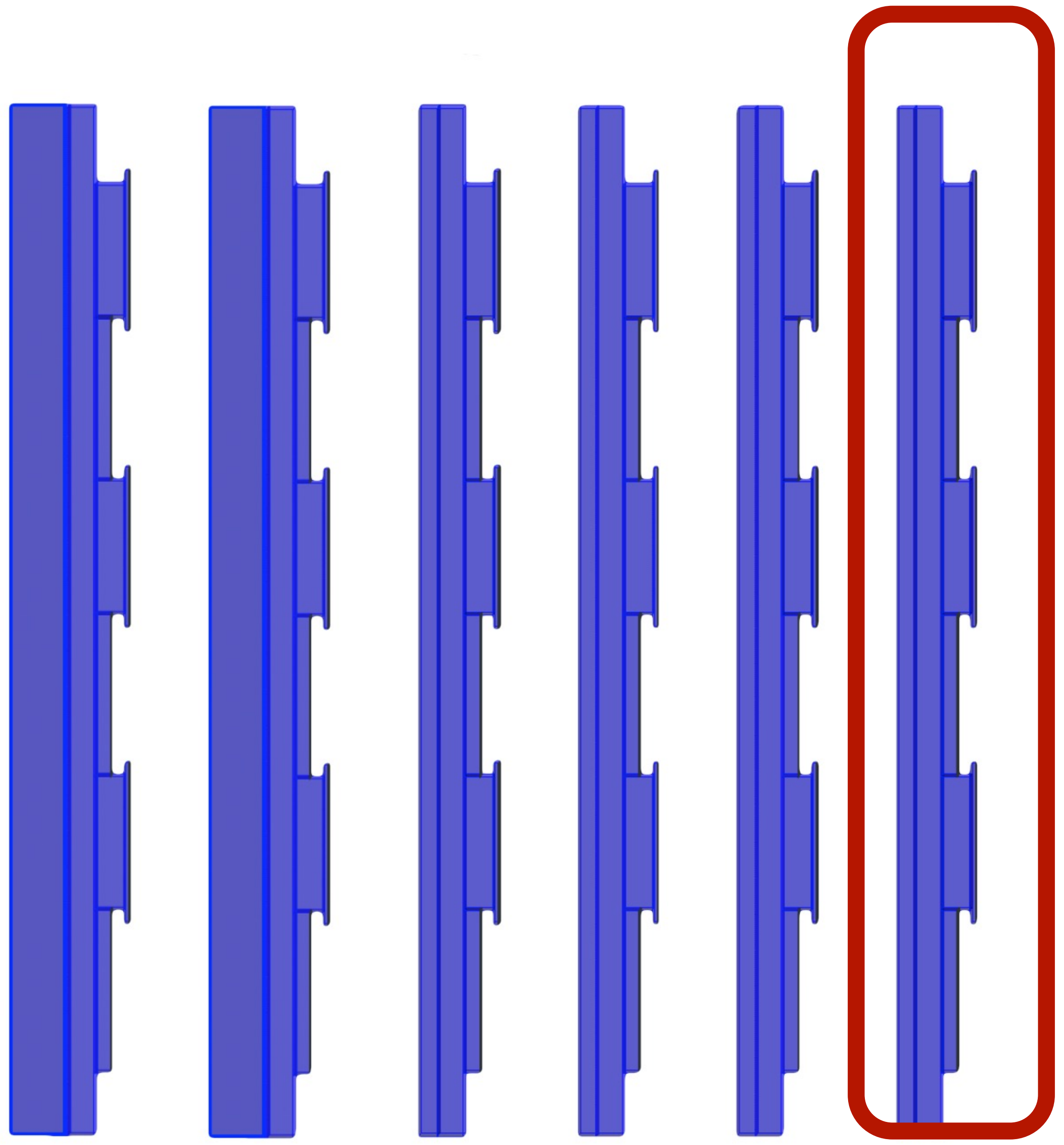
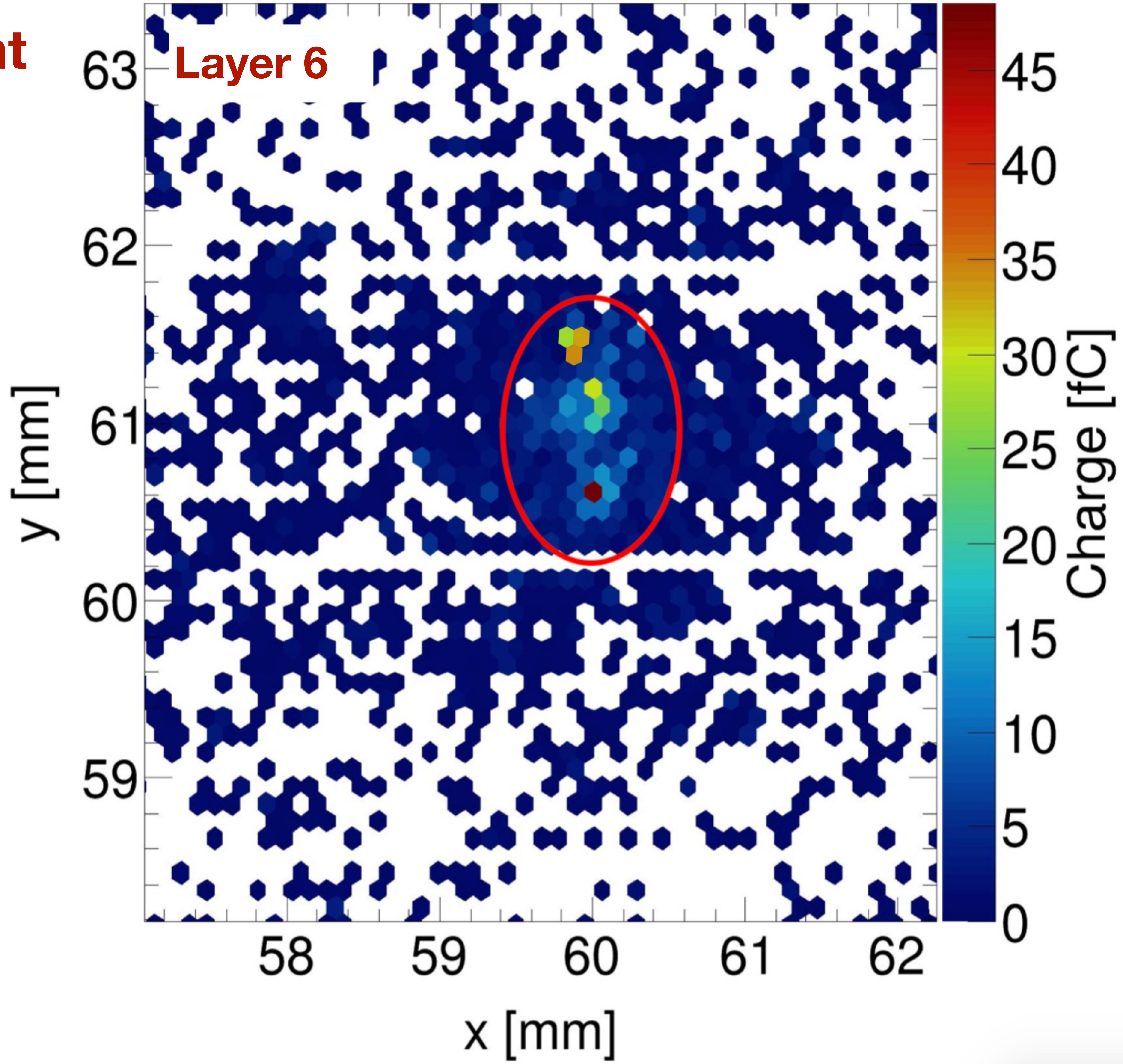
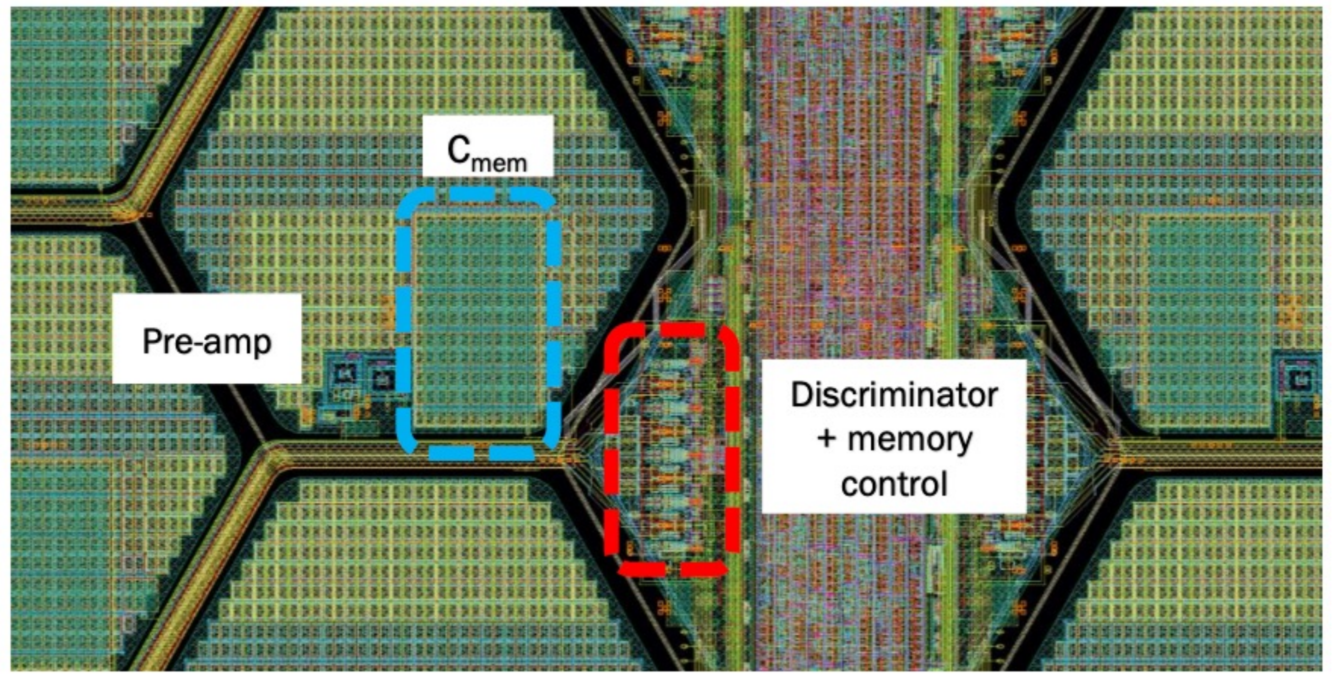




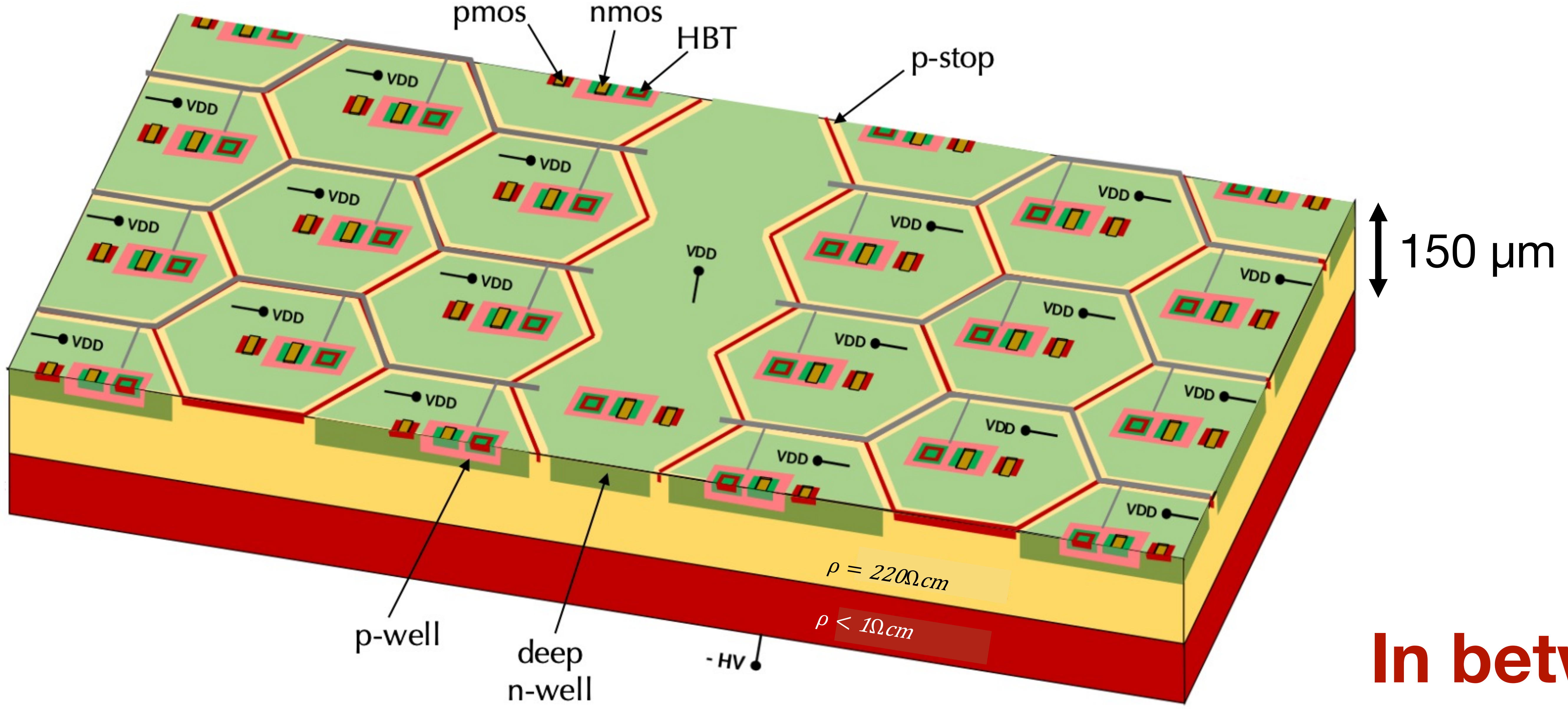
ASIC characteristics

Monolithic active pixel sensor

130 nm SiGe BiCMOS technology (SG13G2 by IHP microelectronics).



- ➡️ **High dynamic range** for charge measurement (0.5 to 65 fC).
- ➡️ **Ultra fast readout** with no digital memory on chip (minimise dead area).
- ➡️ **Local analog memories** to store the charge in pixel.



Main specifications	
Pixel size	65 µm side (hexagonal)
Pixel dynamic range	0.5 to 65 fC
Cluster size	O(1000) pixels
Readout time	< 200 µs
Power consumption	< 150 mW/cm^2
Time resolution	< 300 ps

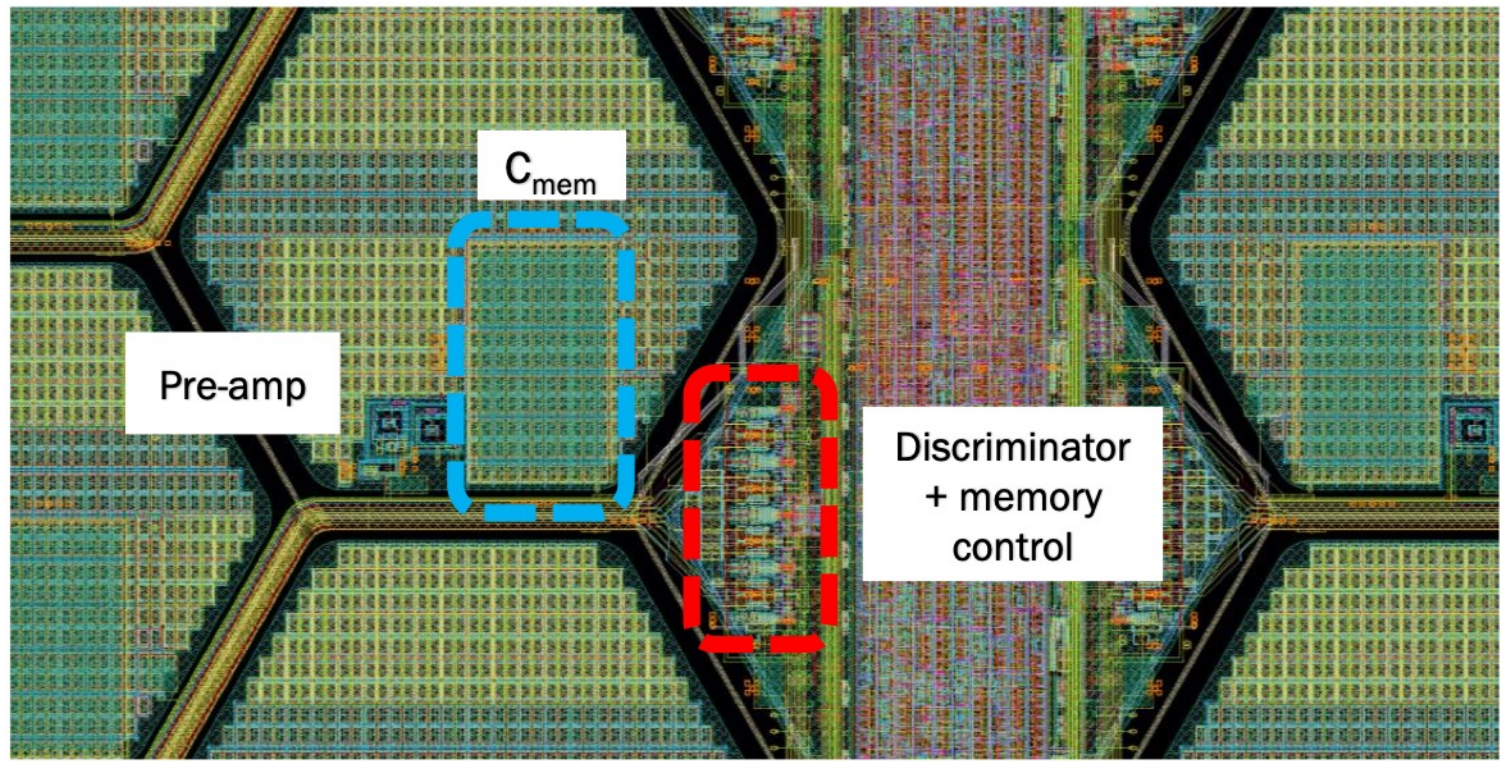
In between imaging chip and HEP detector

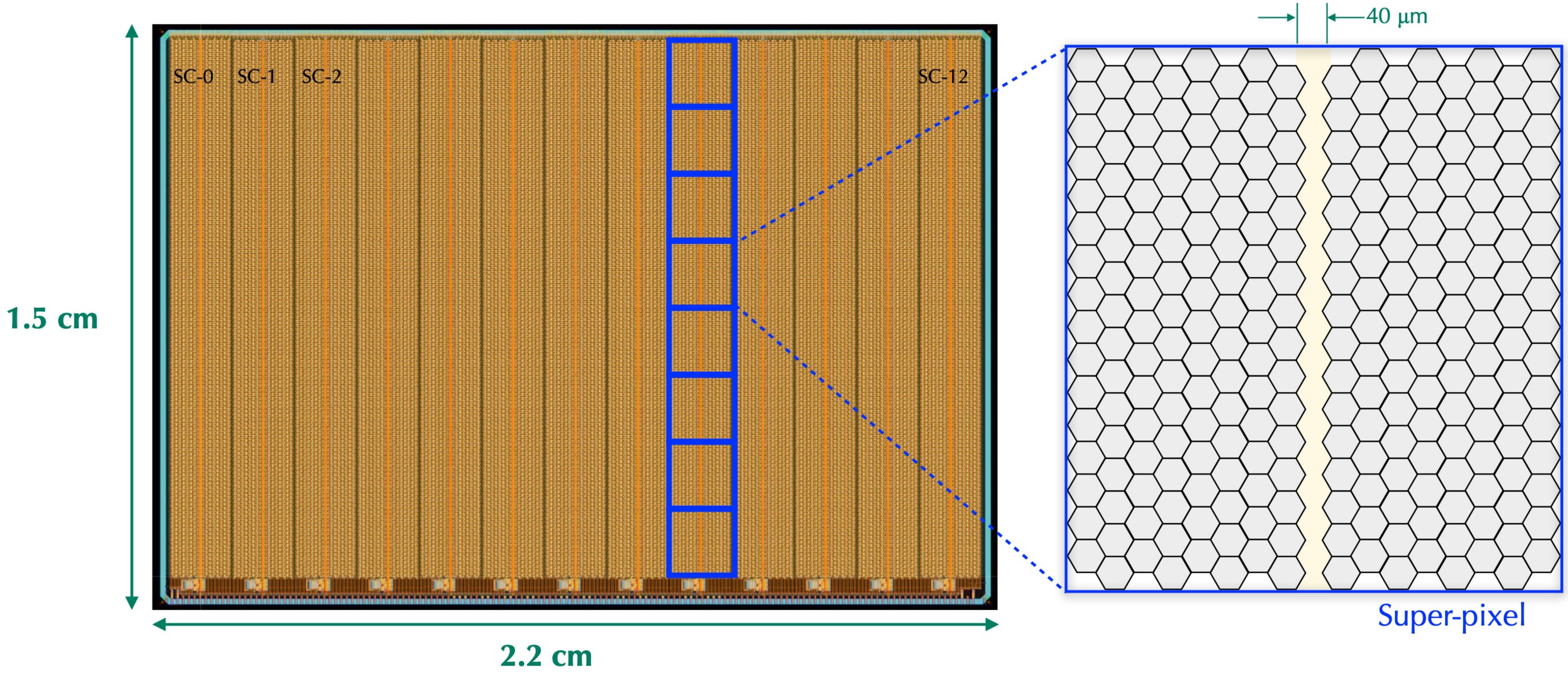
ASIC characteristics: Chip Structure

Chip organized in 13 *super-columns*, each with:

- ➡️ active region, subdivided into 8 *super-pixels* of 16x16 pixel each
- ➡️ digital column (40 µm) in the middle: masking and readout

Digital periphery on the bottom, and multiple guard-ring structure





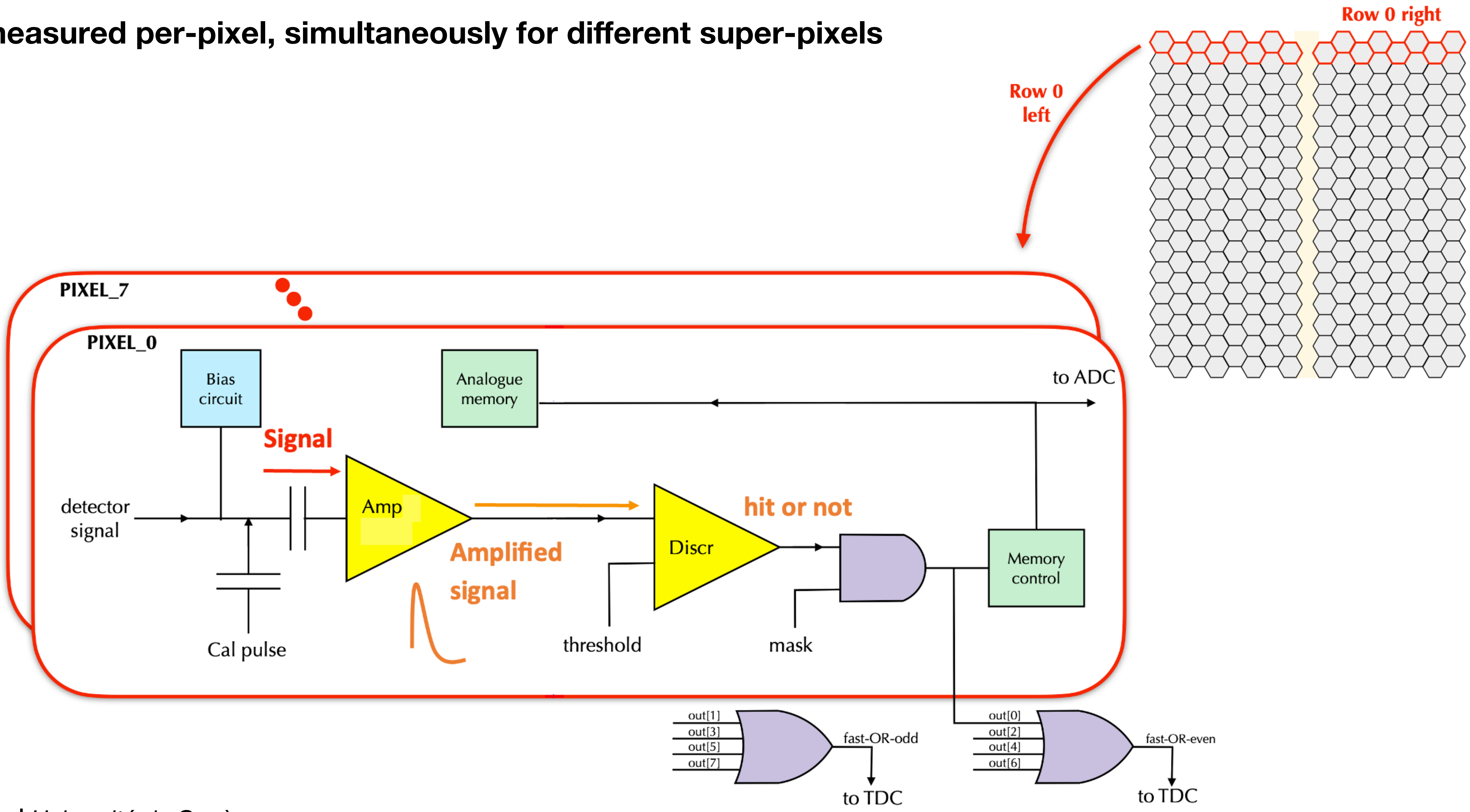
Super pixel :

- ↪16 rows of 8+8 pixels
- ↪ analog multiplexer
- ↪ 4-bit flash ADC
- ↪ 3 fast-OR lines
- ↪ programming logic to mask pixels

Dead area < 5%

ASIC characteristics: Chip Structure

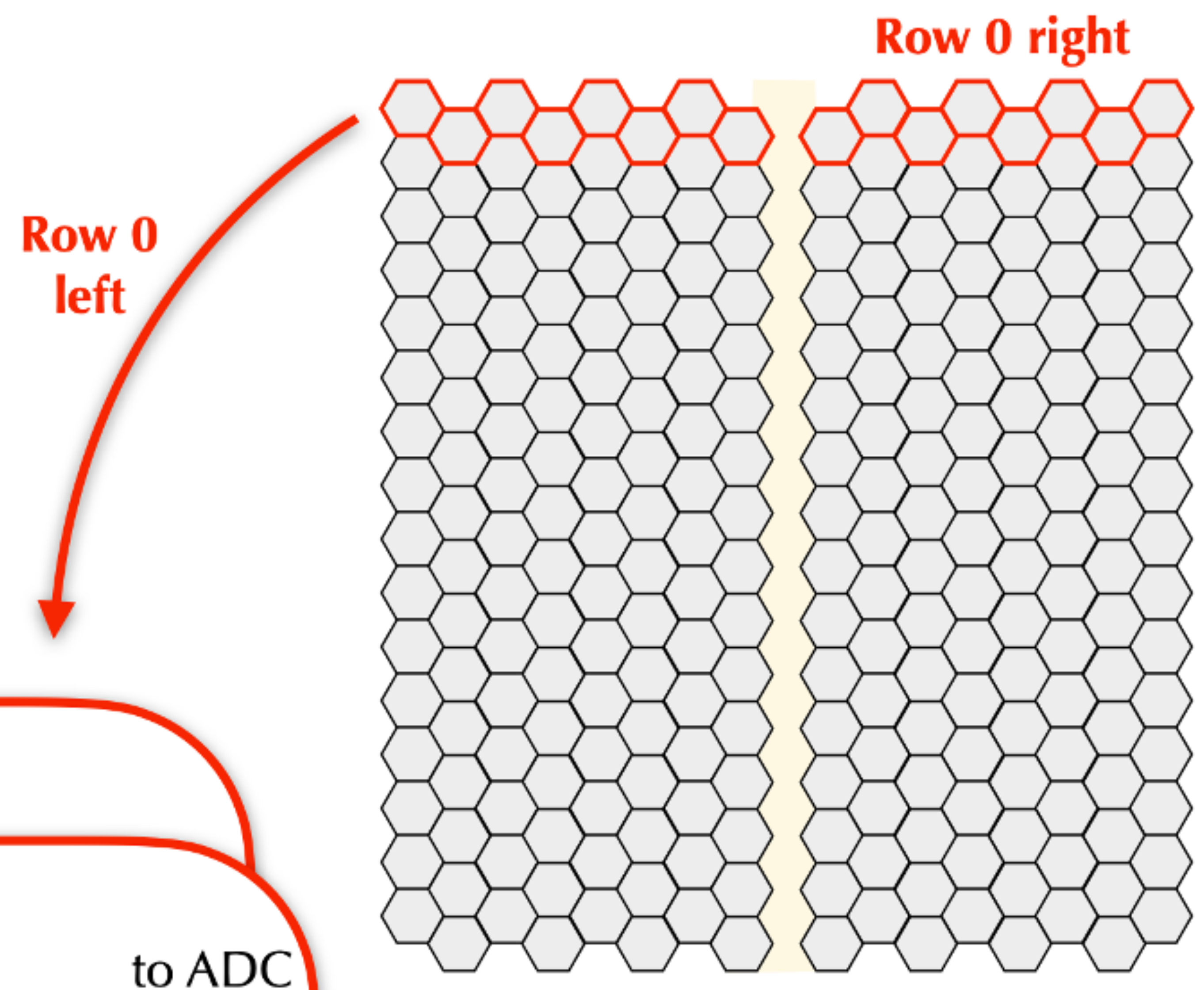
Charge measured per-pixel, simultaneously for different super-pixels

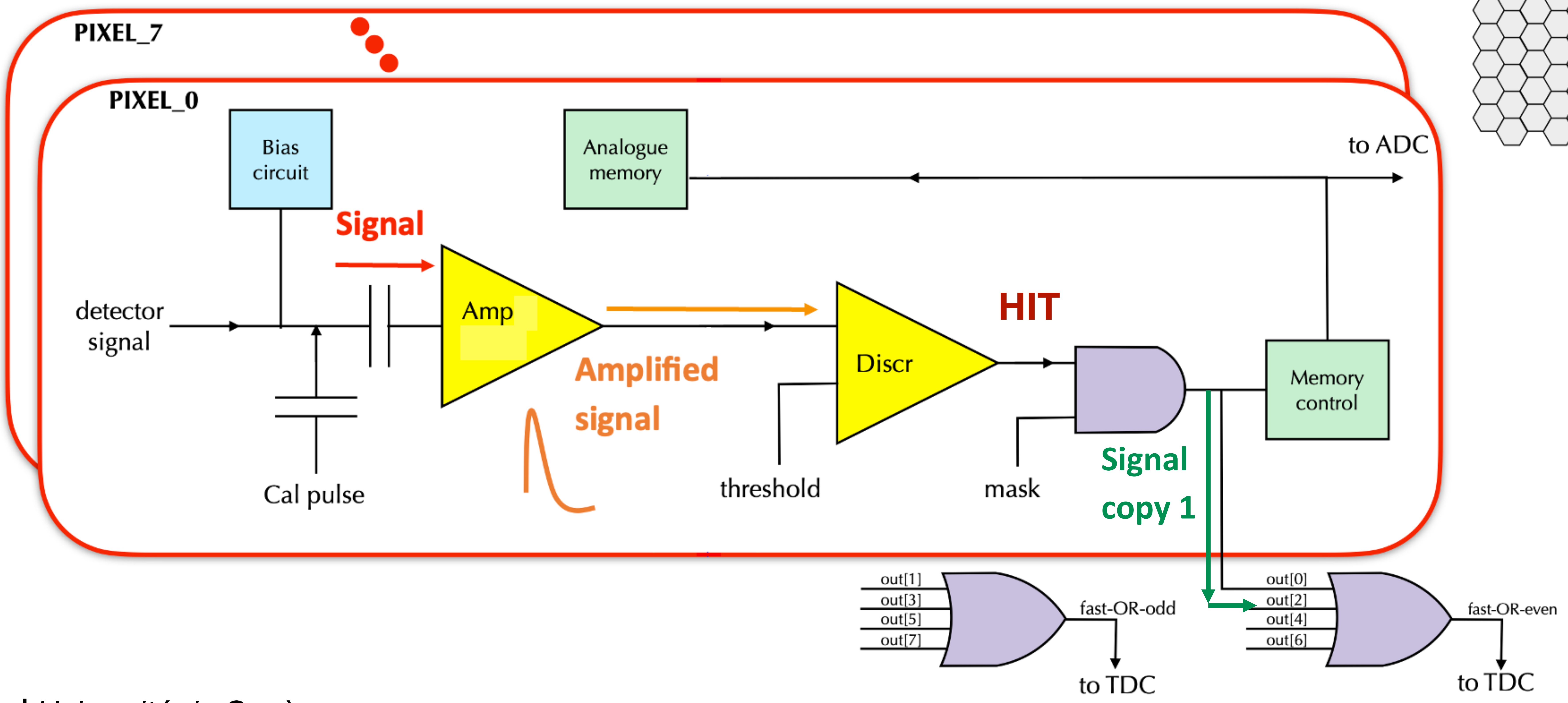


ASIC characteristics: Chip Structure

Charge measured per-pixel, simultaneously for different super-pixels

- Hit above threshold generates signal sent to periphery via fast-OR

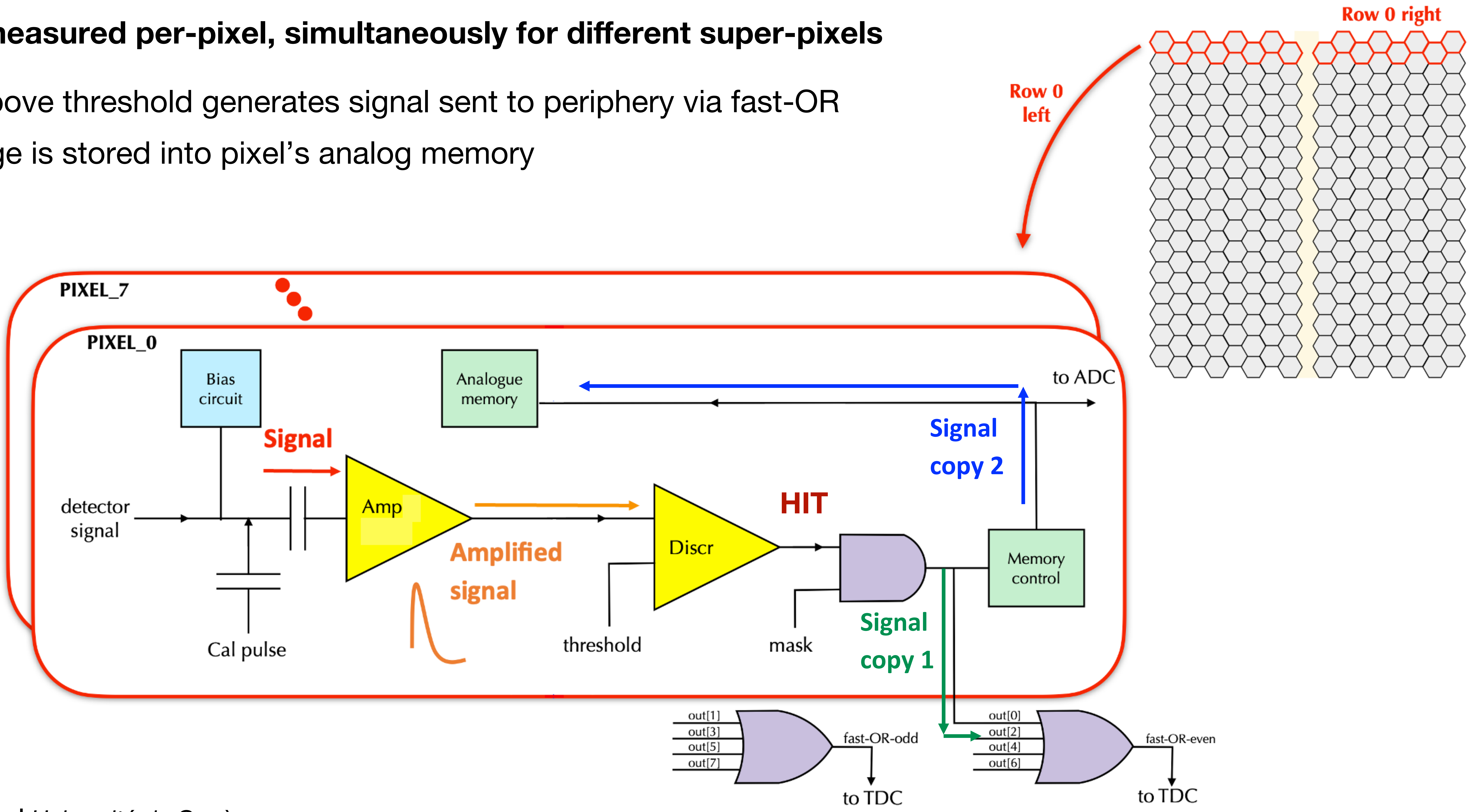




ASIC characteristics: Chip Structure

Charge measured per-pixel, simultaneously for different super-pixels

- Hit above threshold generates signal sent to periphery via fast-OR
- Charge is stored into pixel's analog memory



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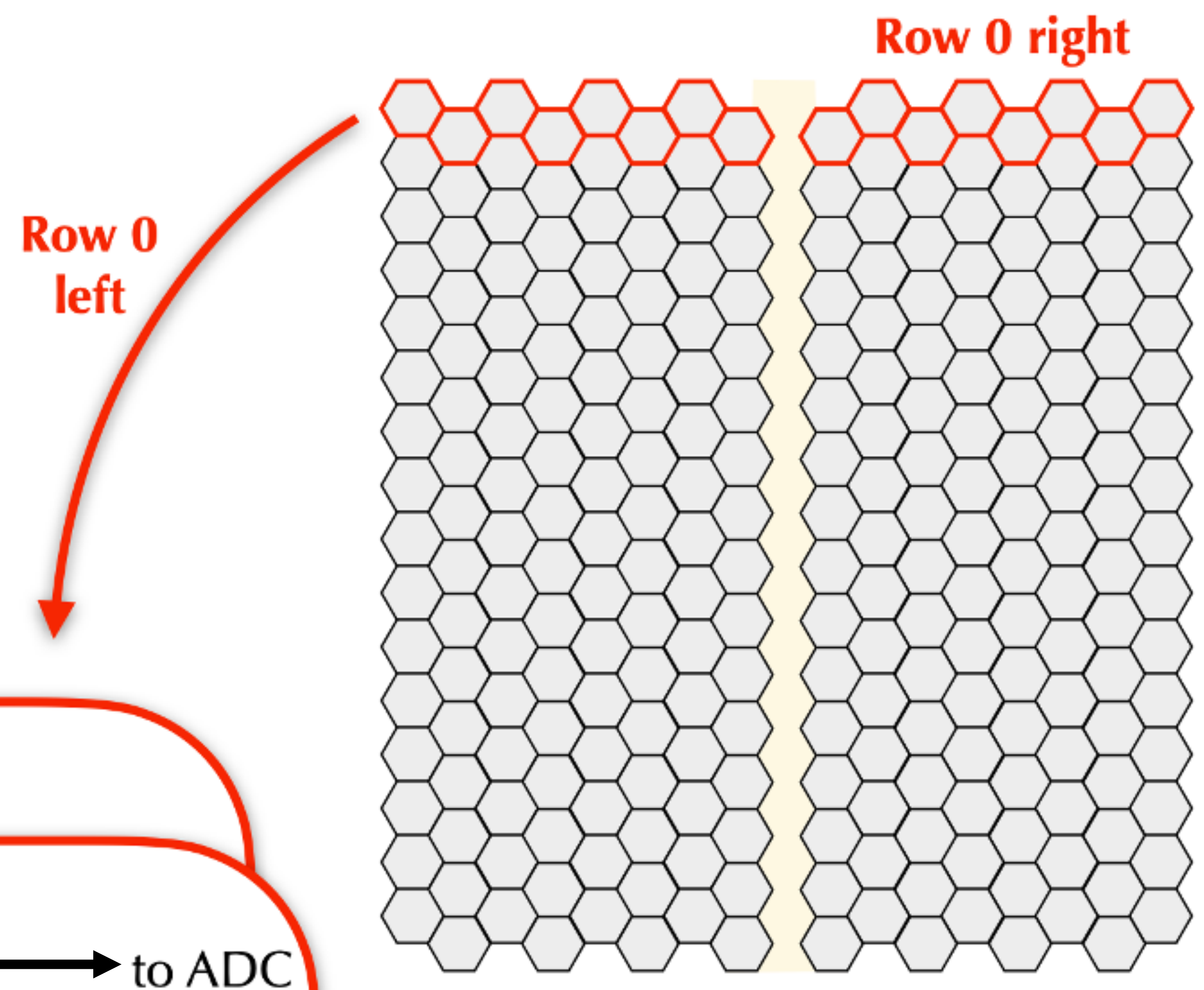
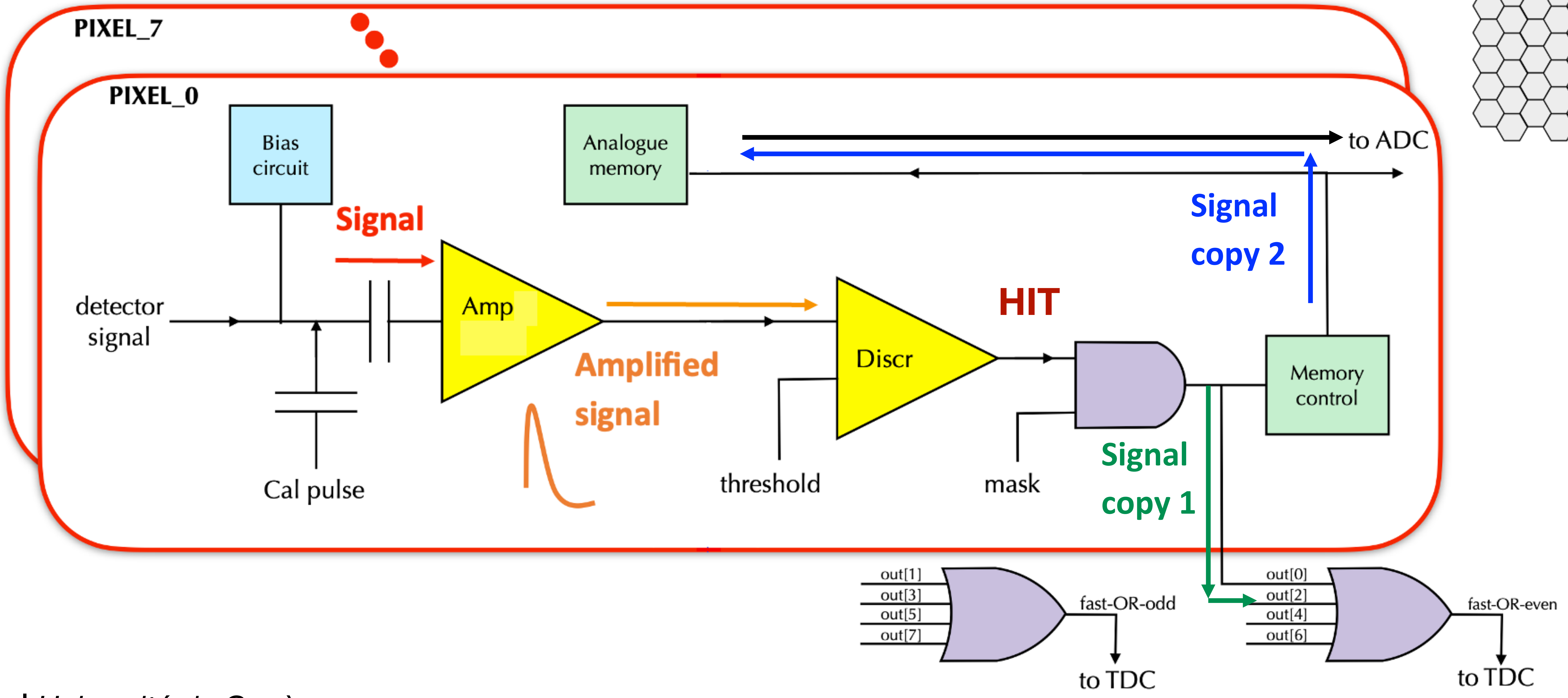
ASIC characteristics: Chip Structure

Charge measured per-pixel, simultaneously for different super-pixels

- Hit above threshold generates signal sent to periphery via fast-OR
- Charge is stored into pixel's analog memory
- After some delay, readout starts super-column after super-column





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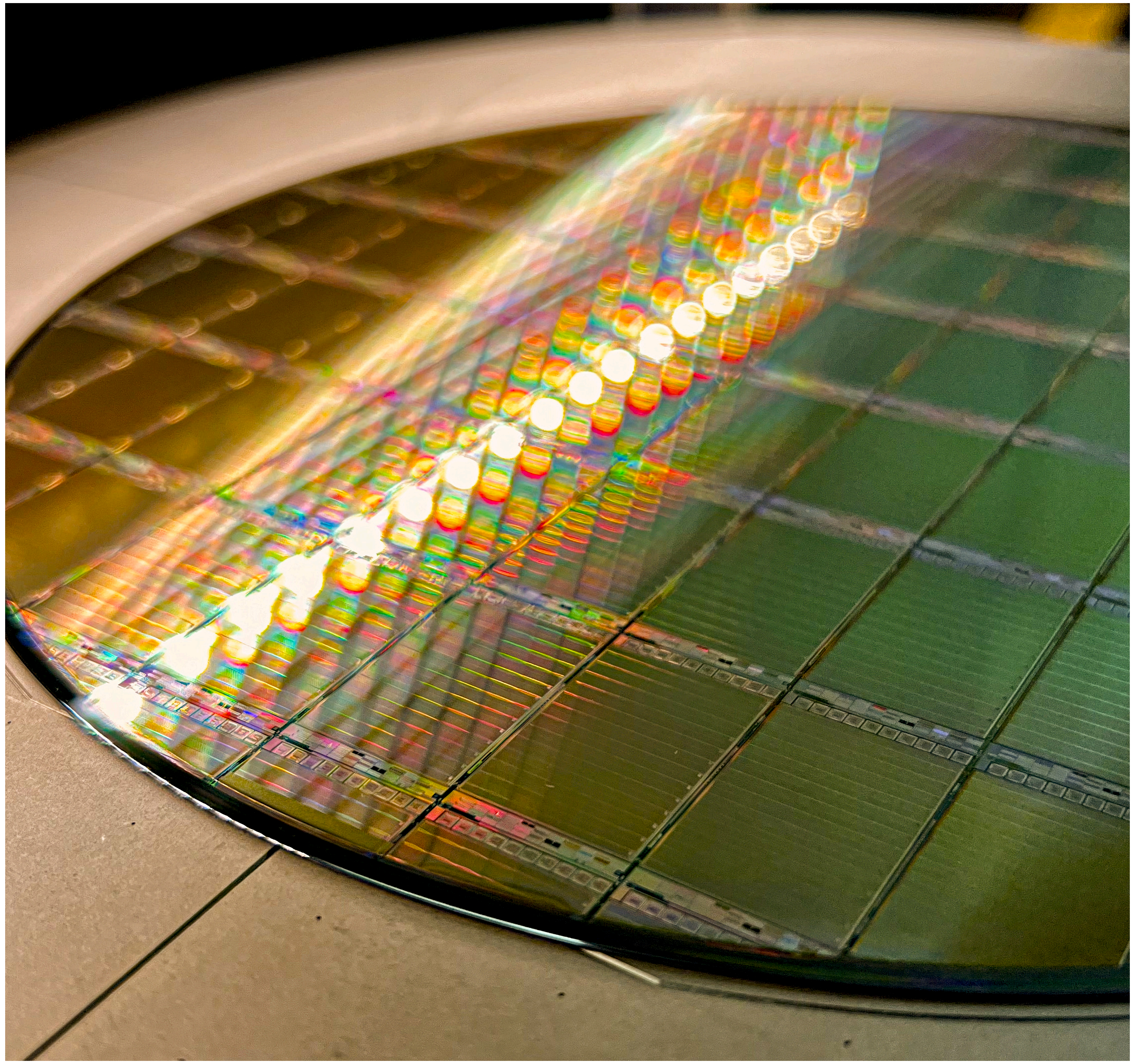
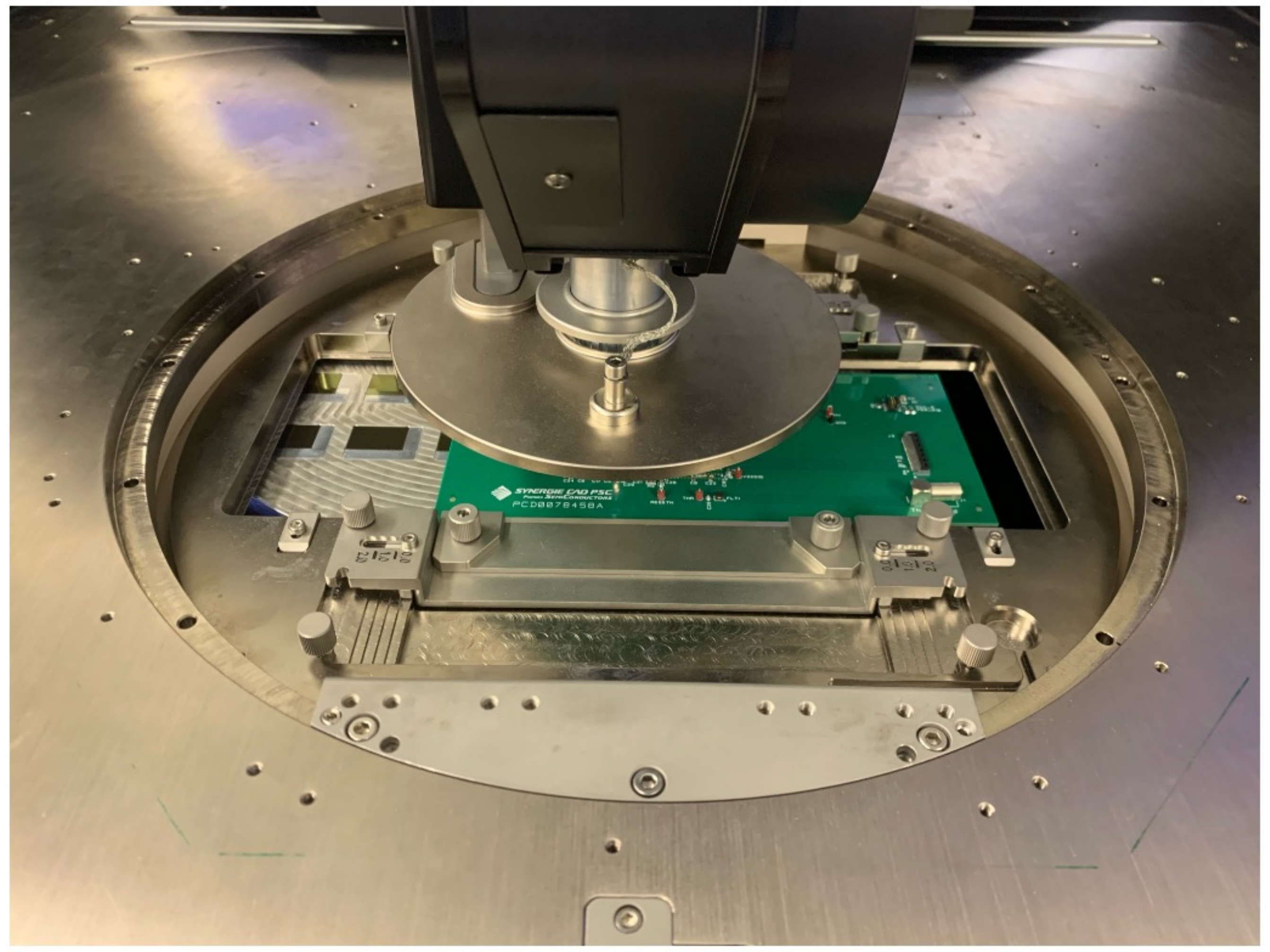
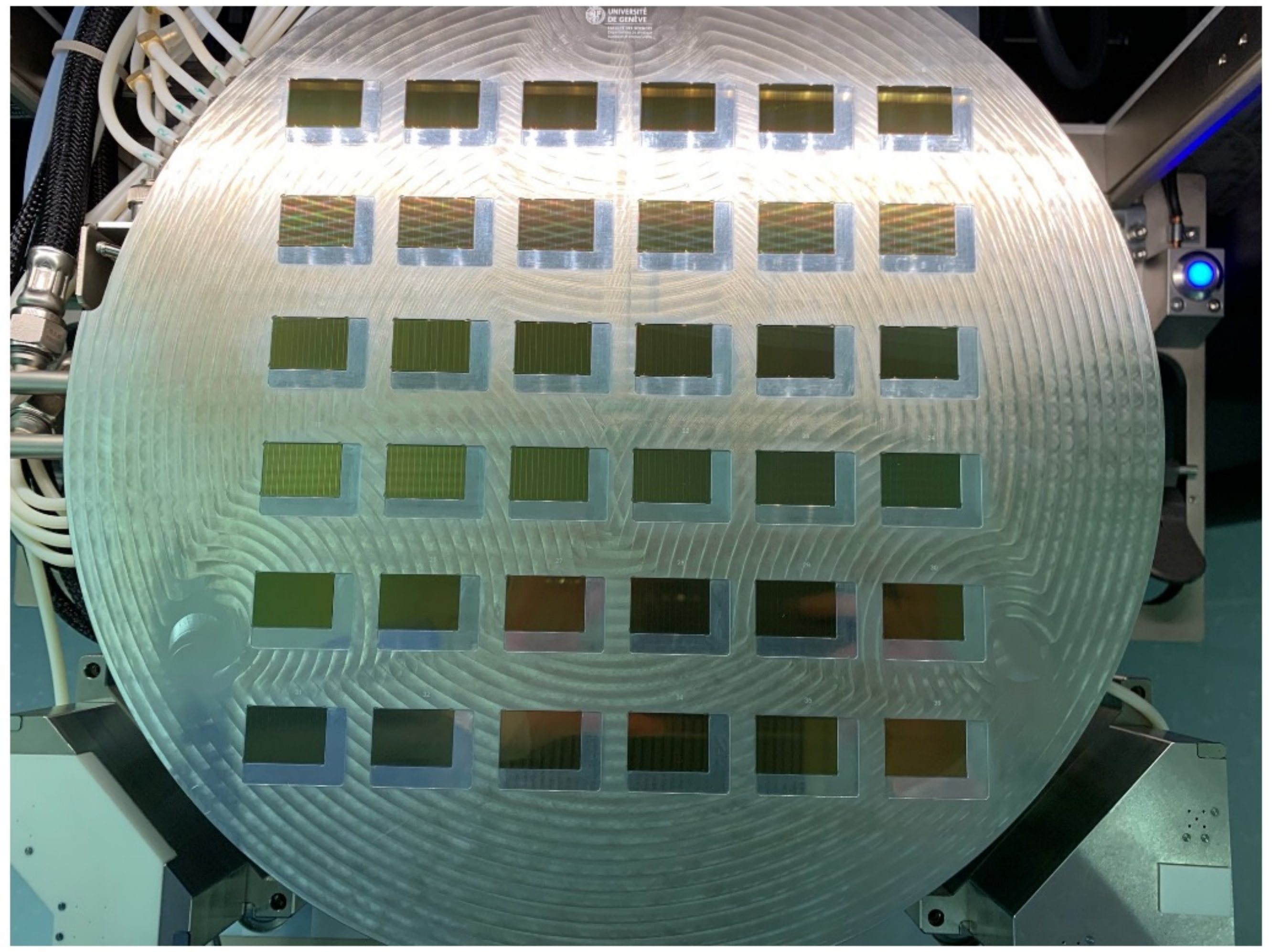
Production ASICs: single chip characterization at probe station



Un-diced wafer



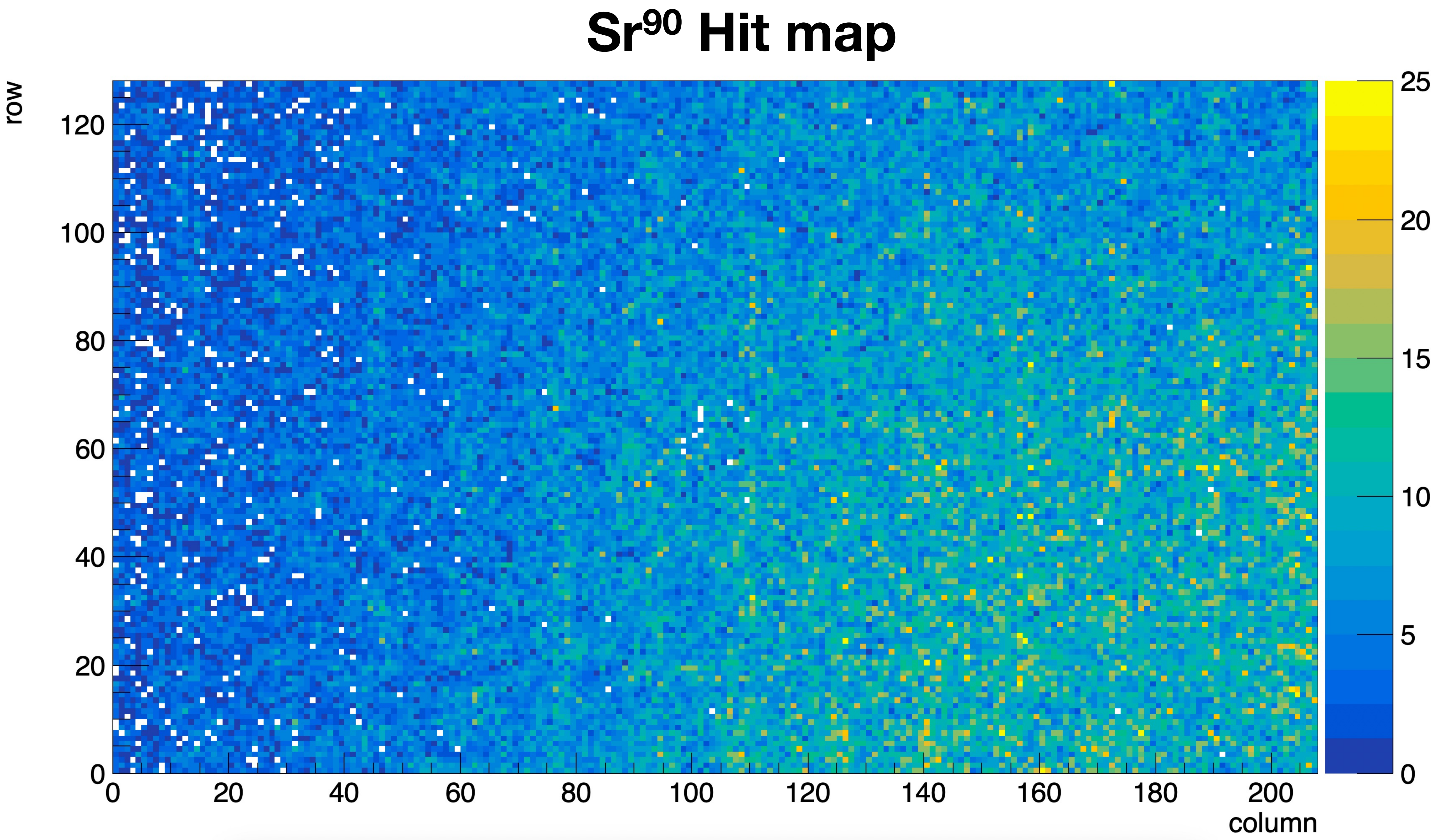
Probe card setup

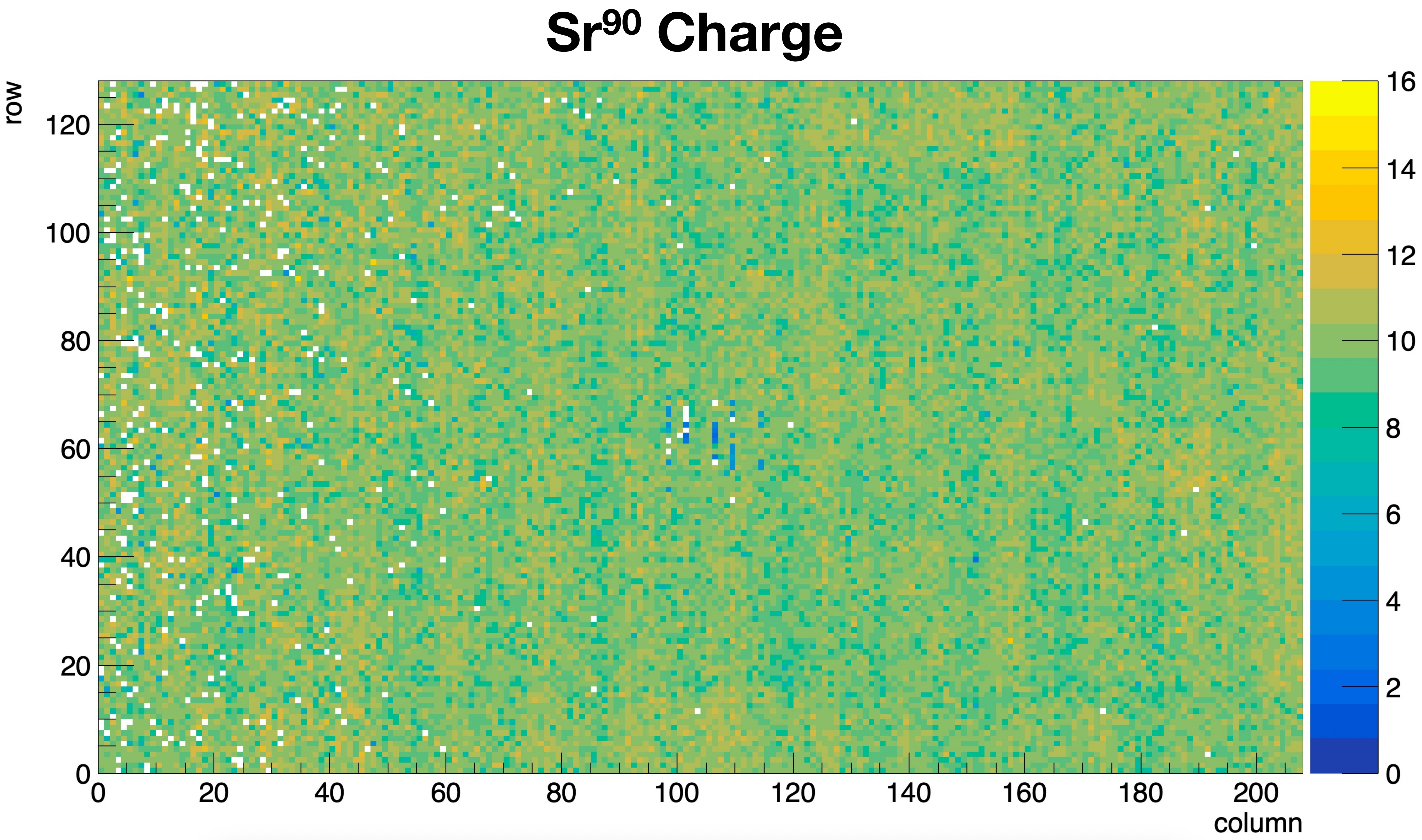


Diced and postprocessed chips

Production ASIC: further studies on single chip boards

Full ASIC irradiated with β electrons from Sr-90 source
MIP-like particle, charge deposition of ~0.5 fC





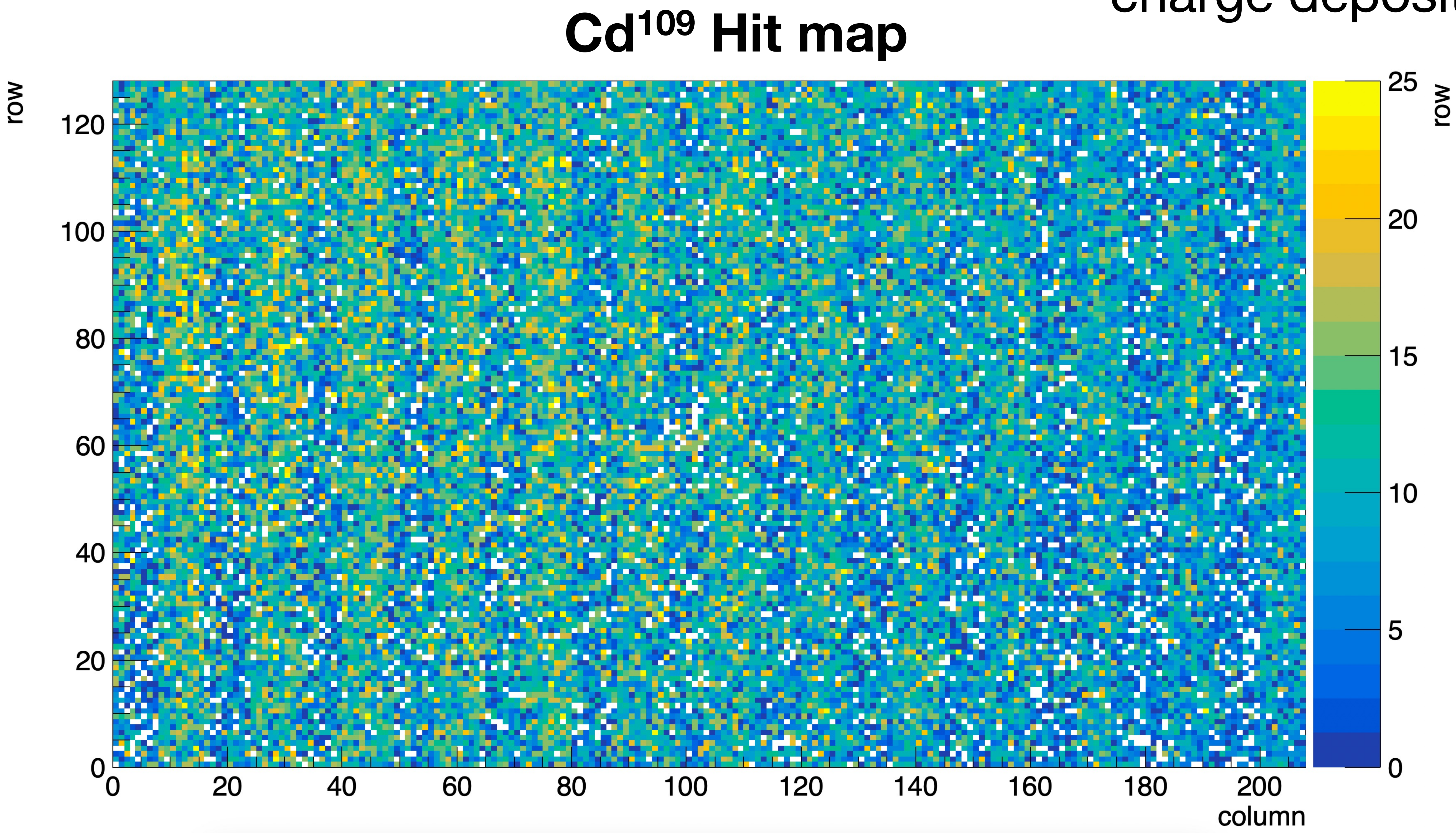
Sensor and readout operating well on the full area

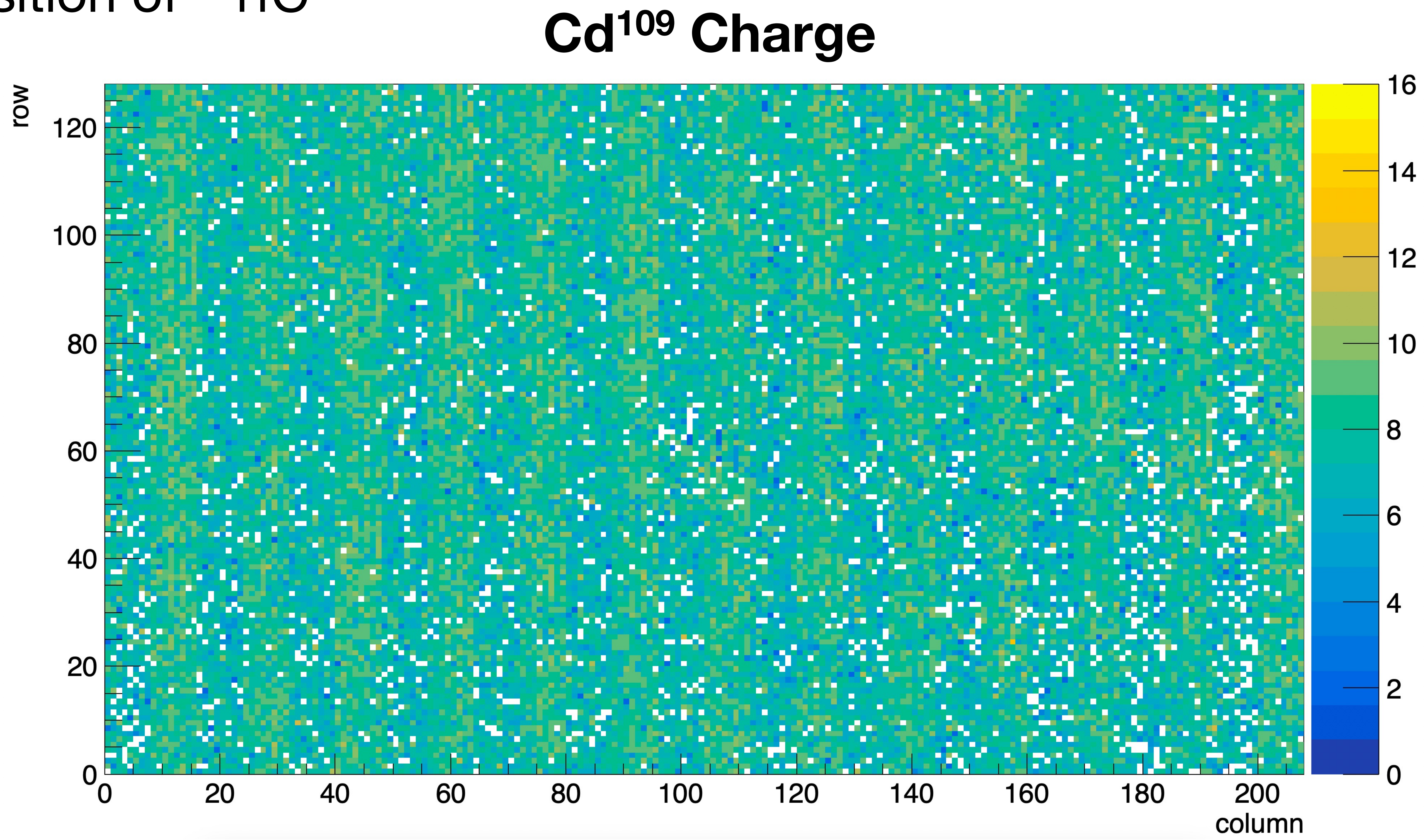
Not calibrated yet

Production ASIC: further studies on single chip boards

Full ASIC irradiated with γ from Cd-109 source

charge deposition of ~1fC



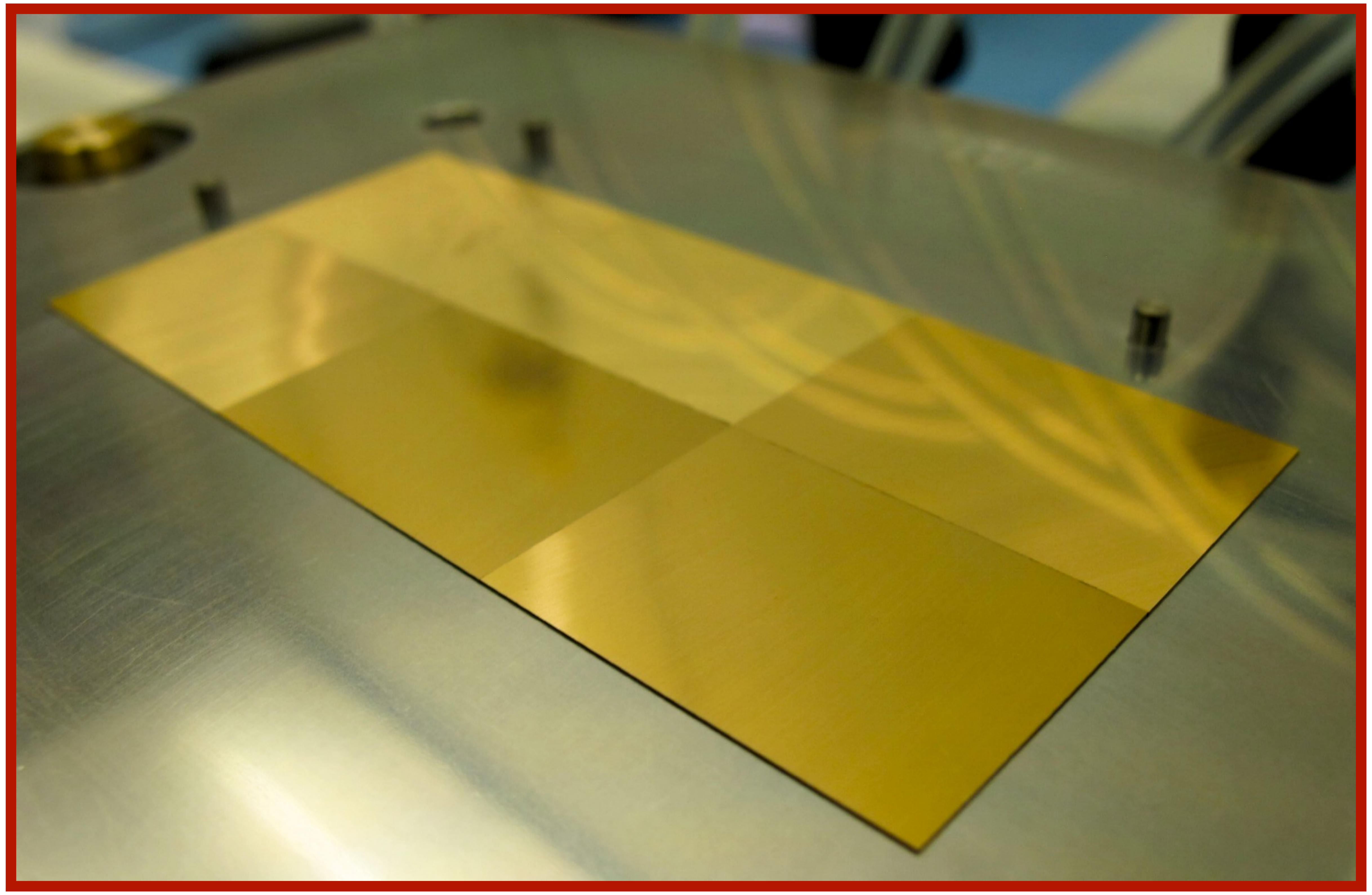


Sensor and readout operating well on the full area

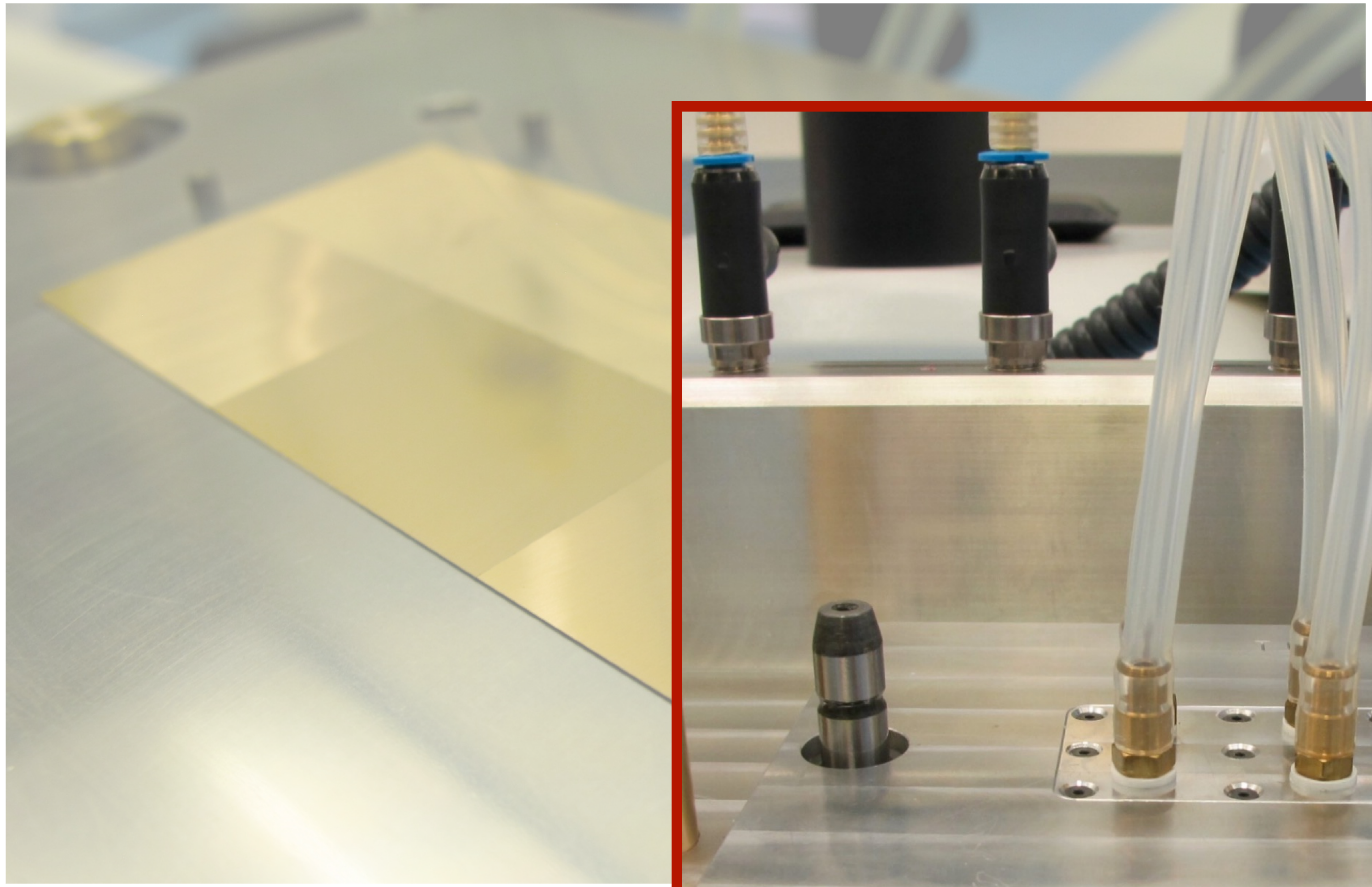
Not calibrated yet

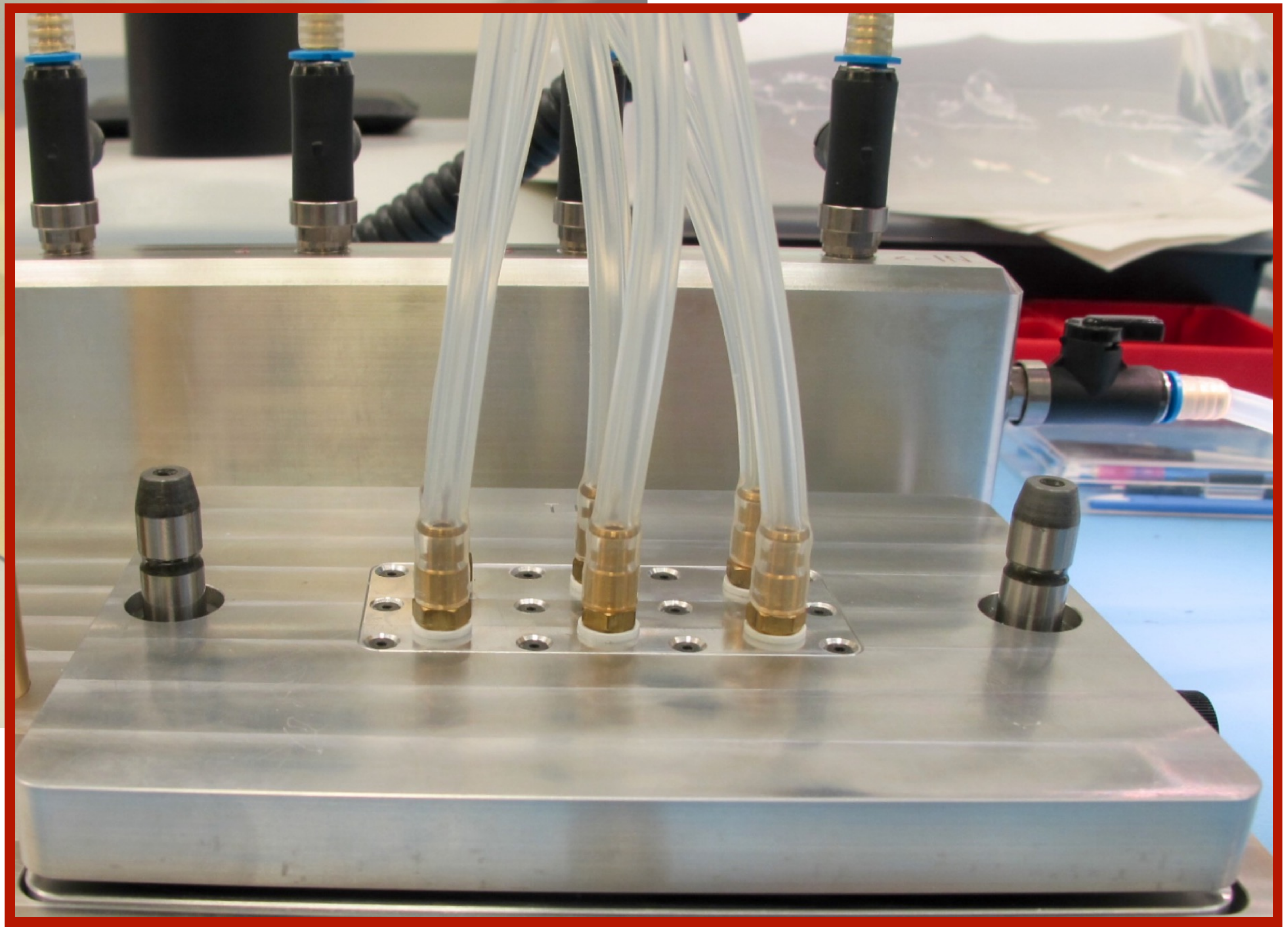
Chip is working well! Now, let's build modules…

Step n°1: aligning the 6 ASICs



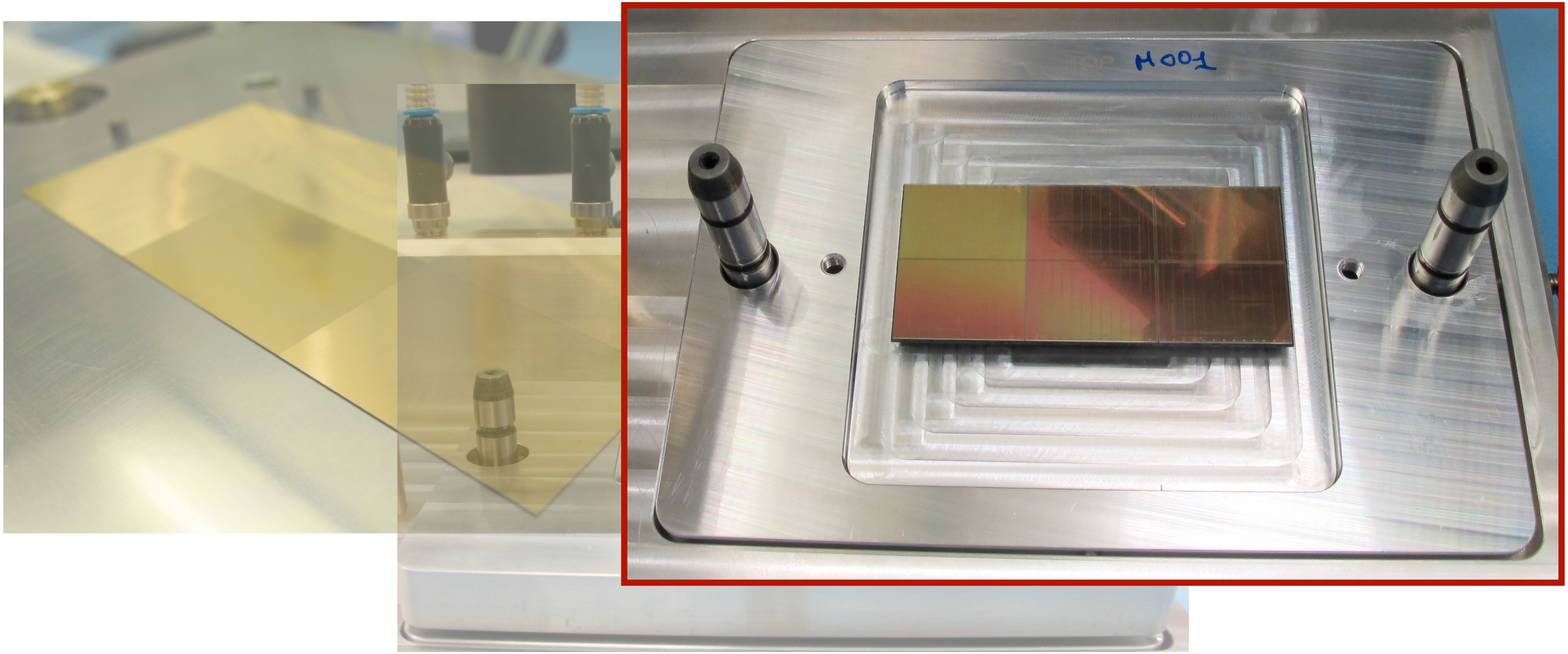
Step n°2: glueing ASICs to back plate



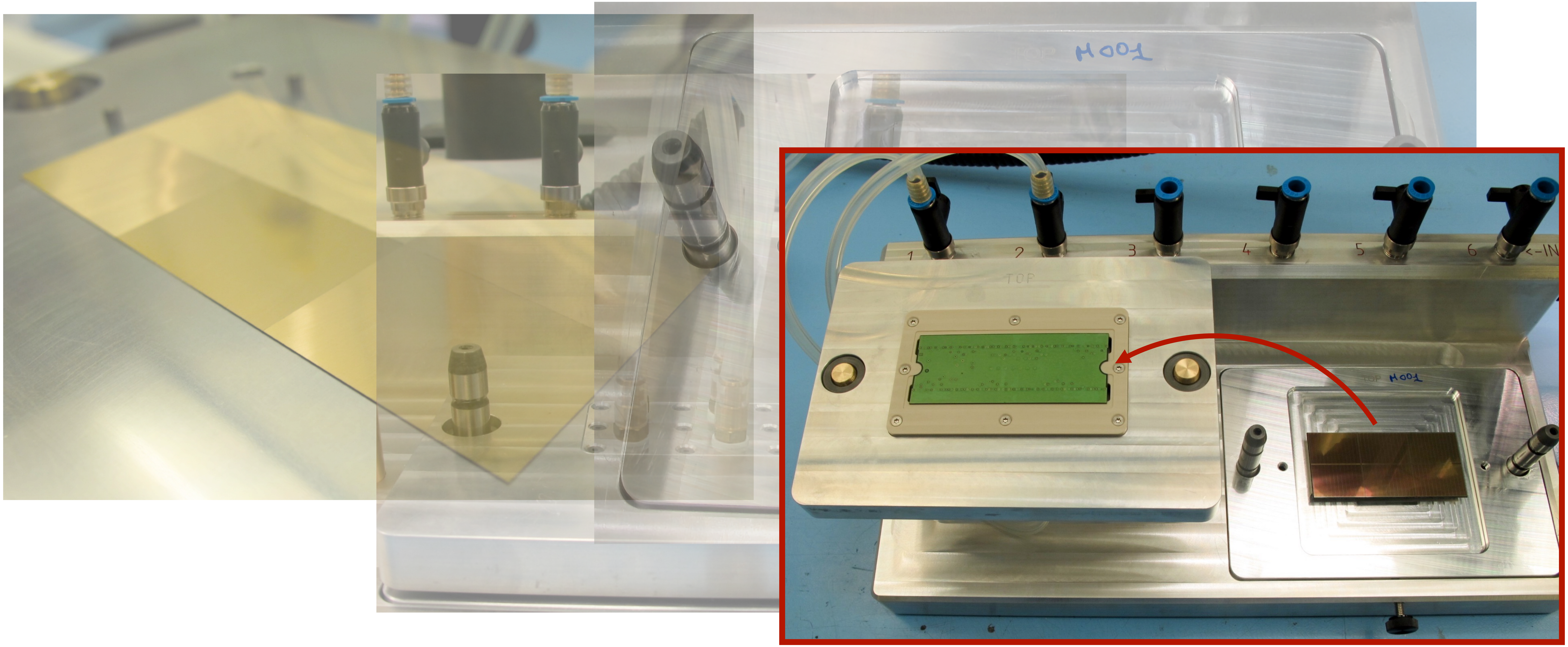


Module assembly

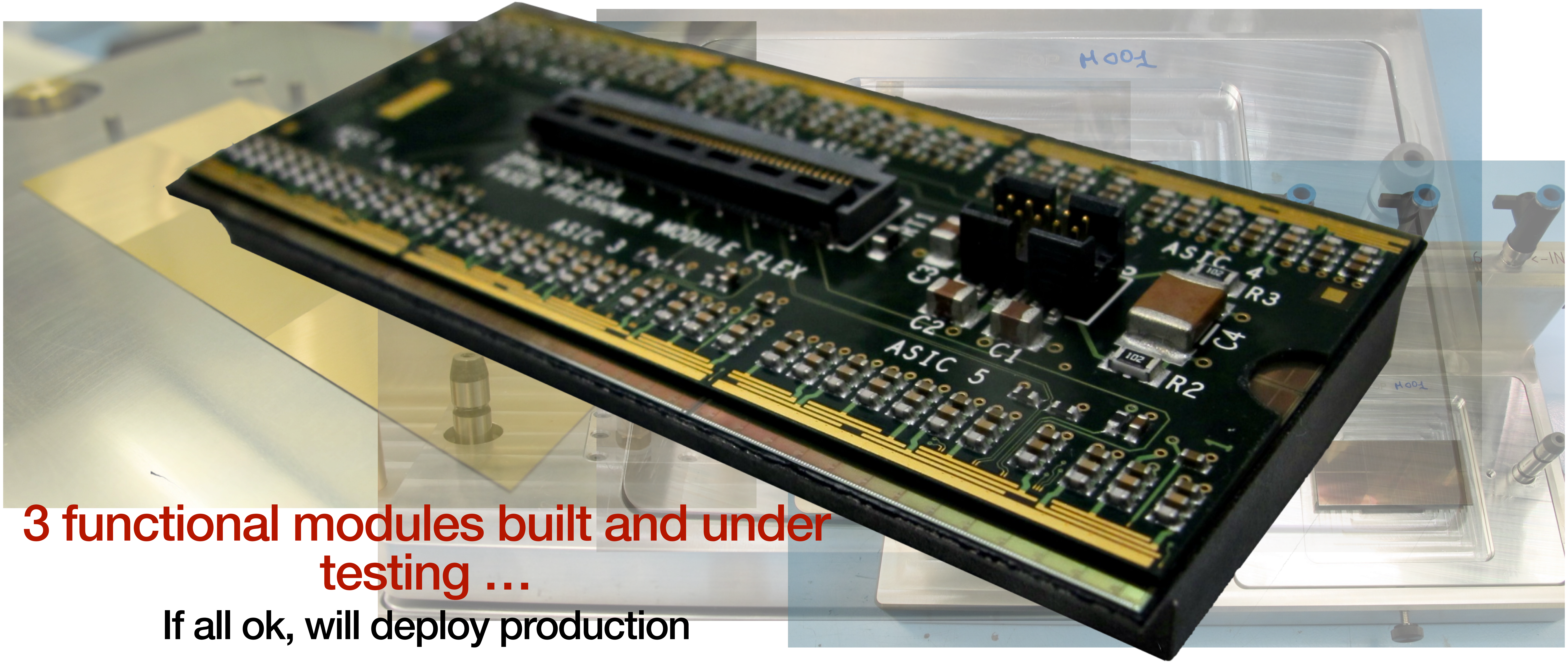
Step n°2: glueing ASICs to back plate



Step n°3: glueing module flex on top of ASICs



Step n°4: build more and make a full plane



3 functional modules built and under testing …

If all ok, will deploy production

Summary & Outlook

- FASER is a small experiment but with good potential of discovery for new physics.
- The new preshower is critical to allow multi-γ tagging and enhance ALPs searches.
- The ASIC, in its third generation, has been produced and meets expectations so far.
  - ↪ Extensive test on-going to assess performance and select chips for module assembly.
  - ↪ Planes will be put in a test beam at CERN in **mid-October 2024** to validate DAQ design and measurement of tracking performance.
- Targeted installation: **December 2024**

Lots of work ongoing: exciting times ahead of us!

FASER collaboration

101 collaborators, 27 institutions, 11 countries

CERN

UNIVERSITÉ DE GENÈVE

KYUSHU UNIVERSITY

UC IRVINE

UNIVERSITÄT BERN

Technion
Israel Institute of Technology

NAGOYA UNIVERSITY

UNIVERSITY of WASHINGTON

JOHANNES GUTENBERG UNIVERSITÄT MAINZ

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WEIZMANN INSTITUTE OF SCIENCE

KEK

UNIVERSITY OF OREGON

DESY.

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Thank you for your attention!