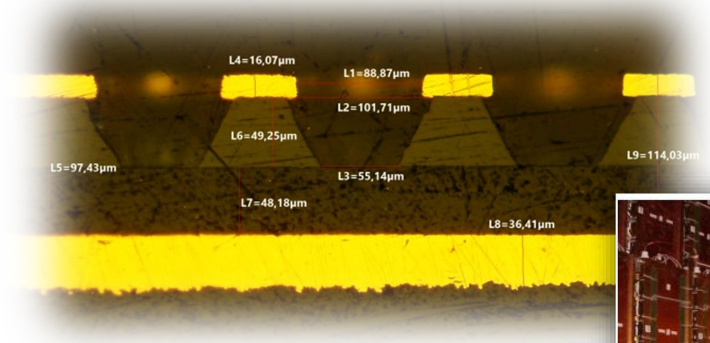
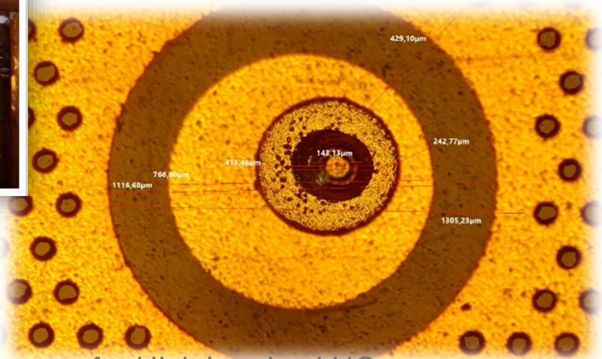
LHCb Muon Detector for the High Lumi at LHC





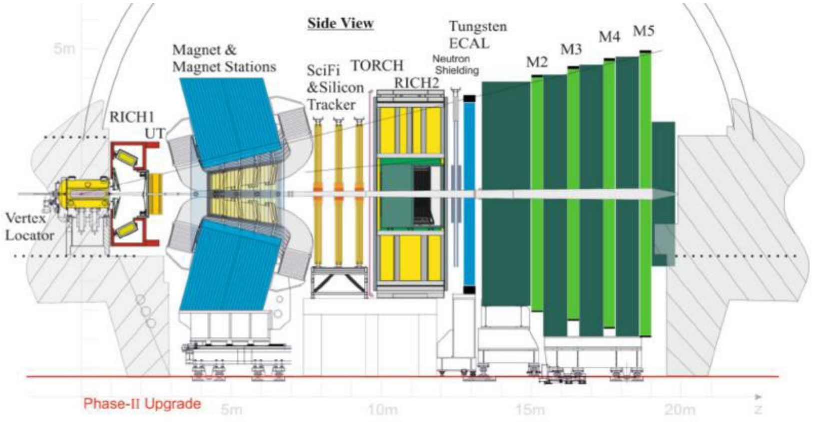
Marco Poli Lener
on behalf of the
LHCb Collaboration

INFN LNF - DDG

Outline

The Muon Apparatus design

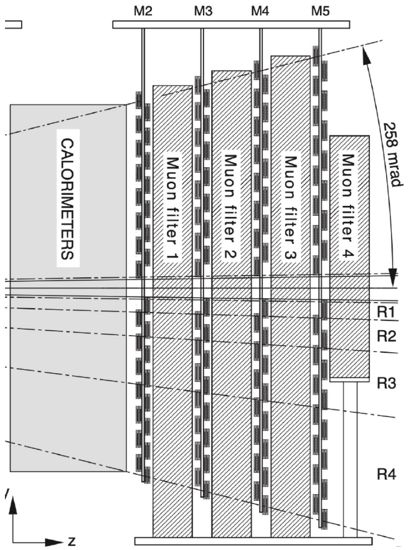
Detector design for the Upgrade phase II (U2)
- **Challenges**
- **Technological solutions**
  - The micro-ResitiveWELL detectors
  - New Front-End Electronics architecture
  - New improved Shielding



Transfer technology to the industry of the detector manufacturing process

Summary & Outlook

Muon system at U2 (as in fTDR)



CURRENT APPARATUS: 4 stations, each composed by 4 layers of gas detector (MWPC) OR-ed readout + iron filters

The original detector has been largely reused at U1 (2×10^{33} cm^{-2}s^{-1})

New off detector electronics + remove strips to readout directly pad in few crowed regions to reduce ghosts

The big increase in luminosity at U2 will force in greater changes

MUON system @ U2: define 3 Muon designs with comparable performance wrt the present one targeting at 3 different luminosity (*):

- Baseline_1.5 L=1.5×10^{34} cm^{-2}s^{-1}
- Middle_1.3 L=1.3×10^{34} cm^{-2}s^{-1}
- Middle_1.0 L=1.0×10^{34} cm^{-2}s^{-1}

→ keeping high hit efficiency in each station (MuonID efficiency ~ station efficiency^4)

→ reducing the accidental hit due to the high background rate

*Given a reasonable cost envelope

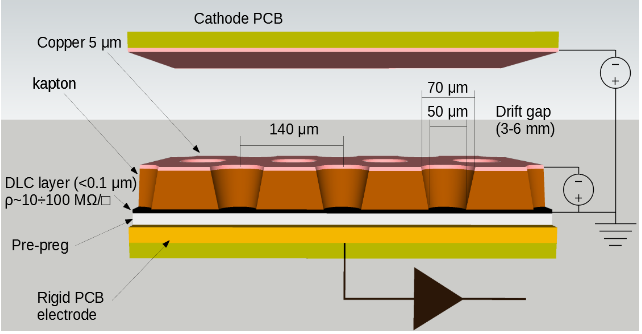
https://cds.cern.ch/record/2776420/

Solutions proposed in the FTDR (2021), currently under scrutiny

Muon system at U2 – the pillars

Rate capability up to ~ 1 MHz/cm²

→ MWPC replaced in the inner regions by µ-RWELL technology (R1 and R2)



Muon system at U2 – the pillars

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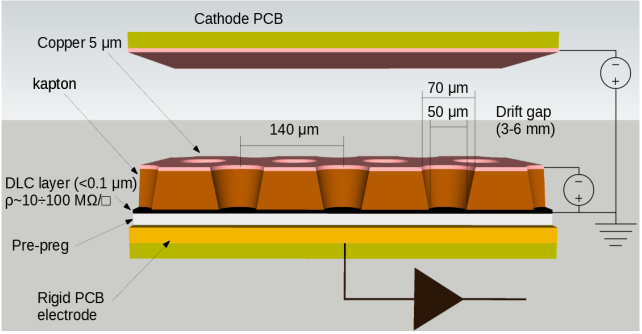

Muon Inefficiency due to FEE deadtime & particle rate

→ Small pads readout in R1 and R2 for μ-RWELL

→ New MWPC with increased granularity (M2R3)

→ Readout individual FEE channels instead the OR

Muon system at U2 – the pillars

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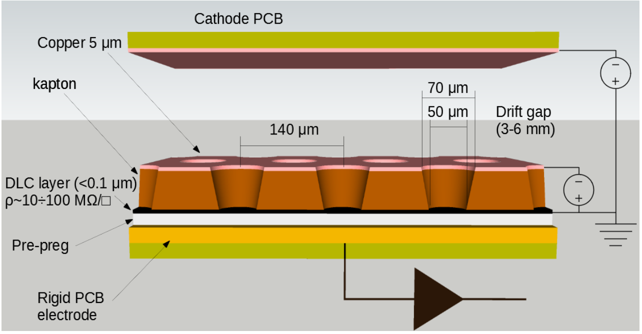


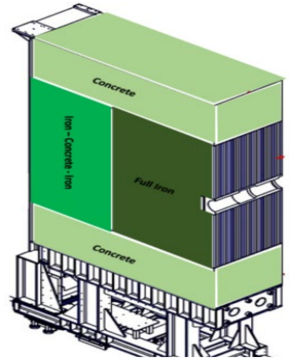
Increase in misID due to large occupancy

- → Increase the shielding in front the Muon system
- → Change readout logic from OR of different gas layers to MAJORITY (2 out of 4): exploits the fact that most of the hits in the Muon System are background and come from particles that cross only one of the 4 gas layers, while muon are penetrating particles.

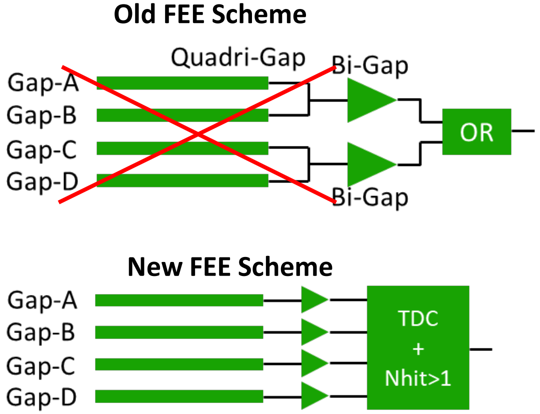
Muon Inefficiency due to FEE deadtime & particle rate

- → Small pads readout in R1 and R2 for µ-RWELL
- → New MWPC with increased granularity (M2R3)
- → Readout individual FEE channels instead the OR

Rate reduction
M2R1 -42%, M2R2 -69% M2R3 -64%



	HCAL	Shielding
1μ, all regions	$97.5 \pm 0.2\%$	$97.7 \pm 0.2\%$
R1	$93.1 \pm 0.9\%$	$93.4 \pm 0.8\%$
R2	$98.2 \pm 0.3\%$	$98.7 \pm 0.2\%$
R3	$99.1 \pm 0.2\%$	$97.4 \pm 0.3\%$
R4	$96.9 \pm 0.4\%$	$98.8 \pm 0.2\%$
2μ, all regions	$94.8 \pm 0.4\%$	$95.4 \pm 0.3\%$



Muon system at U2 – the pillars

Muon Track efficiency vs region

Muon configuration (L = x 10^{34} $cm^{-2}s^{-1}$)	R1	R2	R3	R4
Current detector (1.0)	**45.0**	**83.9**	**91.3**	**96.0**
Middle(*) (1.0)	95.9	97.7	91.3	96.0
Middle(**) (1.3)	95.9	98.0	92.5	95.1
Baseline(**) (1.5)	95.4	97.9	92.1	94.6

(*) µ-RWELL in R1&R2 + FEE majority implementation
(**) improved shielding + new MWPC with higher granularity in R3 + (*)

Inner regions @ U2

µ-RWELL detector requirements[*]

- Rate up to **1 MHz/cm²** on detector single gap
- Rate up to **700 kHz** per electronic channel
- Efficiency (4 gaps) > 98% in the single bunch-crossing (25 ns)
- Stability up to **1C/cm²** accumulated charge in 10y in M2R1, G=4000

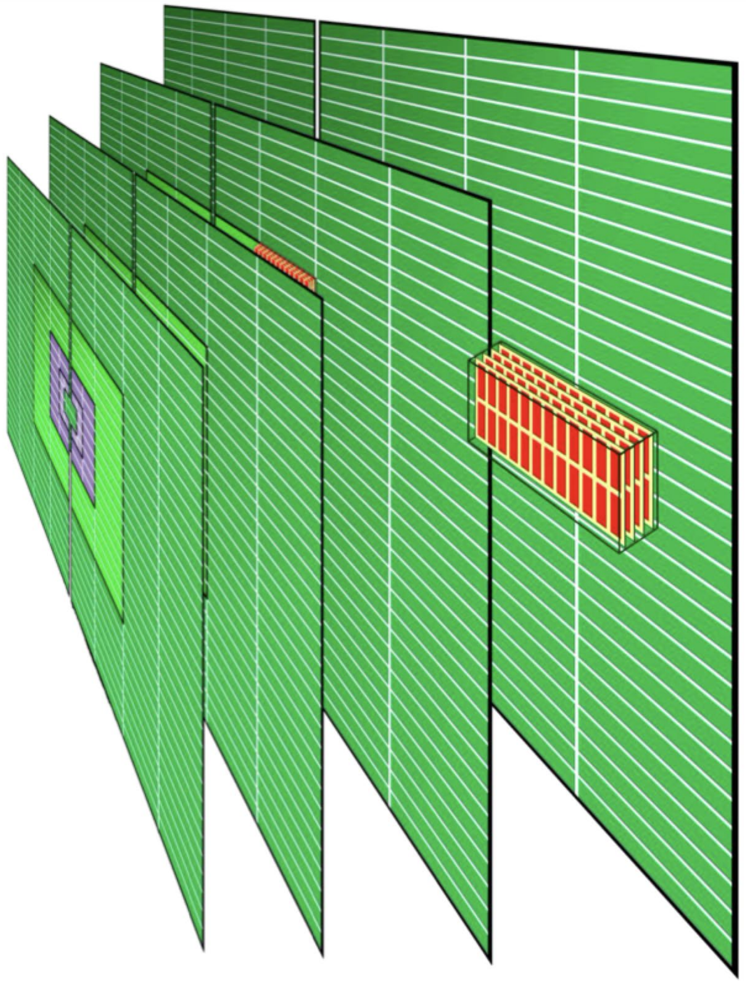
Detector size & quantity (4 gaps/chamber - redundancy)

- R1÷R2: 576 detectors, size 30x25 to 74x31 cm^2, 90 m^2 detector – 130 m^2 DLC

Rates on M2R1-R2 (Hz/cm²)

87171	158083		195088		101979
130403	285249		335035		140339
193482	433458	727665	685944	459769	223005
245971	802007			774528	269882
253768	669975			741341	285779
188207	460502	754272	737256	465171	200051
135798	275142		326036		149601
85221	160448		177895		96254

At **Run 3** start, rate **measurements** perfomed for different luminosity values and **extrapolated** at **Run 5** conditions.

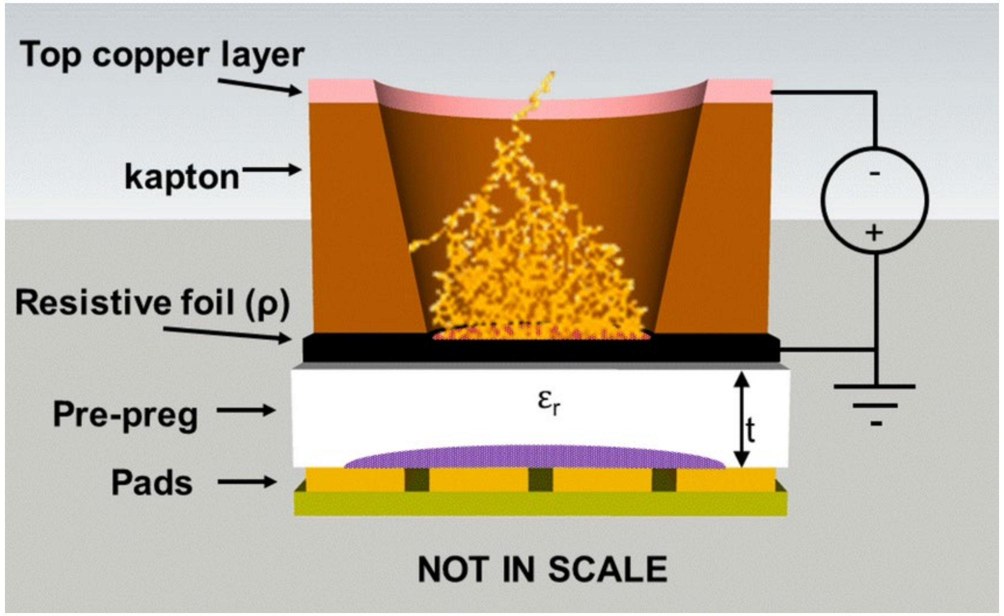


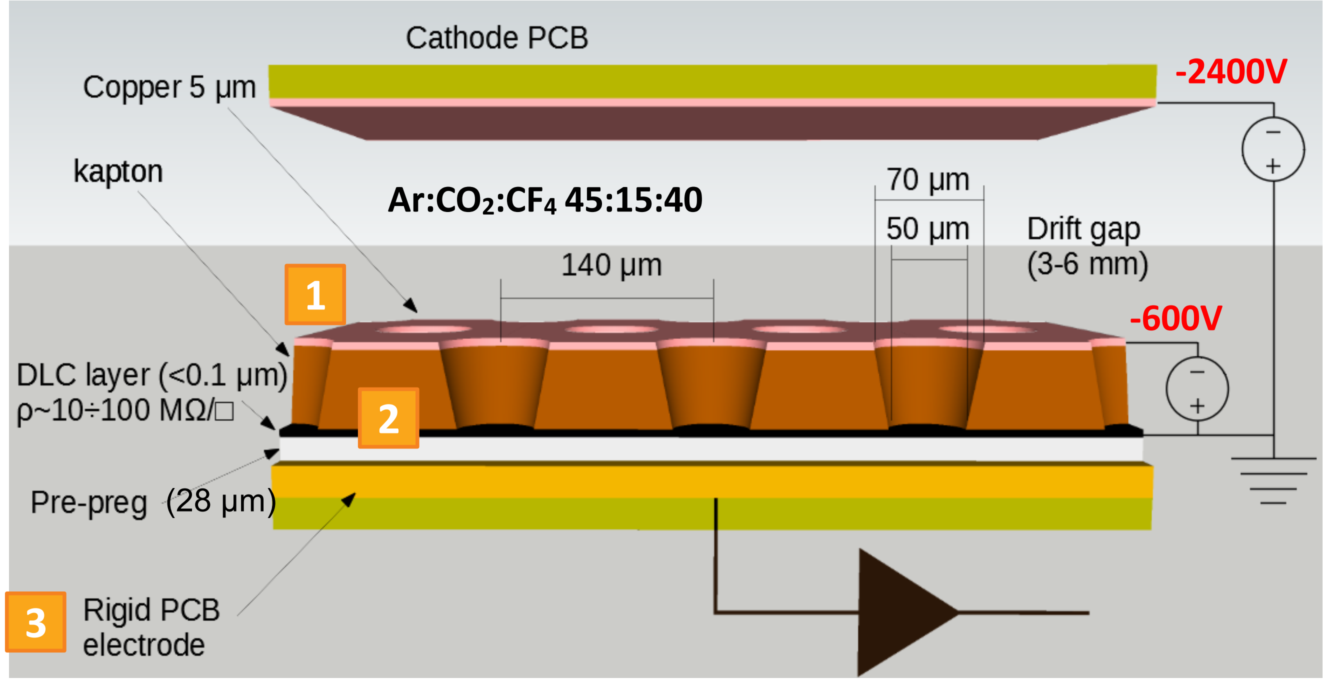
(*) https://cds.cern.ch/record/2776420/

The µ-RWELL detector [reminder]

[G. Bencivenni et al., The micro-Resistive WELL detector: a compact spark-protected single amplification-stage MPGD, 2015 JINST 10 P02008]

The µ-RWELL is a single amplification Micro Pattern Gaseous Detector (MPGD) composed of only two elements: the µ-RWELL_PCB and the cathode. **The core is the µ-RWELL_PCB**, realized by coupling three different elements





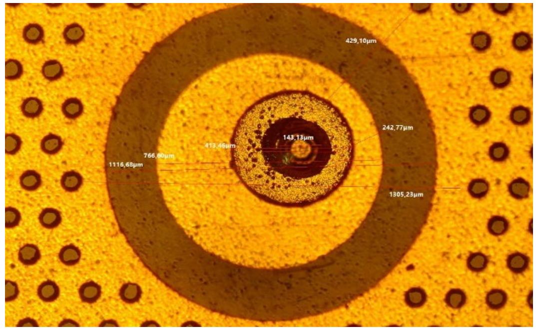
Applying a suitable voltage between the **top Cu-layer and the DLC** the WELL acts as a **multiplication channel for the ionization** produced in the conversion/drift gas gap.

1. **a WELL** patterned Kapton foil acting as **amplification stage** (GEM-like)
2. a **resistive DLC layer (Diamond-Like-Carbon)** for discharge suppression with surface resistivity ~ 50÷100 MΩ/□
3. a standard readout PCB

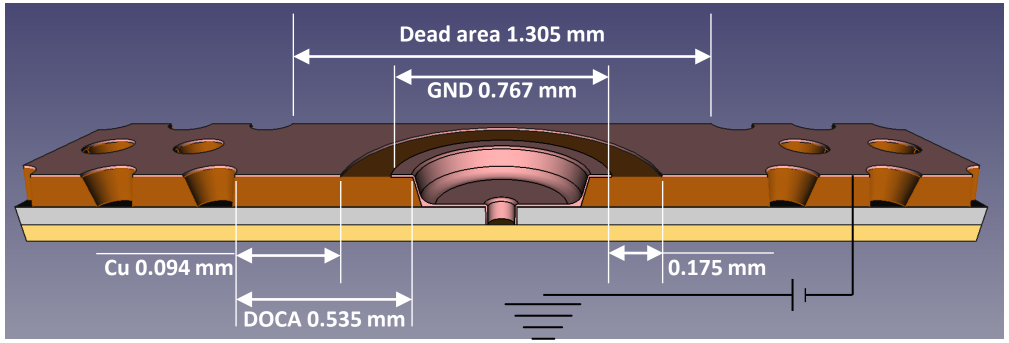
High-rate DOT layout

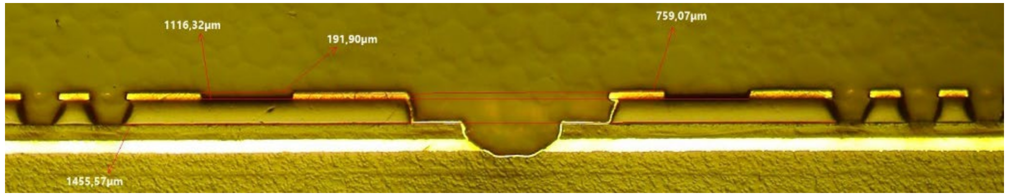
2023 – DOT

DLC grounding by
conductive DOT
Pad R/O = 9×9 mm^2
Grounding: - pitch = 9mm
- rim = 1.3mm



→ **97% geometric** acceptance

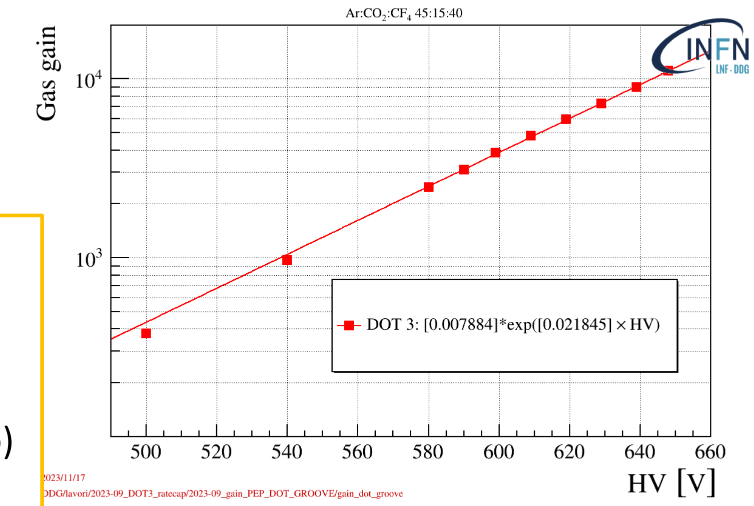


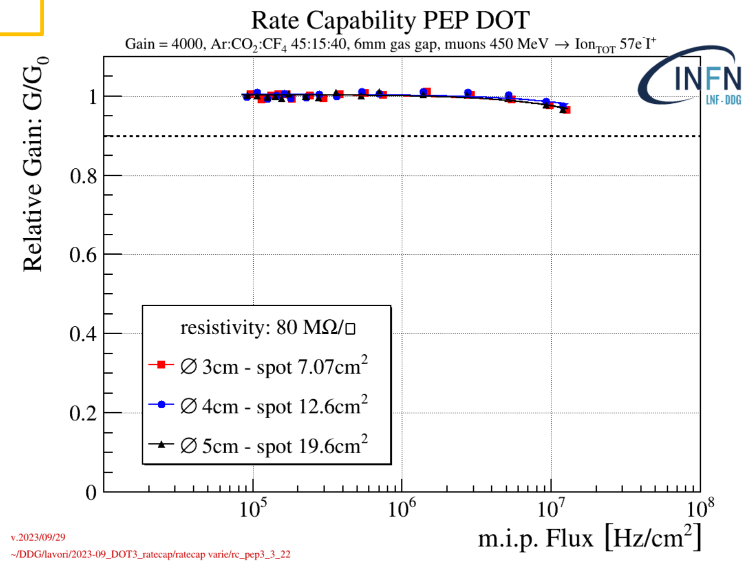


DOT layouts exhibit
satisfactory performance:

- **gas gain** of up to **10^4**
- **rate capability** (@ 90% drop) > **10 MHz/cm^2**

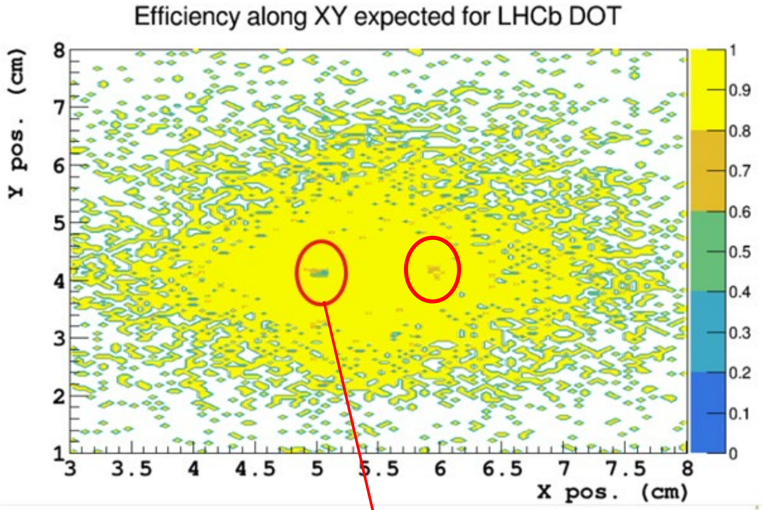
Calibration with X-ray

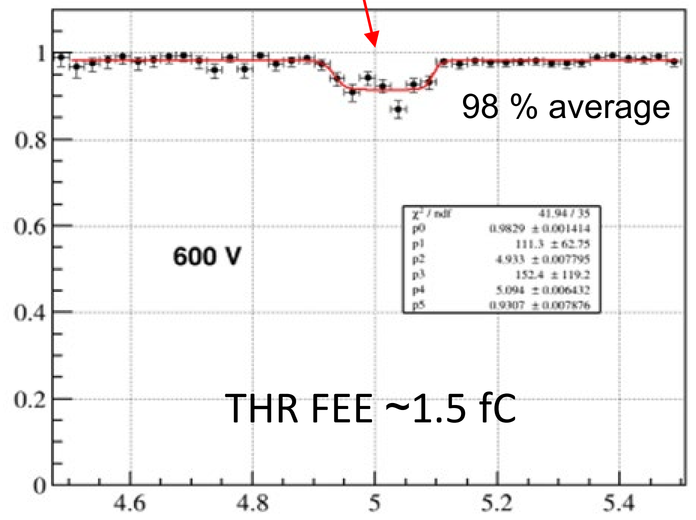




DOT Performance in a Beam Test

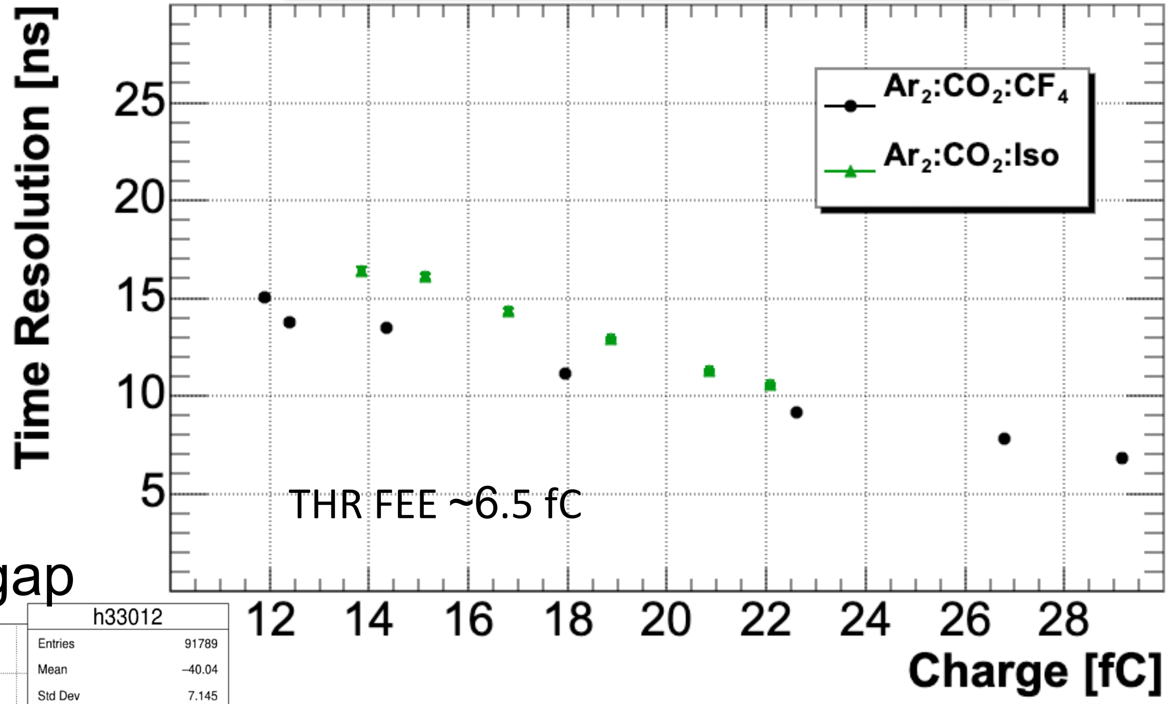
APV-25 FEE



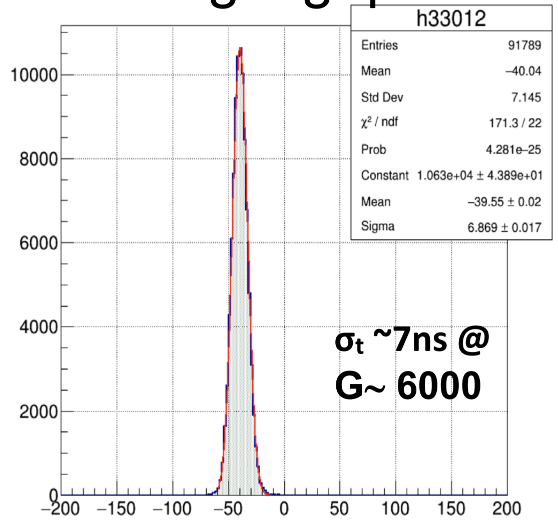


The APV25 Deep Submicron Readout Chip for CMS Detectors

FATIC -2 FEE



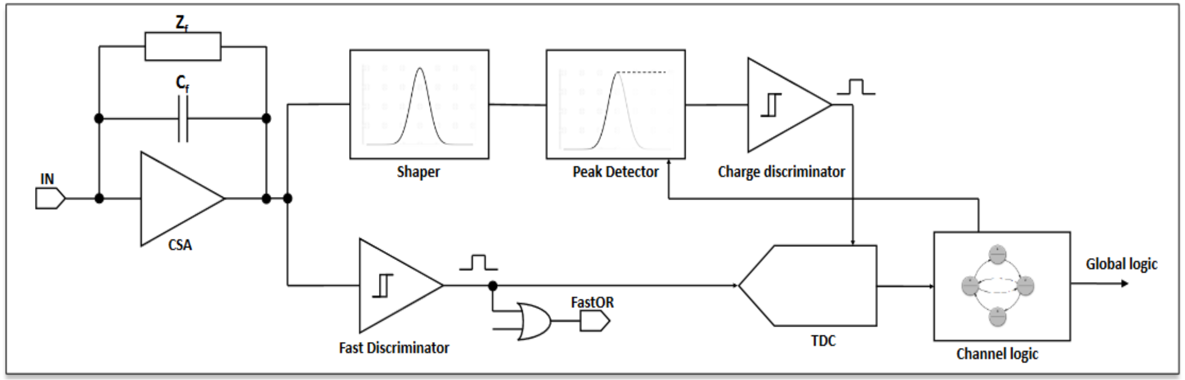
Single gap

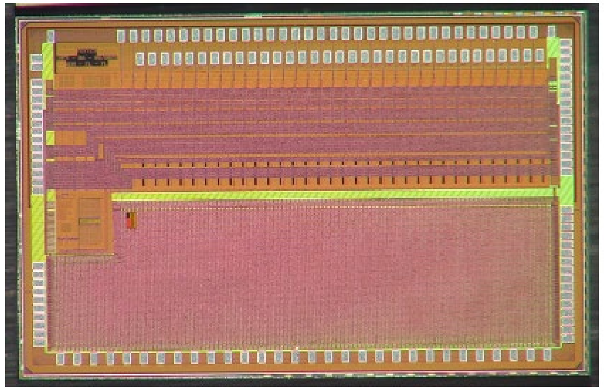


Up to now **CF_4 is fundamental** for the time performance of the detector

A new prototype for the fast timing mpgd (FTM) and the development of fast readout electronics (**FATIC**)

FATIC & future plans





Preamplifier features:
- Recovery time: adjustable
- Input signal polarity: positive & negative
- Recovery time: adjustable

CSA mode:
- Programmable Gain: 10 mV/fC ÷ 50 mV/fC
- Peaking time: 25 ns, 50 ns, 75 ns, 100 ns

Timing branch:
- ✓ Measures the arrival time of the input signal
- ✓ Time jitter: 400 ps @ 1 fC & 15 pF (Fast Timing MPGD)

Charge branch:
- ✓ Acknowledgment of the input signal
- ✓ Charge measurement: dynamic range > 50 fC, programmable charge resolution

FATIC3: Mainly a bug fixing plus some features integration wrt FATCIC 2
- Channel FSM bug fix
- Trigger data filter moved from FPGA to ASIC
- Increase of transmission speed from 320 to 640 Mbps
- Integrated monitoring ADC and voltage reference IP
- Cut of power consumption down to 150 mW

FATIC4: Performance improvement
- Lower dead time, from ~2 us to ~100 ns
- More digital features to make the chip closer to LHCb needs

Submission foreseen for 2025

µ-RWEEL proto-0

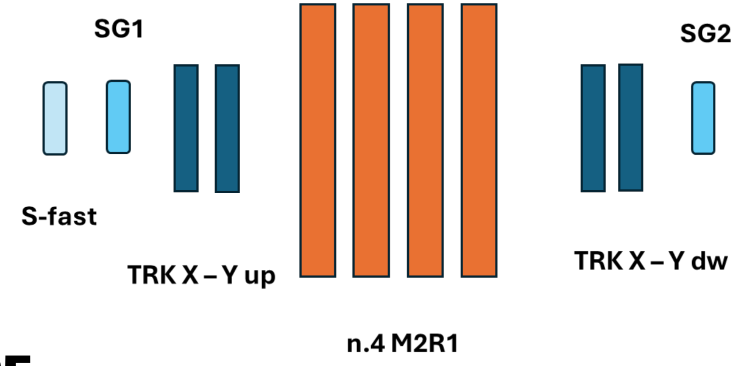
2024

N. 4 M2R1 has been delivered in June 2024:

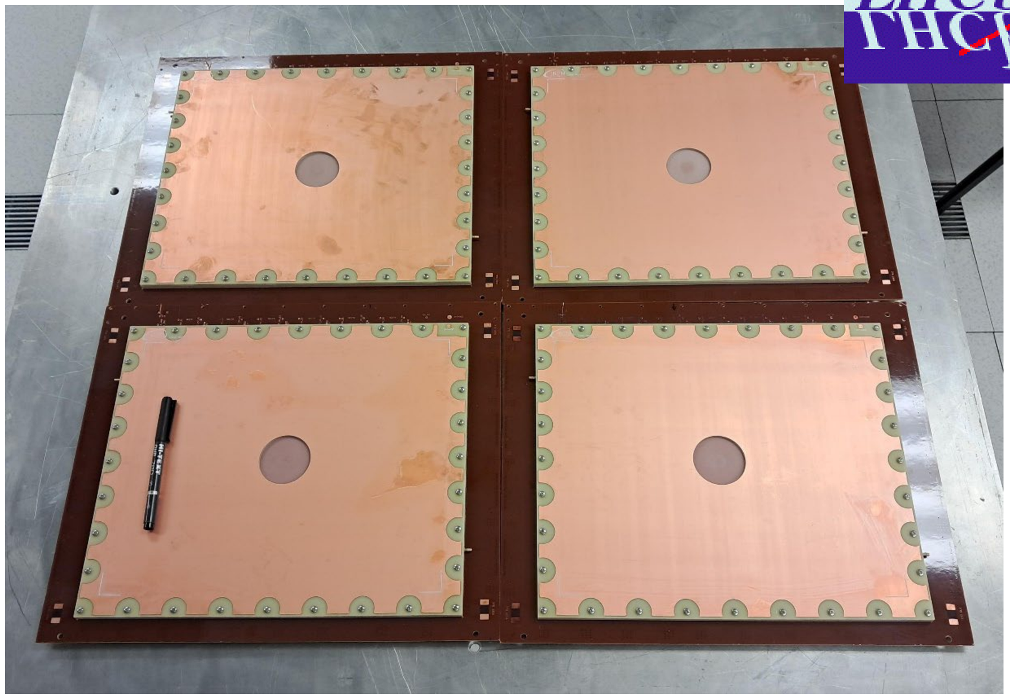
→ The **CID** (CERN-INFN-DLC) sputtering machine, a **joint project between CERN and INFN**, is used for preparing the Diamond-Like-Carbon (DLC) **base material of the detector**

X-ray characterization July 2024

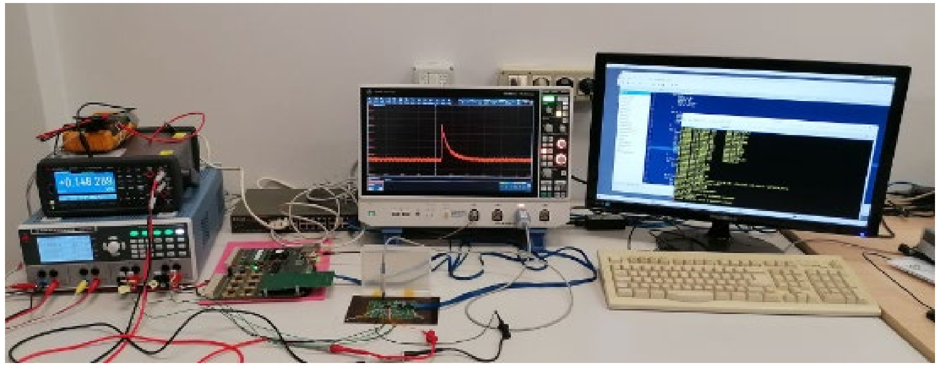
Test Beam with FATIC3 Nov 2024



FATIC 3 Board



N.4 M2R1 proto-0



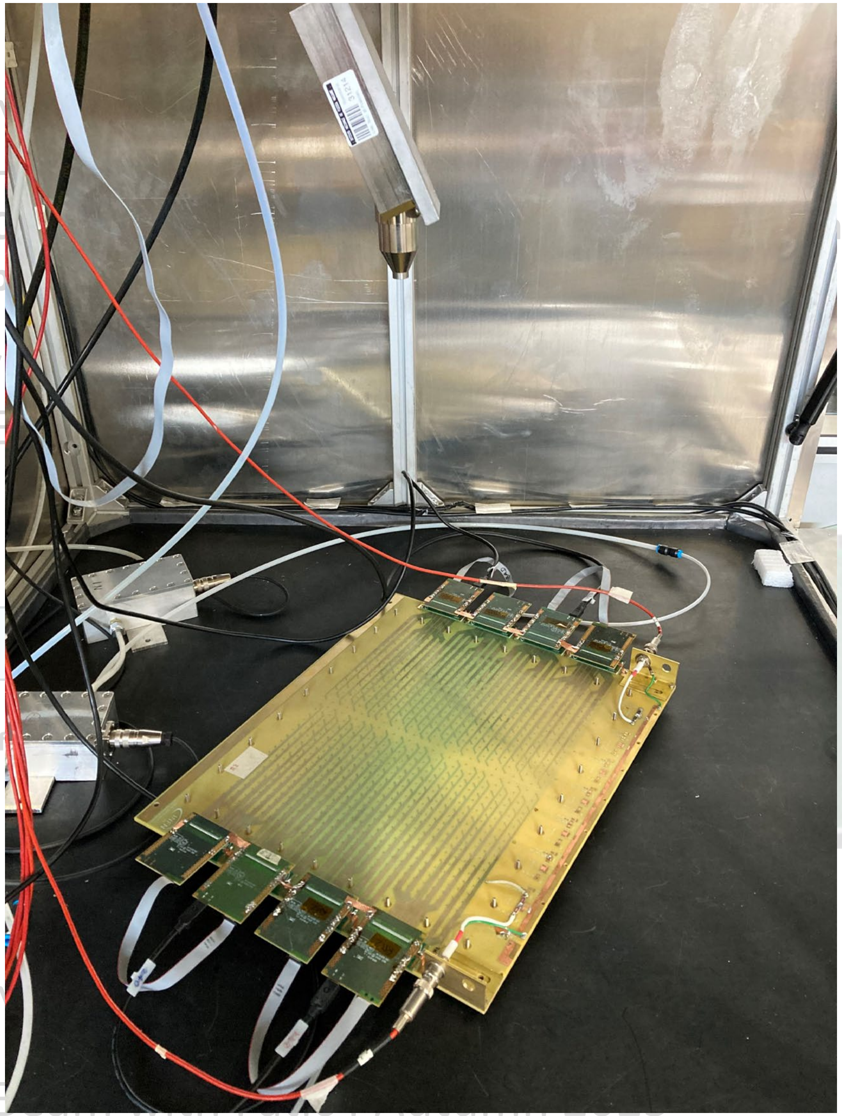
Test of FATIC3 Chip

2025

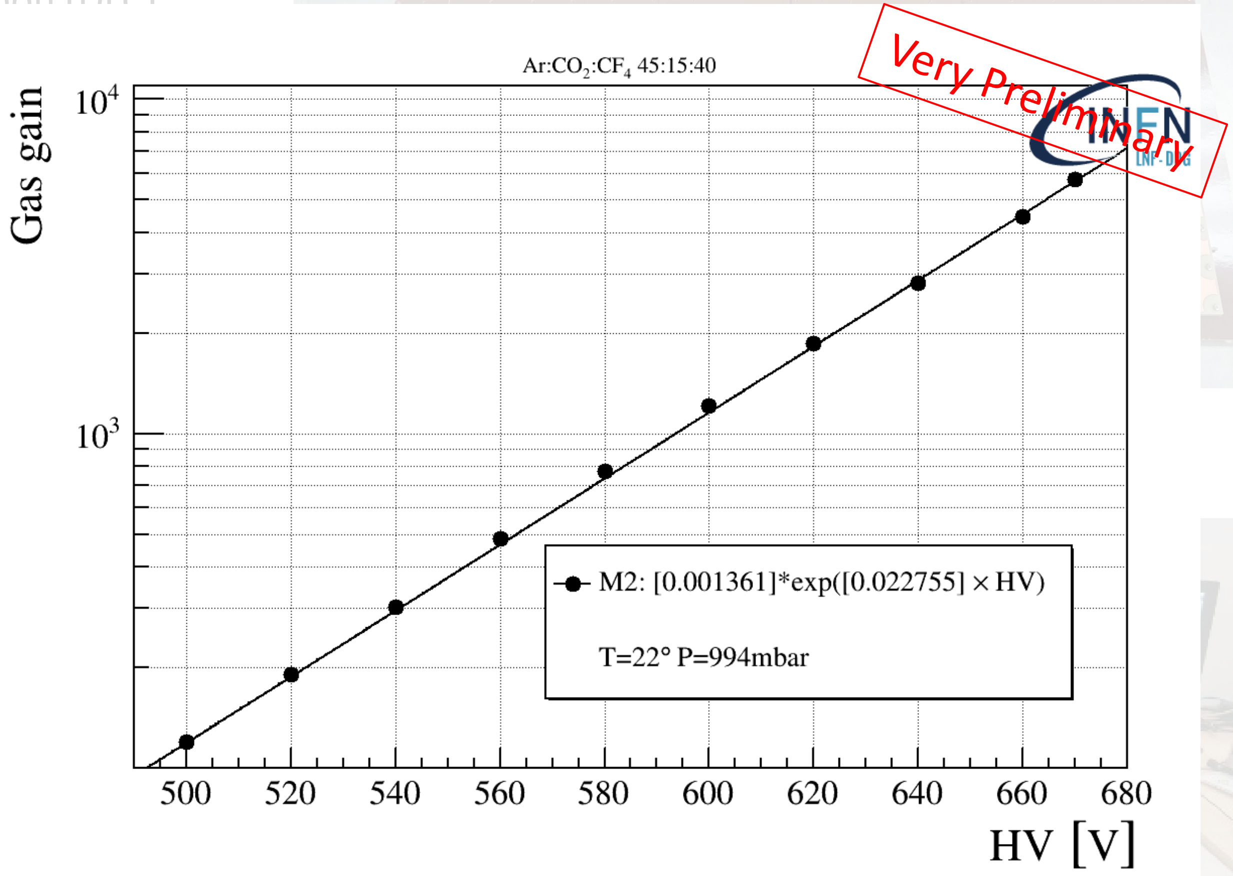
N. 2 M2R2-M5R2 will be produced in 2025

Test Beam with Fatic4 Autumn 2025

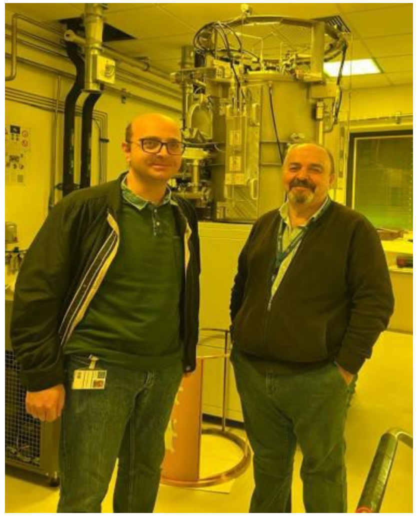
µ-RWEEL proto-0



Calibration with X-ray



DLC sputtering



The **CID** (CERN-INFN-DLC) sputtering machine, a **joint project between CERN and INFN**, is used for preparing the **base material of the detector**. The potential of the DLC sputtering machine is:

- **Flexible substrates** up to **1.7m×0.6m**
- **Rigid substrates** up to **0.2m×0.6m**

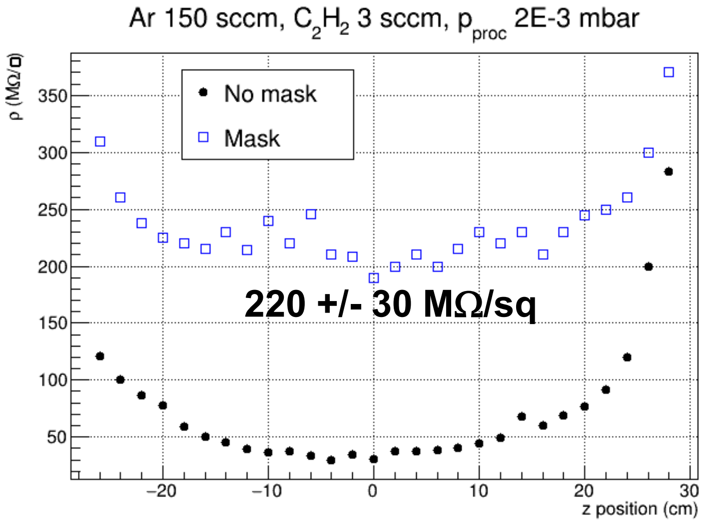
In **2023,** the activity on CID focused on the **tuning** of the **machine on small foils:** very **good** results in terms of **reproducibility and uniformity.**

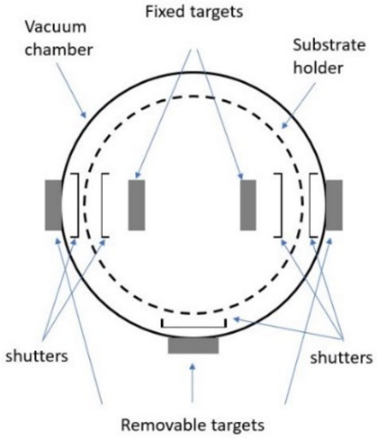
In **2024**, the **sputtering test are made on large foils, uniformity optimization is ongoing.**

C.I.D.

The graphite target

The three external cathodes



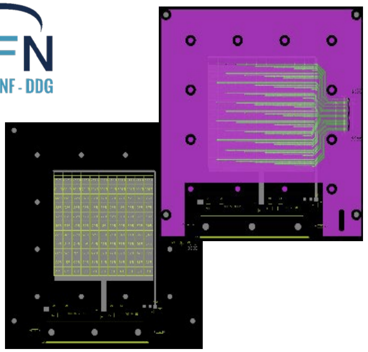


Machine co-funded by CERN and INFN-CSN1. R&D led by INFN LNF, Roma3 and Naples

Technology Transfer

Feedback from tests

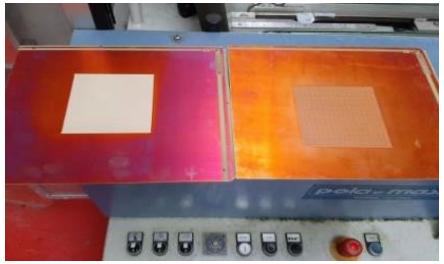
LAYOUT design

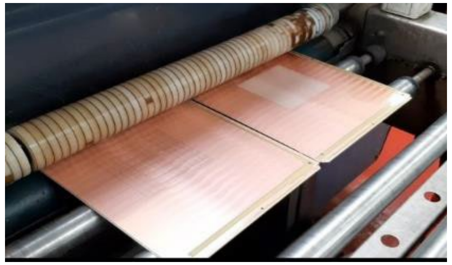


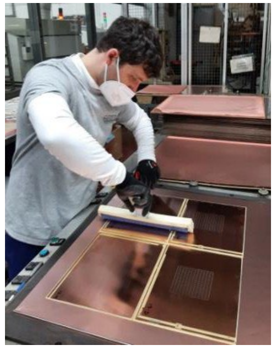
DLC foil production[*]

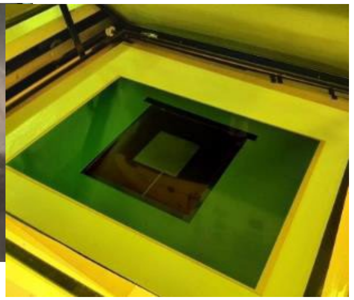
[*] DLC Magnetron Sputtering machine co-funded by INFN- CSN1

PCB production

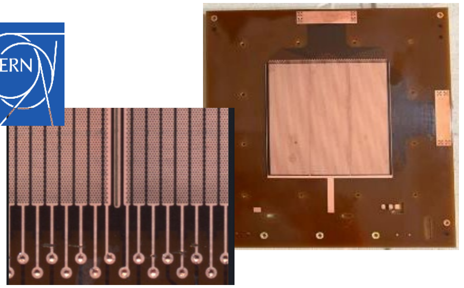


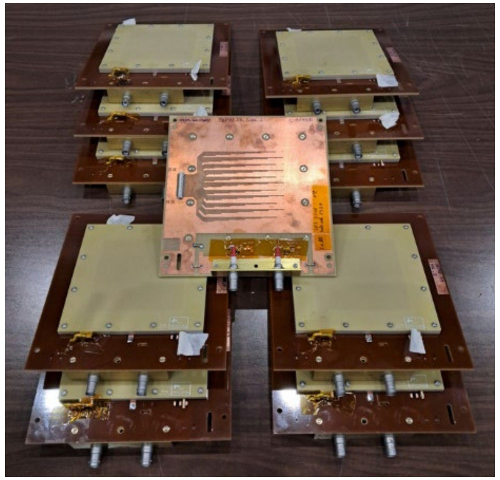






Final detector manufacturing





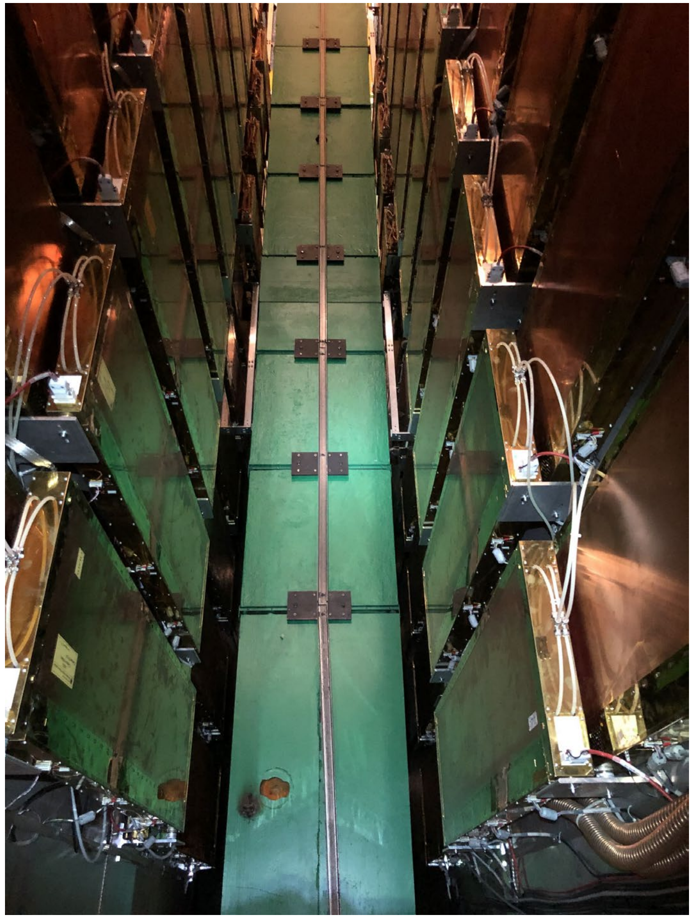
Overview for external regions

MWPC production:

- The number of detectors to be built changes significantly based on the chosen LHCb scenario.
- Ongoing contacts with non LHCb institutes to plan the different scenarios

ASIC chip for MWPC:

- The current chip (CARIOCA*) does not support majority logic
- Tests planned for fall 2024 will check if the FATIC can also be used for MWPC, considering their different capacitance values and signal shapes
- If the FATIC cannot be used for MWPC, a new chip must be developed



(*) Development of the CARIOCA front-end chip for the LHCb muon detector

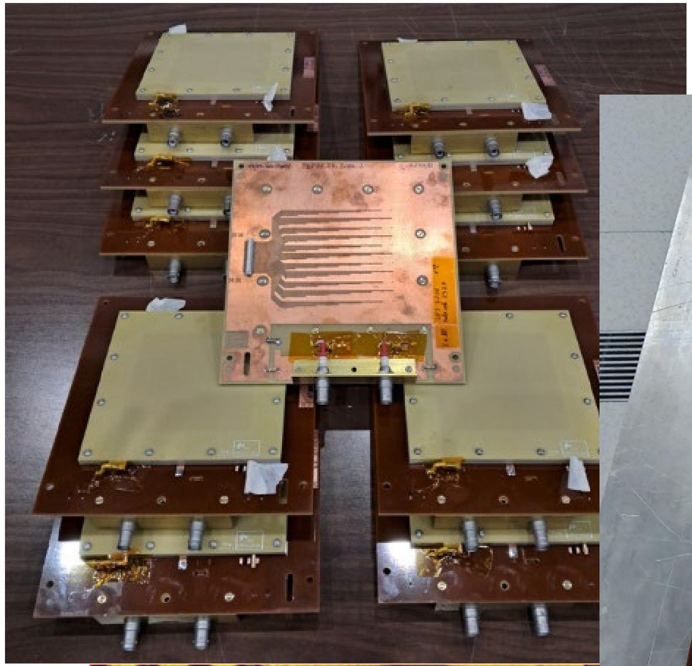
Summary & Outlook

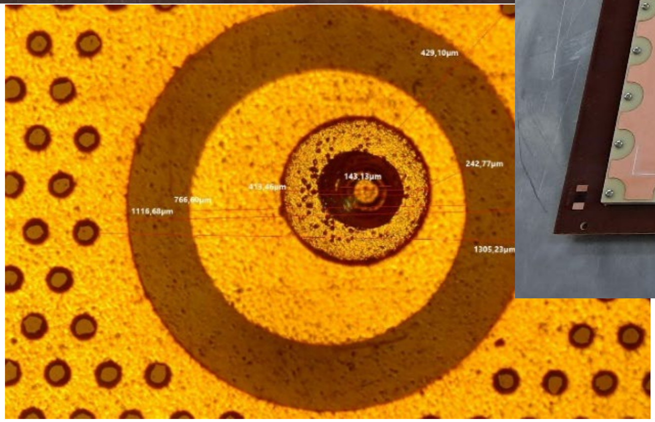
The **R&D** on **high-rate layouts for the LHCb upgrade** has been completed:

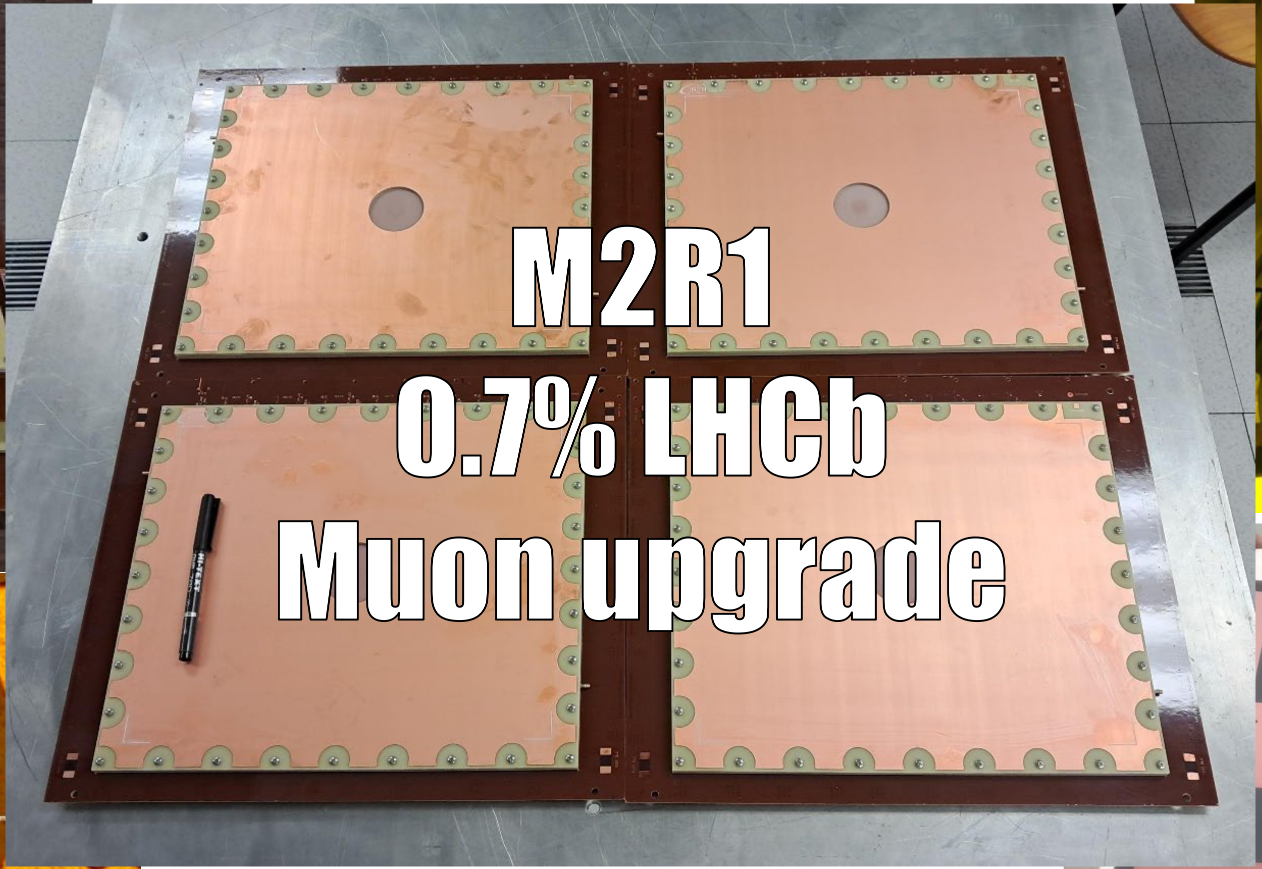
- ✅ the **PEP-DOT** layout shows good performance**:** gain of **10^4, 98%** efficiency, **> 10 MHz/cm^2**, **7ns** time resolution
- **General parameters** of the detector have been set to **maximize stability and gain**:
  - ✅ **ρ ≥ 50 MΩ/sq, DOCA = 0.5 – 0.6mm (dead-zone < 3%)**
  - ✅ **prepreg thickness ~ 28µm**
  - WORK IN PROGRESS: Amplification stage optimization by reducing the **well pitch:** from 140µm down to 90µm
- **Large size**:
  - ✅ **M2R1 (25x30 cm^2** active area): **delivered June '24**, X-ray characterization in July, test beam in **Nov. '24**.
  - WORK IN PROGRESS: **M2R2/M5R2 (31x75 cm^2** active area)**: design** by the end of **2024, production** beginning in **2025**

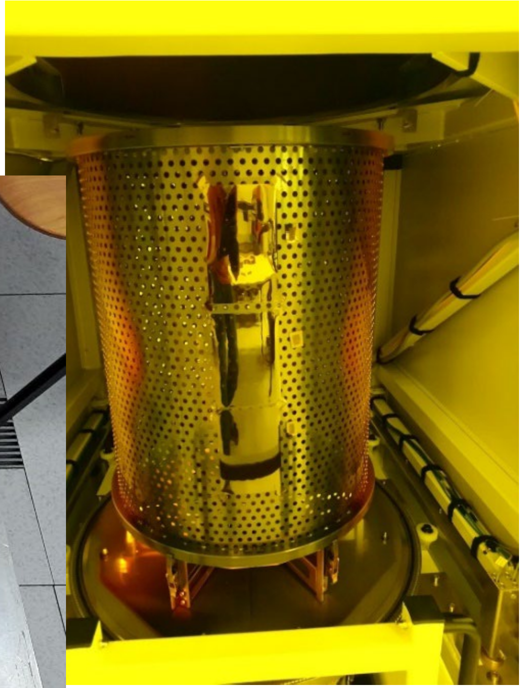
The **detector manufacturing process** is nearly finalized:

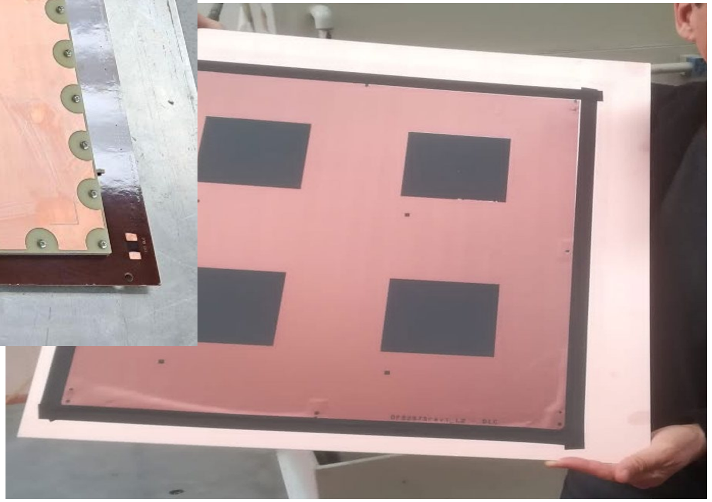
- ✅ Several construction **steps are performed by ELTOS**
- ✅ **Detector finalization** (Kapton etching, electrical hot cleaning, etc.) is **carried out at CERN**
- ✅ The **DLC sputtering machine**, C.I.D., **will provide the base material**, once the sputtering parameters are optimized






M2R1
0.7% LHCb
Muon upgrade





MUON ID

Let’s recall the logic of the present muon identification, its performance essentially drives the design. Its relies in two steps

- Open a Field of Interest (FoI) along the track extrapolation with a size that depends on momentum (Multiple scattering dominates wrt pad size) + Ask for hit presence in consecutive stations according to track momentum

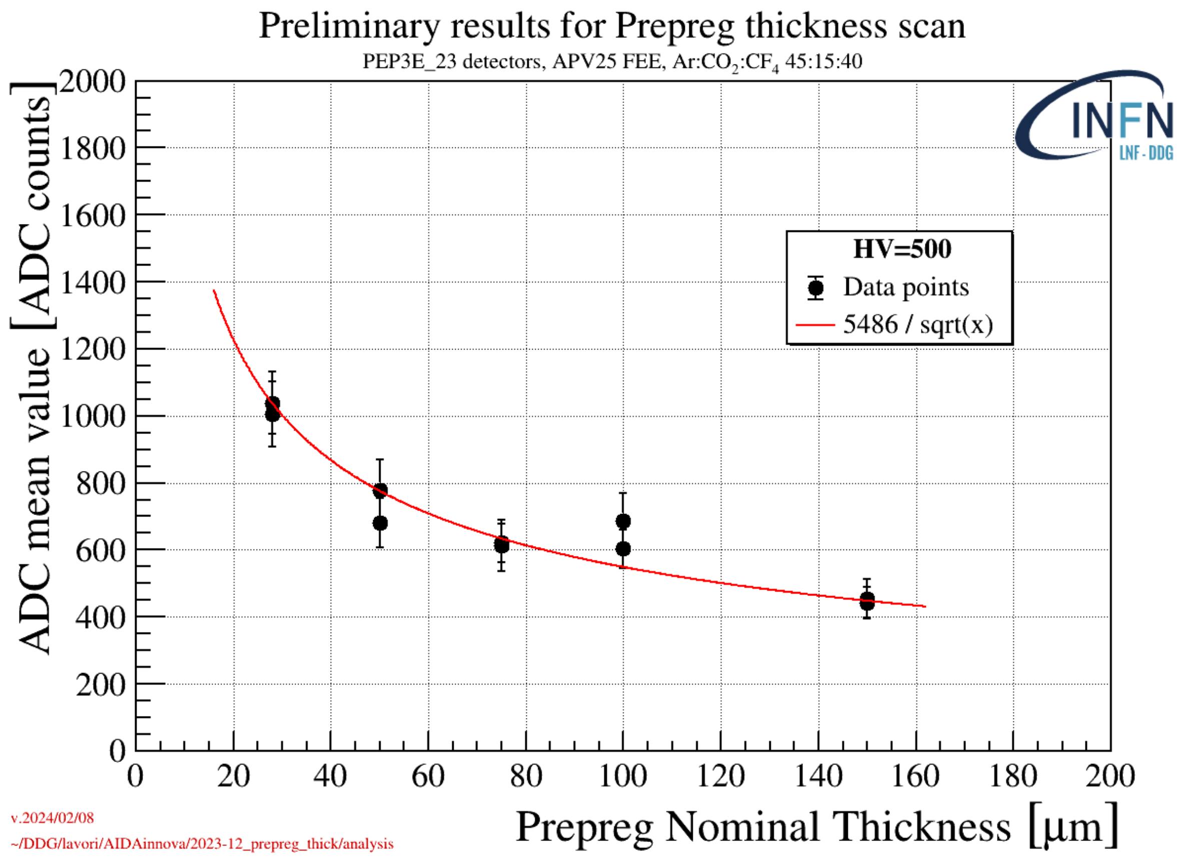
- Fit with a correlated c^2 to discriminate accidental from true tracks

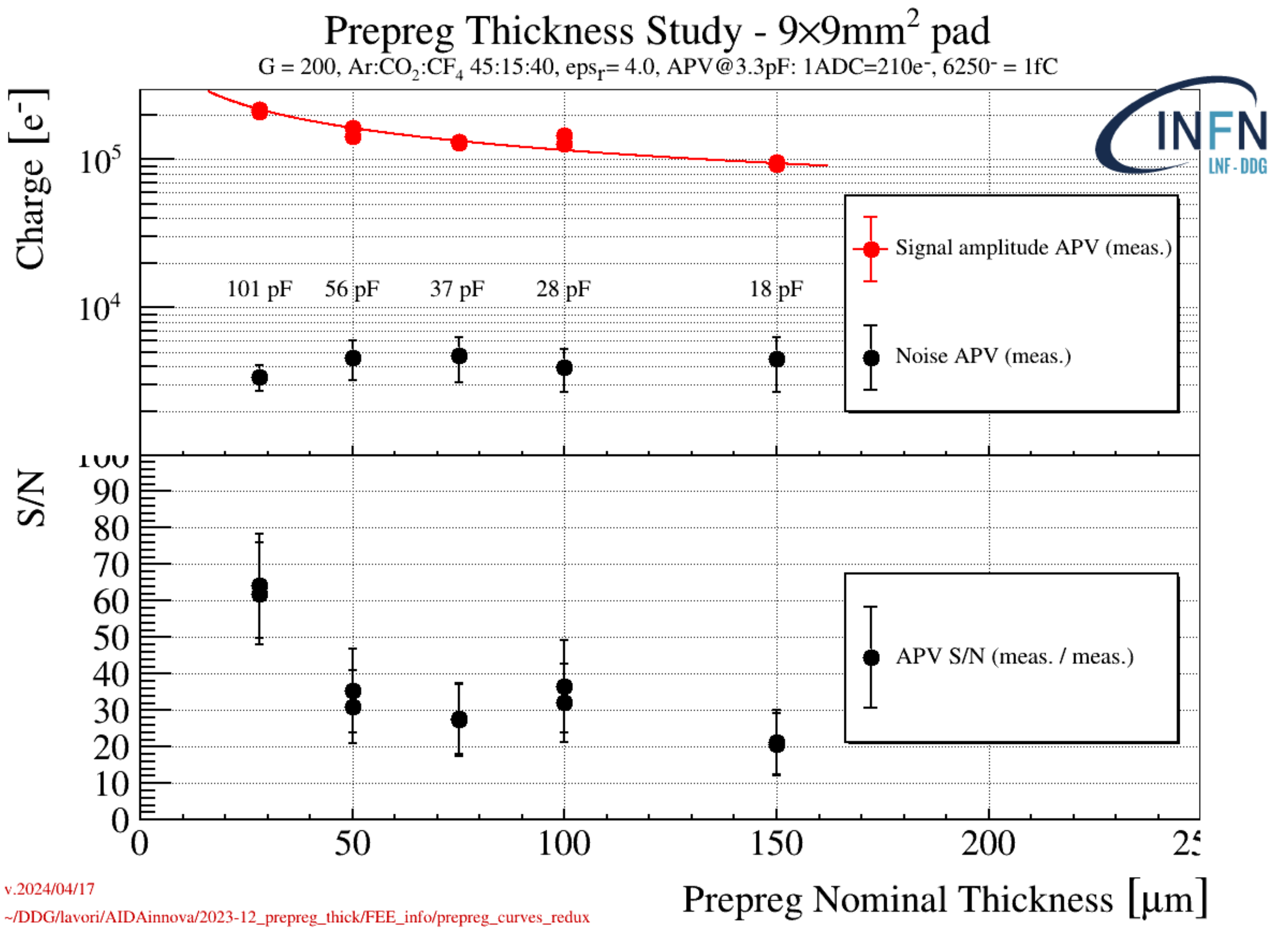
It is clear that we need:

- **high hit efficiency in each station**
- **not too high background rate to reduce the accidental**

Momentum (GeV)	IsMuon	Max. Efficiency
P< 3	**FALSE**	-
3< P < 6	M2& M3	98%
6 < P < 10	M2& M3 & (M4 ‖ M5)	97%
P > 10	M2& M3 & M4 & M5	96%

Prepreg thickness optimization

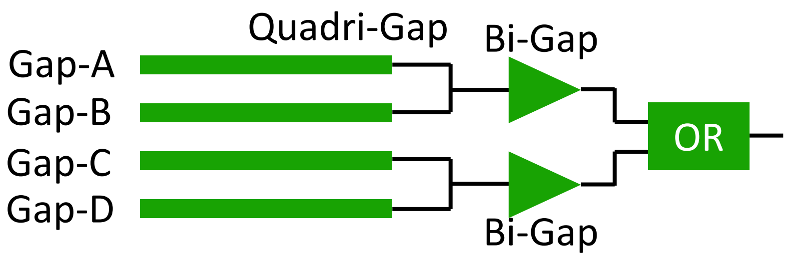




NB: R&D for LHCb – pad R/O
Future plans: searching for prepreg thinner than 28um

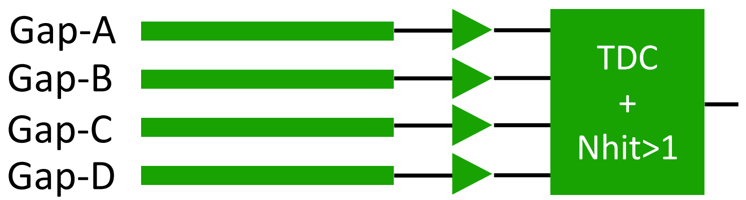
Muon FE Architecture

- **Present FE readout** electronics read the OR of a quadri-gap



- Rates @Run5: very high and dominated by single-gap bkg signals

- **New FE electronics** read 4 gaps individually



- Custom 64 channel FE ASIC
  - 4 gaps read individually
  - Majoriy logic: validate events with Nhit>1 to reduce uncorrelated background hits
  - TDC info of a single gap (selectable via ECS) is read

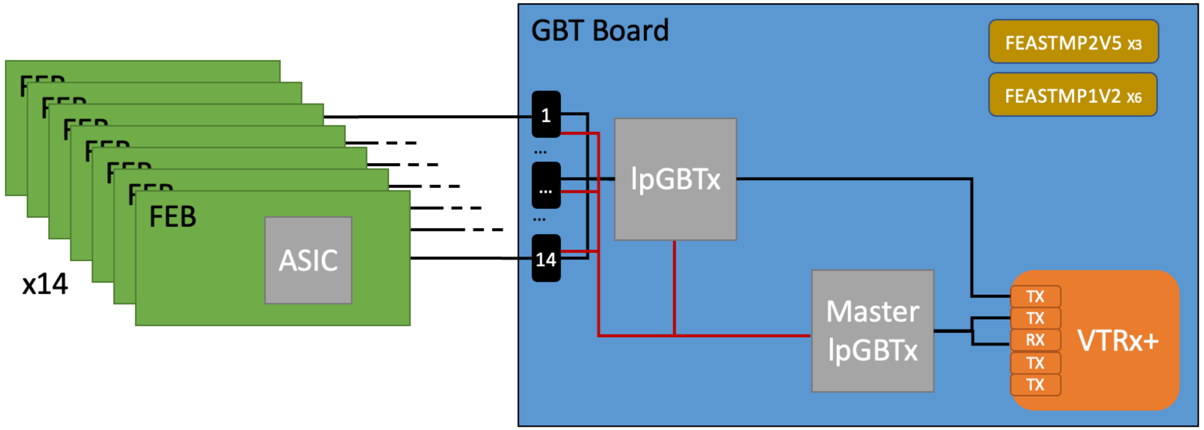
Muon RO architecture (*)

Current baseline architecture:

- Specific links dedicated to Data and TFC/ECS: 1 Data lpGBTx and 1 Master lpGBTx per GBT board
- Up to 14 FE chip per data lpGBTx via 1 eLink @ 640MHz

New architecture by numbers

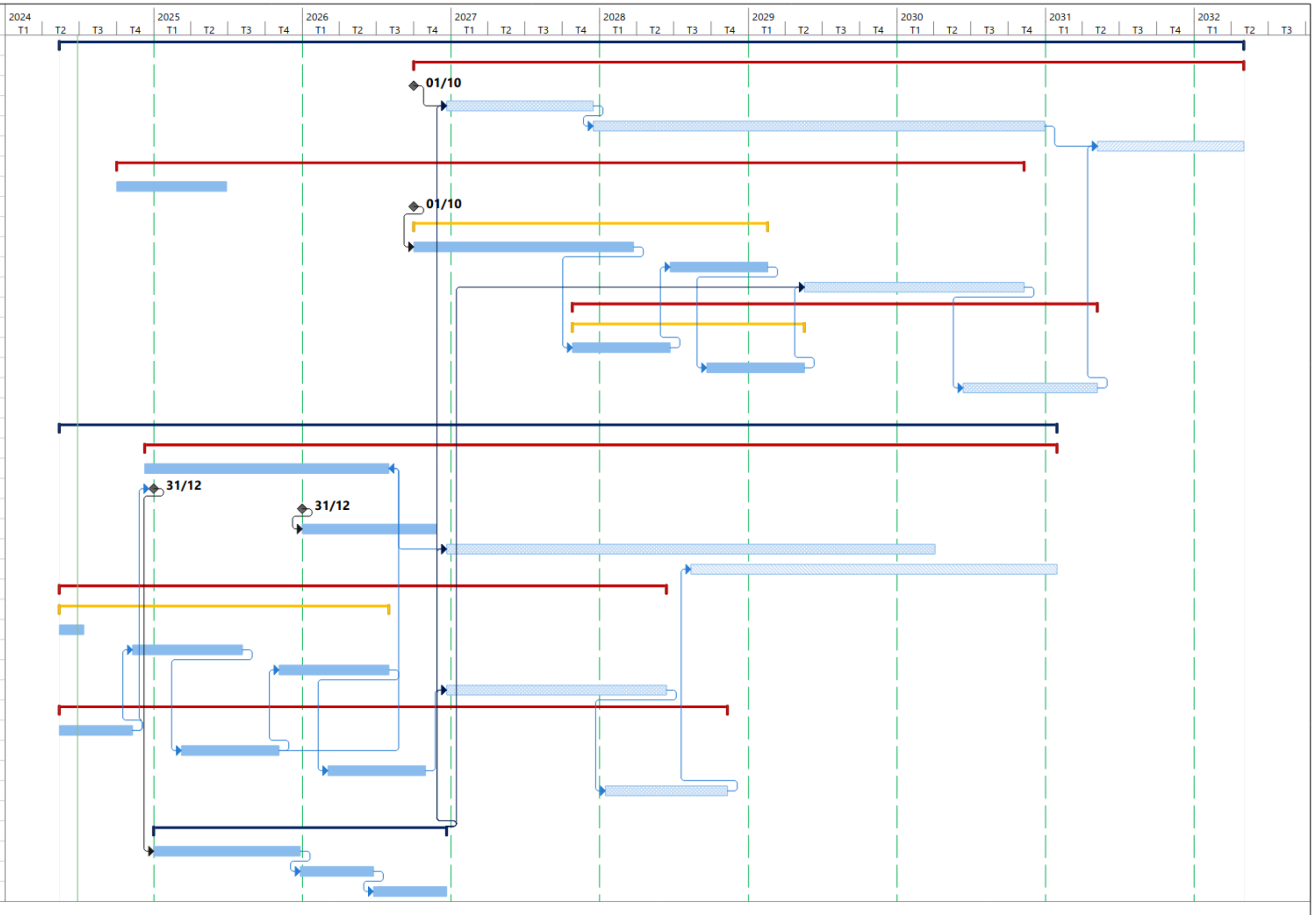
- ASIC 13K
- lpGBTx: 1576 (Data) + 1576 (TFC/ECS)
- PCIe400 70
- FE Bandwidth 8.5Tbps



Presented by P. Albiccoco at “FEE@U2 workshop” https://indico.cern.ch/event/1348261/contributions/5741282/attachments/2786544/4858506/LHCb_240124.pdf

Preliminary schedule

Nome attività	Durata	Inizio	Fine	Predecessori
MWPC	**97.03 mes?**	**13/05/24 09:00**	**02/05/32 09:00**	
MWPC construction	**68 mes?**	**01/10/26 09:00**	**02/05/32 09:00**	
Decision on construction	0 mes?	01/10/26 09:00	01/10/26 09:00	
Material procurement	12 mes?	21/12/26 09:00	16/12/27 09:00	3,40
Detector production	37 mes?	16/12/27 09:00	30/12/30 09:00	4
FE installation	12 mes?	08/05/31 09:00	02/05/32 09:00	5,18
MWPC ASIC	**74.33 mes?**	**01/10/24 09:00**	**09/11/30 09:00**	
Investigate usage of ASIC RWELL	9 mes?	01/10/24 09:00	28/06/25 09:00	
Start of MWPC ASIC Design	0 mes	01/10/26 09:00	01/10/26 09:00	
MWPC ASIC Design	**29 mes?**	**01/10/26 09:00**	**17/02/29 09:00**	
ASIC version 1 (design and production)	18 mes?	01/10/26 09:00	24/03/28 09:00	9
ASIC version 2 (design and production)	8 mes?	22/06/28 09:00	17/02/29 09:00	16
Production (engineeering run, packaging, test)	18 mes	18/05/29 09:00	09/11/30 09:00	17,40
MWPC FE	**43 mes?**	**26/10/27 09:00**	**08/05/31 09:00**	
Prototyping + test	**19 mes?**	**26/10/27 09:00**	**18/05/29 09:00**	
Proto1 test (ASIC ver1)	8 mes?	26/10/27 09:00	22/06/28 09:00	11FI-5 mes
Proto2 test (ASIC ver2)	8 mes?	20/09/28 09:00	18/05/29 09:00	12FI-5 mes
Production	11 mes?	12/06/30 09:00	08/05/31 09:00	13FI-5 mes
RWELL	**81.73 mes?**	**13/05/24 09:00**	**29/01/31 09:00**	
RWELL construction	**74.73 mes?**	**09/12/24 09:00**	**29/01/31 09:00**	
R&D	20 mes?	09/12/24 09:00	01/08/26 09:00	36FF
Validation M2R1 design with FATIC3	0 mes	31/12/24 09:00	31/12/24 09:00	35
	0 mes	31/12/25 09:00	31/12/25 09:00	
Prototyping	11 mes?	31/12/25 09:00	26/11/26 09:00	24
Detector production	40 mes?	21/12/26 09:00	04/04/30 09:00	40,22
FE installation	30 mes?	12/08/28 09:00	29/01/31 09:00	38FI-3 mes
RWELL ASIC	**49.73 mes?**	**13/05/24 09:00**	**13/06/28 09:00**	
RWELL ASIC Design	**27 mes?**	**13/05/24 09:00**	**01/08/26 09:00**	
FATIC3 (production and test)	2 mes?	13/05/24 09:00	12/07/24 09:00	
FATIC4 (production and test)	9 mes?	09/11/24 09:00	06/08/25 09:00	35
FATIC5 (production and test)	9 mes?	04/11/25 09:00	01/08/26 09:00	36
Production (engineeering run, packaging, te	18 mes?	21/12/26 09:00	13/06/28 09:00	40,37
RWELL FE	**54.73 mes?**	**13/05/24 09:00**	**10/11/28 09:00**	
Proto1 test (FATIC3)	6 mes?	13/05/24 09:00	09/11/24 09:00	
Proto2 test (FATIC4)	8 mes?	09/03/25 09:00	04/11/25 09:00	31FI-5 mes
Proto3 test (FATIC5)	8 mes?	04/03/26 09:00	30/10/26 09:00	32FI-5 mes
Production	10 mes?	15/01/28 09:00	10/11/28 09:00	33FI-5 mes
TDR	**24 mes?**	**31/12/24 09:00**	**21/12/26 09:00**	
TDR writing	12 mes?	31/12/24 09:00	26/12/25 09:00	23
TDR approvation	6 mes?	26/12/25 09:00	24/06/26 09:00	41
INFN financing	6 mes?	24/06/26 09:00	21/12/26 09:00	42



Muon system at U2 – the pillars

Rate capability up to ~ 1 MHz/cm²

→ MWPC replaced in the inner regions by μ-RWELL technology (R1 and R2)

Muon Inefficiency due to FEE deadtime & particle rate

- → Increase granularity in R1 and R2 for the μ-RWELL
- → New MWPC with increased granularity in most critical R3 part
- → Readout individual FEE channels instead of group of them

Muon Track efficiency vs region

Muon configuration	R1	R2	R3	R4
Current detector (1.0)	**45.0**	**83.9**	**91.3**	**96.0**
Middle (1.0)	95.9	97.7	91.3	96.0
Middle (1.3)	95.9	98.0	92.5	95.1
Baseline (1.5)	95.4	97.9	92.1	94.6

Increase in misID due to large occupancy

- → Increase the shielding in front the Muon system
- → Change readout logic from OR of different gas layers to MAJORITY (2 out of 4): exploits the fact that most of the hits in the Muon System are background and come from particles that cross only one of the 4 gas layers, while muon are penetrating particles.