Integration test of a new inner-station TGC system for the ATLAS experiment at HL-LHC

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Abstract

We integrated the detector and the readout electronics for a new inner-station TGC system at the ATLAS experiment and evaluated the performance in preparation for the HL-LHC. The TGC detectors installed in the endcap inner stations of the ATLAS detector will be upgraded from doublet to triplet chambers to improve the selectivity of the first-level muon trigger. The challenging structure of fitting a triplet within the same envelope as the doublet necessitates integration tests with the readout electronics. The detector and readout electronics from early production were integrated, and the measurements showed an acceptable noise level and a detection efficiency of 94% for each layer. Additionally, the trigger firmware was developed requiring coincidences in two or more layers for this detector, which was confirmed through the functional simulation.

Introduction

- The HL-LHC is planned to start in 2029. The ATLAS detector must process 4000 fb^{-1} of proton-proton collision data and withstand over 200 pile-up events.
- To select interesting events from the vast amount of hits, upgrades are planned for detector, trigger, and DAQ.
- The TGC detectors used for muon triggers, located at $1.05 \leq |\eta| \leq 1.3$, will be replaced.
  - From doublet to triplet
  - To suppress fake muons (charged particles not directly originating from proton-proton collisions) and low momentum muons (Fig. 1).
  - Distinguish between truth muons and fake muons by taking coincidence with the end-cap TGC detector (Fig. 2).
- **The assembly of the first module of the new TGC detector has been completed, and the performance was evaluated.**
  - The noise level and detection efficiency for cosmic muons are measured.
  - The DAQ system is based on SoC device.

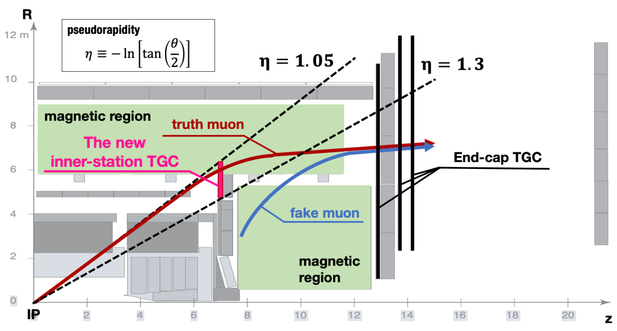

Figure 1:
Location of the new inner-station TGC and the difference between truth muons and fake muons

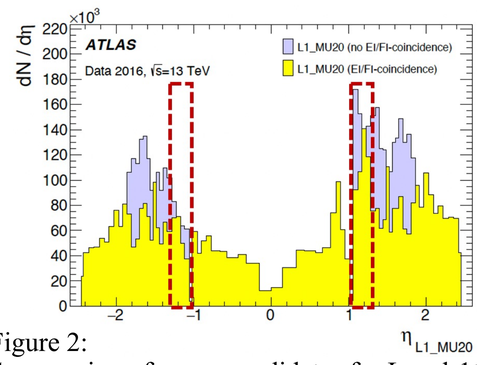

Figure 2:
Suppression of muon candidates for Level-1trigger (The red area indicates the region covered by the new inner-station TGC)

TGC detector and set up of DAQ system

New inner-station TGC detector

- **Triplet structure for both wire and strip (Fig. 3).**
- The same thickness as doublet.
- The study of noise level and detection efficiency are key ingredients of the performance evaluation.

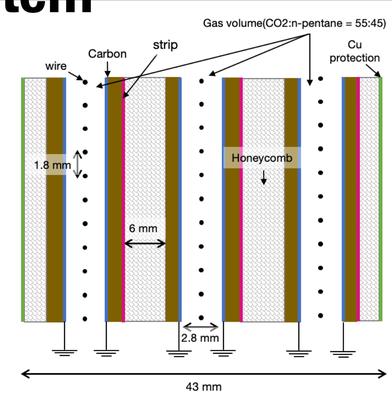

Figure 3: Internal structure of TGC detector

DAQ system

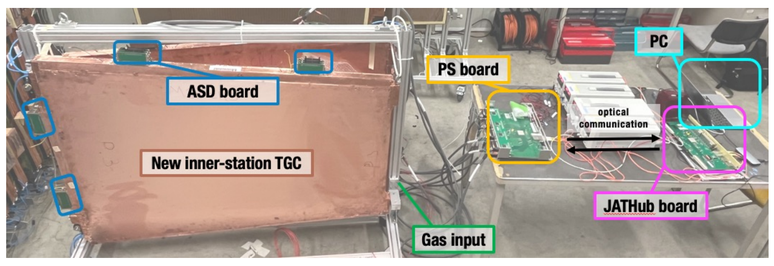

Figure 4: Setup of the experiment

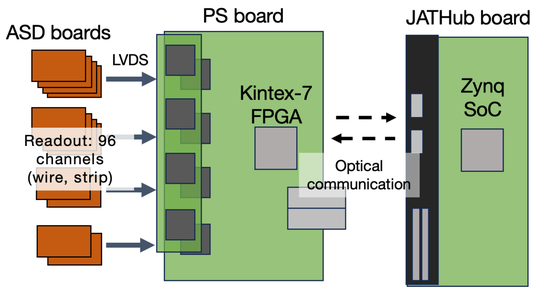

Figure 5: Block diagram of readout

- TGC hits are digitized on the ASD board.
  - Synchronized to 40 MHz by the PP ASIC on the PS board
- Hits are sent to JATHub (Fig. 4).
  - It receives 256-bit hit data from the PS board (Fig. 5)
  - Every 25 ns via optical communication
  - JATHub buffers the received data and its associated timing
  - Receiving the trigger accept signal (L1A), the data are transferred to a FIFO memory
- Data in the FIFO memory are read out by the Processing System of Zynq SoC.

Noise evaluation

Method for measuring

$$\text{Occupancy} = \frac{(\text{Average noise hits of per PP ASIC})}{1176500}$$

- Trigger: Random trigger
- Accumulated data: 1,176,500 events
- Error bars show standard deviation (variation per channel is visible)
- Threshold voltage for ASD boards comparator (Vth = 0-100mV, 10mV steps)

Result for Module 1

- Noise disappears at Vth ≥ 20 mV for wire and Vth ≥ 90 mV for strip
- **It can be operated with the normally used Vth=60 mV for wires.**
  The strips required Vth=90 mV which is slightly higher than the normally used 70mV but acceptable for the operation.

Noise evaluation (continued)

Result for Module 2 (Fig. 6)

- Noise disappears at Vth ≥ 20 mV for wire and Vth ≥ 50 mV for strip
- **It can be operated with the normally used Vth=60 mV and 70 mV for wires and strips, respectively.**

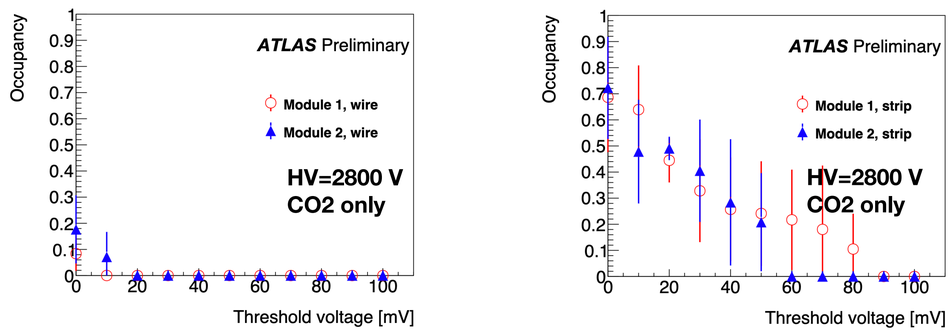

Figure 6: Analysis results of noise evaluation (left: wire, right: strip)

Efficiency evaluation

- Trigger: hits required for at least two layers
- The current TGC detector's efficiency is 92-93%.
- HV=2800 V, Vth=100 mV, CO2 + n-pentane
- Accumulated data: 1,000,000 events

$$\text{Efficiency} = \frac{(\text{Number of hits on all three layers of wires, strips})}{(\text{Number of hits on layer 0 and layer 2 wires and strips})}$$

- **Efficiency: 94.0 ± 0.1% (wire), 92.2 ± 0.1% (strip)**
- The efficiency is consistent with the expectation; the inefficiency is mainly due to the internal support structure (Fig. 7).

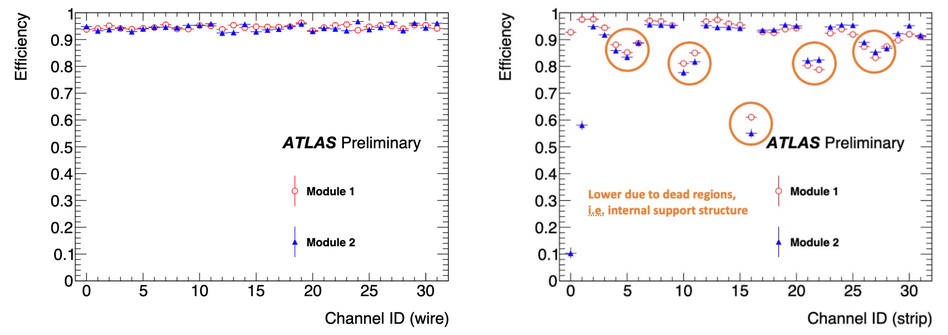

Figure 7: Efficiency in layer 1 when a hit is requested on layer 0 and layer 2 (left: wire, right: strip)

Trigger logic for a new inner-station TGC

- Developed a trigger circuit for the firmware of the trigger and readout board (Fig. 9)
- Designed a 25 ns latency coincidence circuit, treating all proton collisions every 25 ns the same.
- Provides significantly better position resolution (Fig. 8).
- Previously, an OR was taken for 8-channel groups.
- Newer, hits from all channels will be used without grouping.

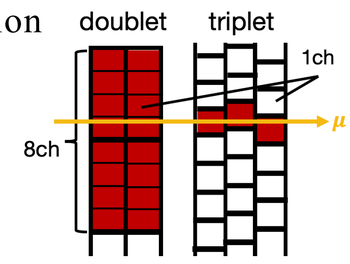

Figure 8: Differences in positional resolution with and without grouping

3 out of 3 coincidence logic

Position 5 = Layer 0 (1) & Layer 1 (2) & Layer 2 (2)

2 out of 3 coincidence logic

Position 5
= (Layer 0(1) & Layer 1(2) & $\overline{\text{Layer 2(2)}}$)
|| (Layer 0(1) & $\overline{\text{Layer 1(1)}}$ & Layer 1(2) & Layer 2(2))
|| ($\overline{\text{Layer 0(1)}}$ & $\overline{\text{Layer 0(2)}}$ & Layer 1(2) & Layer 2(2))

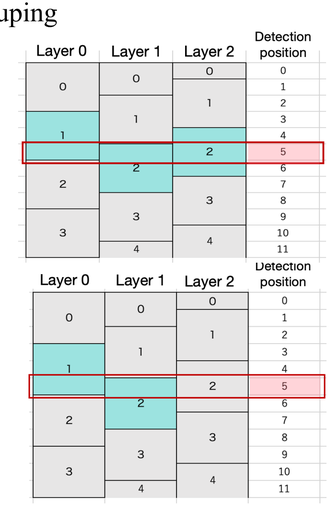

Figure 9: Example of how to take coincidence

Simulation

- The correct output was obtained for 2428 different input patterns without a single bit being wrong.

Summary

- The ATLAS experiment will be upgraded for the HL-LHC to be started in 2029.
- The performance of the new inner-station TGC was evaluated (noise and efficiency) and a coincidence circuit was developed for the first-level trigger.
- The threshold voltages for eliminating noise were 60 mV and 70-90 mV for wires and strips, respectively.
- The efficiency was 94.0 ± 0.1% and 92.2 ± 0.1% for wires and strips, respectively.
- The coincidence circuit for the new inner station TGCs was confirmed with logic simulation.
- Mass production of the chambers and electronics boards is ongoing.

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