Upgrade of the ATLAS Monitored Drift Tube detector for the HL-LHC

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on behalf of ATLAS MDT upgrade group

1. Introduction

ATLAS monitored drift tube (MDT) readout electronics will be upgraded for HL-LHC. In addition, about 100 small-radius MDT (sMDT) chambers have been built to replace the current MDT chambers in the innermost barrel region small sectors (BIS chambers), see Fig 1.

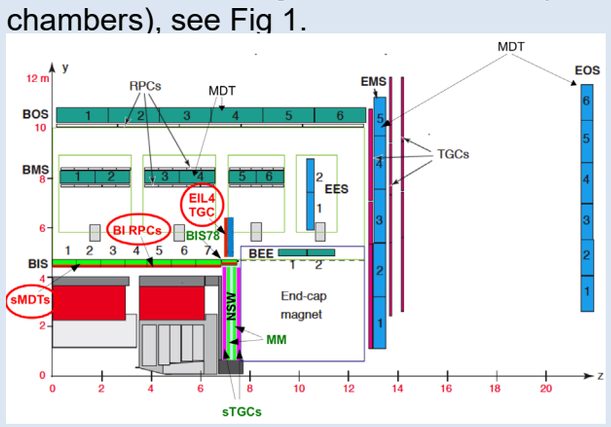


Fig 1. R-Z views of the Phase-II ATLAS muon spectrometer layout (small sector) [1].

2. sMDT Chamber Construction

48 sMDTs built at MPI, 48 sMDTs built at UM and MSU. All chambers passed QA/QC tests and were shipped to CERN BB5.

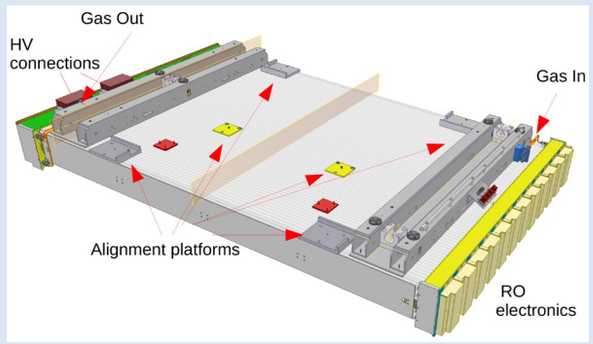


Fig 2. sMDT layout: Two multi-layer, each of 4 tube-layers; Drift tubes diameter 3 cm (MDT) → 1.5 cm (sMDT) [2]

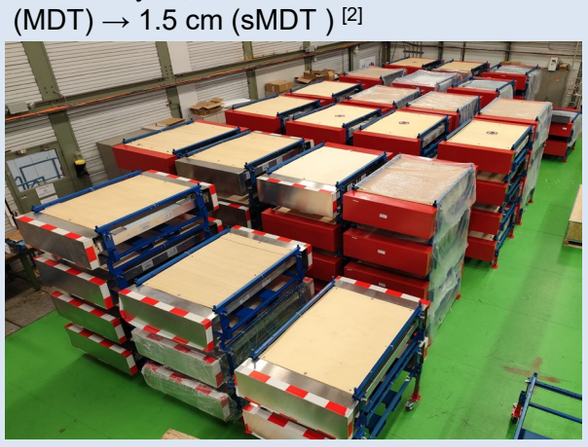


Fig 3. sMDT chambers in CERN BB5

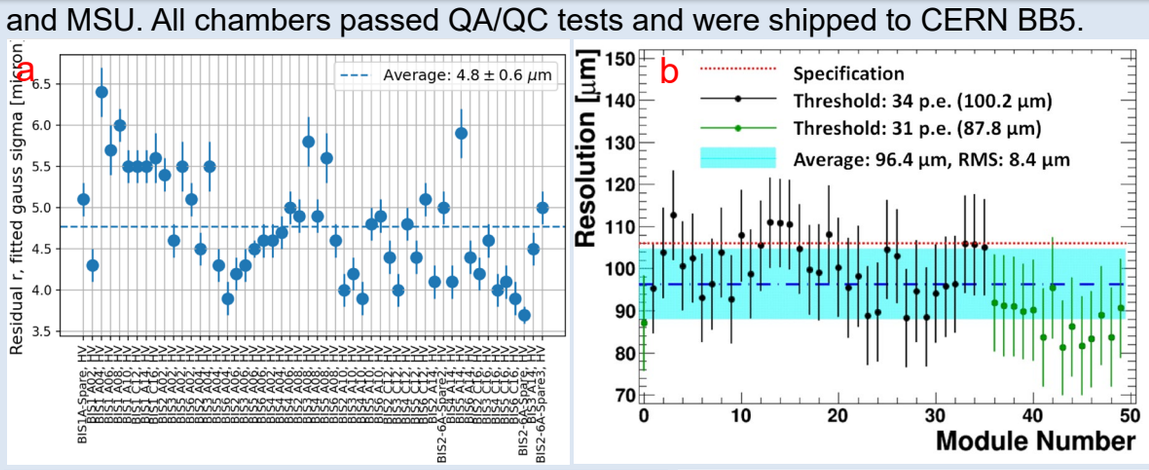


Fig 4 [3]. Wire positioning accuracy on HV side of MPI sMDT chambers (a); Single tube resolution of chambers constructed by UM (b) and MPI (c); Noise results of sMDTs of MPI and UM at -39 mV threshold (d).

3. (s)MDT Electronics

- **Scope**

Signals from each 24 (s)MDT tubes are processed by 3 ASD (Amplifier-Shaper-Discriminator) chips and 1 TDC chip on a mezzanine [4]. A Chamber Service Module (CSM) collects data of up to 20 mezzs and transmits it to the backend. MDT will be used as L0 trigger to improve muon momentum measurement after LS3.

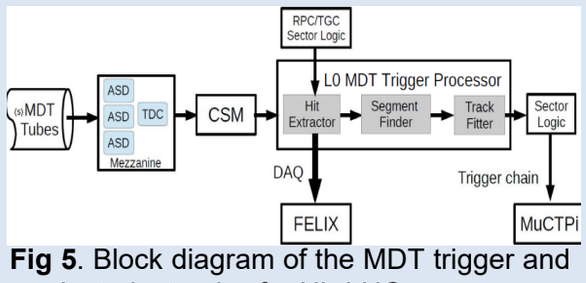


Fig 5. Block diagram of the MDT trigger and readout electronics for HL-LHC.

- **CSM**

✓ 20 mezzanine cards @320Mpbs input
✓ lpGBT (low power GigaBit Transceiver)
✓ 10.24 Gbps output line x2
✓ Temp. & Volt monitoring by GBT-SCAs
✓ Compatible with legacy mezzanines
✓ CSM passed all functionality tests, TID and annealing tests.
✓ Pre-production of CSM is on-going.

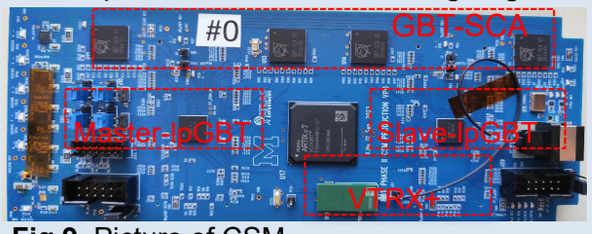


Fig 9. Picture of CSM

- **ASD Chip**

✓ 8 channels, IBM 130 nm CMOS
✓ Charge sensitive amplifier, 3-stage shaper, discriminator, Wilkinson ADC to convert input charge to digital pulse
✓ LVDS output driver (reduced swing)
✓ Tested all ASDs for Phase-2 upgrade

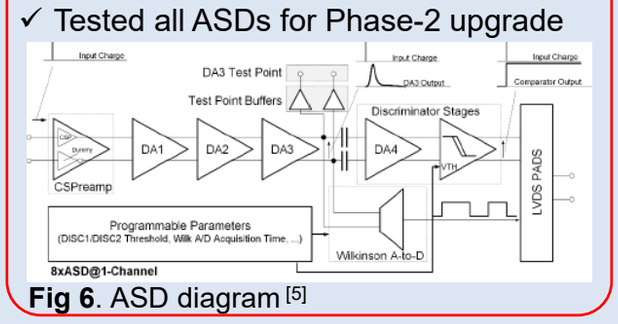
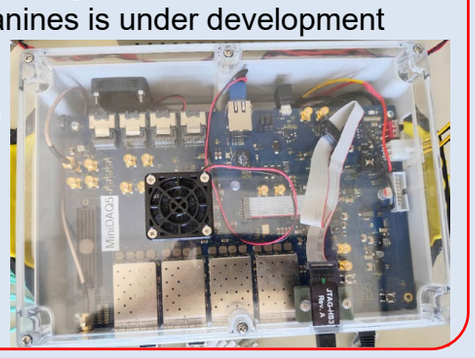


Fig 6. ASD diagram [5]

- **miniDAQ** [6]

✓ Lightweight system to test all front-end electronics & joint tests with chambers
✓ 8x 10 Gbps SFP transceivers, 1x Gbps Ethernet port for data offline storage
✓ Directly configure lpGBTs on the CSM
✓ JTAG configuration for CSM-FPGA and mezzanines is under development

Fig 10. miniDAQ



- **TDC Chip**

✓ 24 channels per chip, 130 nm CMOS
✓ 780 ps binsize, 102us dynamic range
✓ Triggerless mode by default
✓ 320 Mbps x2 output data rate
✓ TMR protections for key modules
✓ Tested enough TDCs for Phase-2

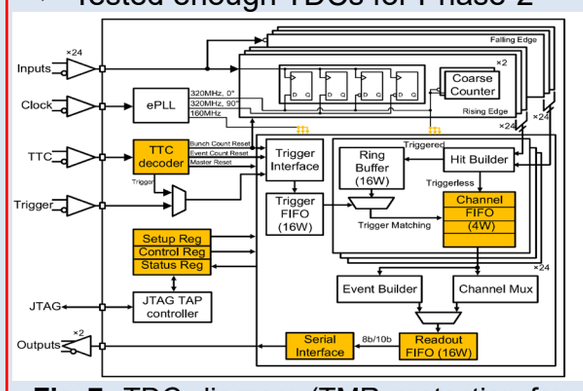


Fig 7. TDC diagram (TMR protection for Orange modules) [4]

- **DAQ Software**

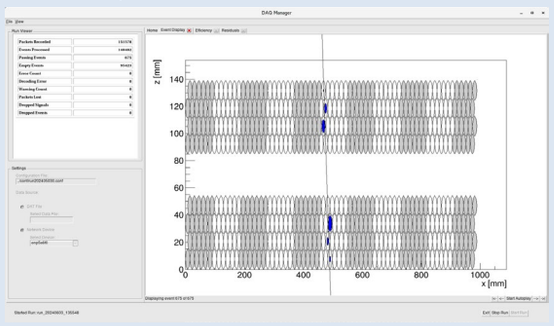


Fig 11. DAQ GUI for online ADC/TDC spectra & event tracking

- **(s)MDT Mezzanine Card**

✓ Each mezzanine card contains 3 ASD chips and 1 TDC chip
✓ Pre-productions are on-going

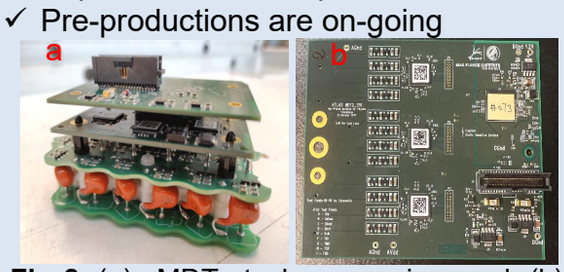


Fig 8. (a) sMDT stack mezzanine card; (b) MDT flat mezzanine card.

- **L0MDT**

✓ L0 MDT-TP includes Service Module (SM) and Command Module (CM);
✓ Interfaces with Sector Logic transceiver and FELIX were demonstrated;
✓ All FE functionalities have been tested;
✓ Recently reliable data taking with the cosmic stand and new FE electronics was demonstrated for first time

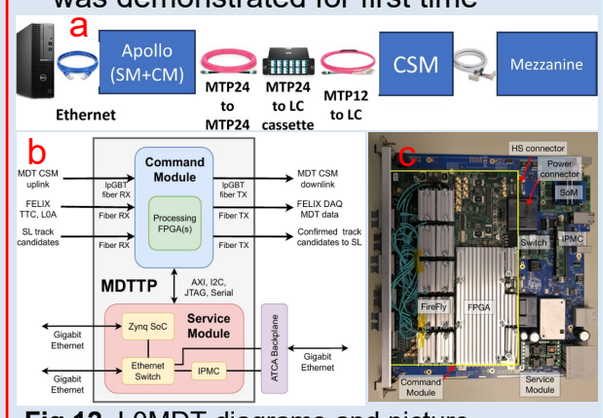


Fig 12. L0MDT diagrams and picture

4. (s)MDT Test Stands

Fig 13. a-b: UM & MPI sMDT test stands in BB5; c: sMDT test stand in UM; d: BIS7 MDT test stand in CERN 188; e: BIS7 MDT test stand in UM; f: BO MDT test stand in LMU.

5. Joint Test Results with sMDT

✓ BIS1A16 sMDT in BB5, Fig 13 (a);
✓ 93:7 Ar:CO_2 at 3 bar, HV at 2730 V;
✓ 10 new stack mezzanines;
✓ ASD main threshold at -28 mV;
✓ Readout by miniDAQ;
✓ Single wire tracking resolution of around 100 μm with an average detection efficiency above 99 %.

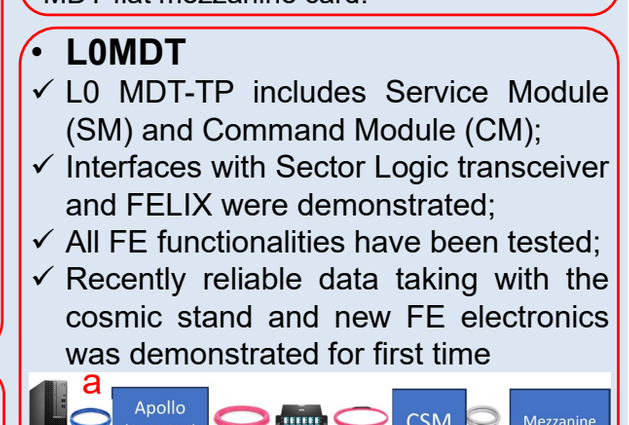


Fig 14. (a) ADC spectra of 10 mezzanines; (b) Hit map; (c) Fitted TDC spectrum of single channel; (d) Auto-calibrated r(t) function

References

[1] ATLAS-TDR-026, CERN (2017).
[2] C. Wei et al., 2022 JINST 17 P10010.
[3] ATLAS Note.ATL-MUON-PROC-2024-003
[4] Y. Liang, et al., NIM A 939 (2019) p10-15.
[5] K. Penski. JINST (2024) 19 C05008.
[6] Y. Guo, et al., NIM A 1046 (2023) 164896.

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