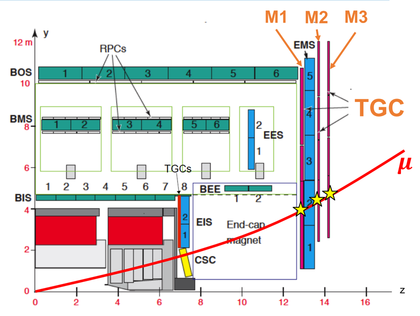
A comprehensive firmware validation machinery for the Level-0 Endcap Muon trigger for LHC-ATLAS Phase2 upgrade

42nd International Conference on High Energy Physics (ICHEP 2024)
18-24 July 2024, Prague

We will report on our study focusing on developing a logical circuit for the Level-0 (L0) Endcap Muon Trigger in the HL-LHC ATLAS experiment. We aim to achieve systematic and efficient firmware validation through a comprehensive study across hardware, software, and databases. Specific approaches include conducting systematic tests using benchmarking artificial track data, high-statistics full-simulation data, and further actual collision data. Our design of the validation system enables systematic tests by coherently injecting identical data in the software simulation environment and actual hardware testbench. Along with the system's design, we have developed a relational database to centrally manage cabling information and data format, as well as a bit-wise simulator of the trigger logic circuit. This presentation will discuss the concepts of the validation system design, specific implementation methods, and experiences gained from test results.

1. TGC Detector and L0 Muon Reconstruction in Endcap

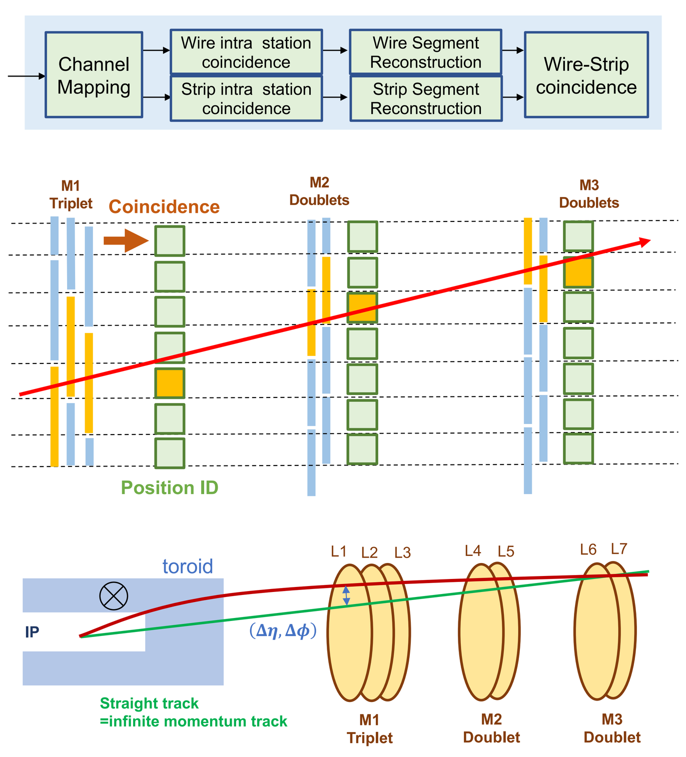


TGC (Thin Gap Chamber)

- High speed gas detector with a short wire interval (1.8mm) and thin gap (2.8mm) for muon trigger in endcap.
  - Measures 2-dimensional position.
- Consists of 7 layers (gas-gaps) in 3 stations
  - The inner most three layers in 1st station "M1", the next two layers in the "M2", and the outermost two layers in "M3" stations, respectively.
  - 320,000 detector channels.

Muon Trigger and the Phase-2 upgrade

- All frontend and backend digital electronics to be replaced and upgraded to cope with ATLAS Phase-2 trigger and DAQ specification with improved performance.
  - The new trigger system performs high-speed track reconstruction with a coincidence logic.
  - Latency for online muon reconstruction using TGC hits (including p_T estimation) from bunch crossing is about 1.5 μs.
  - CTP will make the L0 trigger decision using the L0 muon trigger output.
- In the new trigger system, all TGC hit data are transferred to backend "Sector Logic" (SL) board at every 40 MHz bunch crossing with a fixed latency and exploited by advanced first-level muon trigger based on a fast tracking.



SL trigger calculation process

① **Channel Mapping**
- Convert **bitmap received on serial link** (128 bit × 58 link) to **logical channels** (hits are taken for each of the M1, M2, and M3 stations).
- Developed by the relational database of cabling.

② **Inter Station Coincidence**
- by coincidence of **logical channels,** determine **Position IDs** (M1・M2・M3).

③ **Segment Reconstruction**
- from combining of **Position IDs**, obtain $(\Delta\eta, \Delta\phi)$ which is the difference in position from the infinite momentum track by LUT.

④ **Wire-Strip Coincidence**
- from $(\Delta\eta, \Delta\phi)$, get p_T by LUT.

A system for developing complex trigger electronics is essential and has been designed and developed in this work.

2. Concept of the Validation Machinery & Core Elements

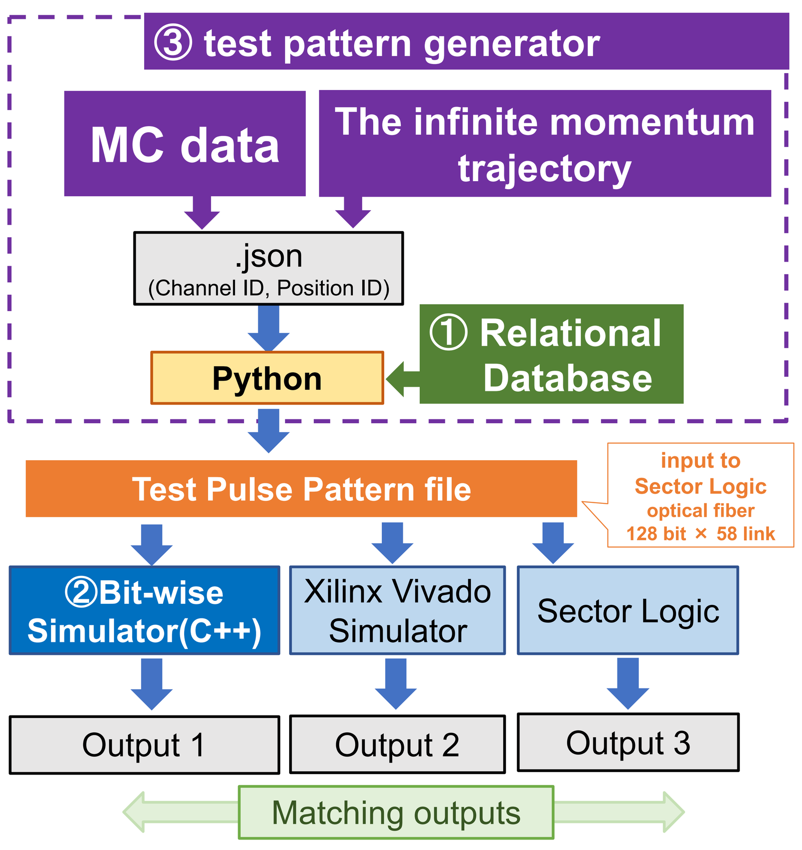
To ensure robust verification, the system provides **common test vectors** coherently for the **hardware testbench**, **firmware simulation**, and **software based simulation**, which allows event by event comparison among the three frameworks.

Three core elements:

1. Relational Database
- Centralize management for knowledge of both the current and Phase2 systems.
  - Systematic handling of the cabling to map detector channels to electronic channels, and input data format from the serial fiber optical links.

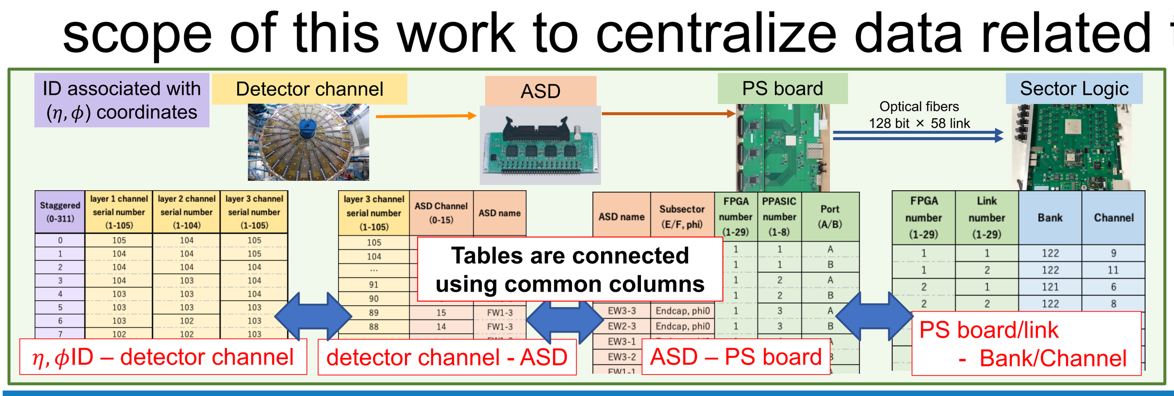
2. Bit-wise simulator
- Use the exact same logic and I/O as SL trigger firmware.

3. Test Vector generator
- Can generate various **test vector**, for example, the infinite momentum trajectory and MC data.
- Use the relational database managing cabling.



3. Relational Database to Manage Cabling

- Implemented as Relational Database using MySQL.
  - The Endcap muon trigger is a complex system with multi-stage and various scales of electronics.
  - Relational database can manage information by connecting minimal tables.
    - A single table describes the one-to-one correspondence of components.
    - Modifications to the table are minimal, even with changes in wiring.
- This database is commonly used in the TGC community beyond the scope of this work to centralize data related to TGC.



Scale of channels and electronics count at Phase2 TGC system

Detector channels	320k
ASD (Amplifier - Shaper - Discriminator)	~23k
PS board (Primary ProcesSor board)	1434
SL (Sector Logic)	48
optical fiber(between PS board - SL)	4k

4. Bit-wise Simulator

A simulator in C++ to emulate the firmware behavior in software.

- Utilize the same logic at the bit level as the firmware.
  - Bitwise calculations instead of float approximations.
- Mirror the same structure as the firmware.
  - The simulator's logic is divided into calculation blocks with the same processes and areas as the firmware.
- Can output results for each SL trigger calculation process (① ~ ④).
  - Verification step by step for each integration test.

5. Preparation of test vector

A generator creates test vector input for both the SL and the simulator.

- Convert hit data to bitmap received on serial link (128 bit x 58 links)
- The following two inputs are particularly useful, and the machinery for production of test vectors from these inputs has been developed.

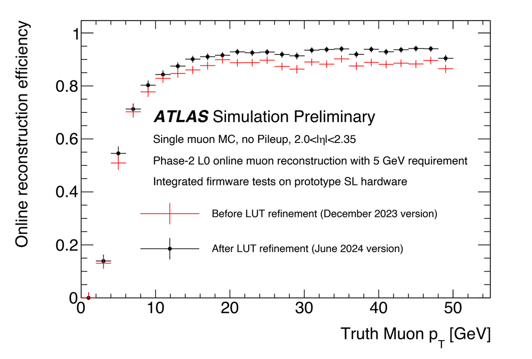
A) The infinite momentum trajectory
- Mechanism to specify (η, ϕ)-ID for the input test vector.
- Generate the simplest infinite momentum linear track.

B) MC data
- Mechanism to extract a channel list from the root file, starting with MC/actual collision data and to create the input test vector from it.

6. Hardware tests with high statistics test vectors

This system is already in use.

- **The infinite momentum trajectory** is used as first verification.
  - e.g. LUT verification by plotting the efficiency of all M3 channels.
- **MC data** is used in hardware test.
  - Prepared input test vectors (MC data) for SL hardware and the bit-wise simulator using the generator.
- Enable to perform highly accurate comparisons between the outputs of SL and bit-wise simulator.
  - These results are used for developing LUT, firmware optimization, HDL code debugging, etc.
  - The right plot shows the improved efficiency achieved by testing this system.



The improvement in the performance of the online muon reconstruction in the Level-0 muon trigger electronics

7. Conclusion

- Designed the entire SL trigger verification system for the Phase2 upgrade of L0Muon and developed its components, including:
  - Relational Database
  - Bit-wise simulator
  - Test pattern generator
- The verification system is actively used for SL development research.

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← You can find the details of the plots seen in Sec 6.

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