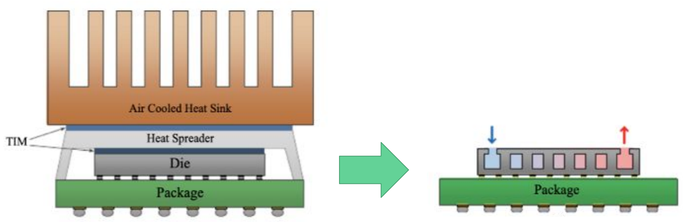
Liquid-based micro-channeling for efficient FPGA cooling

G. Baldinelli, M. Boscardin, F. Bosi, A. Coccaro, M. Crivellari, P. Francavilla, P. Mammini, M. Massa, F. Palla, C. Turrioni
on behalf of the INFN Perugia, Pisa and Genova and FBK Cool FPGA group

MOTIVATION FOR MICROCHANNELS ON THE SURFACE OF THE DIE



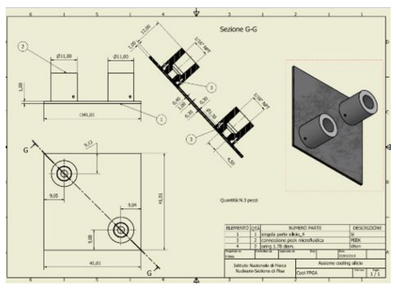
Embedded cooling technologies for densely integrated electronic systems
2015 IEEE Custom Integrated Circuits Conference (CICC)
https://ieeexplore.ieee.org/document/7338365

- **More efficient cool down** (e.g. high surface/volume ratio, low thermal resistances between the fluid and the circuit dissipating power)
- **Less obstruction for air-based cooled components**
- **It overcomes limitations of high density PCB**

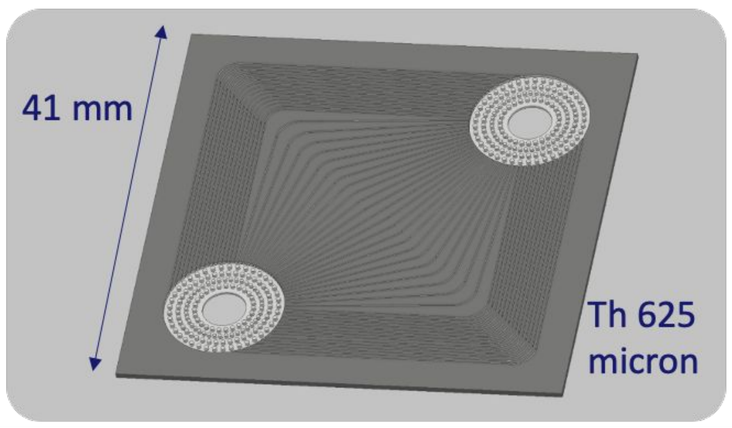
CONS:

- **Risks due to manipulation of the bare die**
- **Probably less suitable for large scale systems** (in case we need to manipulate O(1k) devices)

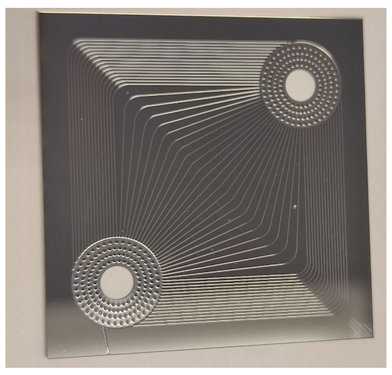
THE COOLFPGA APPROACH



- Silicon - DRIE process:
  - **XILINX** KINTEX ULTRASCALE XCKU040
  - **INTEL** STRATIX 10 MX
- **Specific peek connection** by **Cole-Parmer Company** on a test structure
- Tested Plugs in **silicon** and **pyrex**



THE PROTOTYPES



LIQUID PRESSURE TESTS

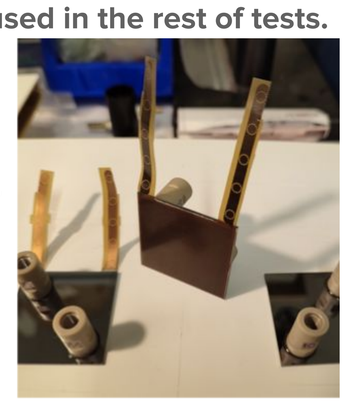
DOUBLE SHEET OF SILICON

Load and breaking tests with pressurized liquid demonstrated extreme fragility of the bond between the two layers of silicon. **Silicon double layer solution has been abandoned.**

SILICON-PYREX (300 µm) type
Demonstrated good behaviour at the test. **SILICON-PYREX solution used in the rest of tests.**

Samples equipped with

- heaters for the simulation of electronics,
- glued with **Masterbond EP30TC**, a thermally conductive glue.



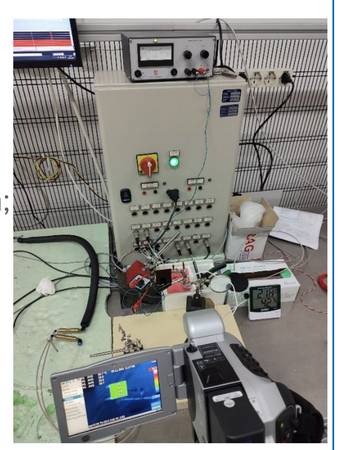
THERMAL TESTS

SETUP

- Temperature detected with an **infrared camera** at a distance of 30 cm;
- **External temperature = 21.4°C;**
- **Relative humidity = 51%;**
- **Sample emissivity = 0.96.**

POWER TEST

- Samples 4x4 = 16 cm^2;
- Cooling liquid: **Novec 7100 at 5°C,** mass flow rate=0.33 kg/min;
- Voltage and current increased to reach the desired dissipated power.

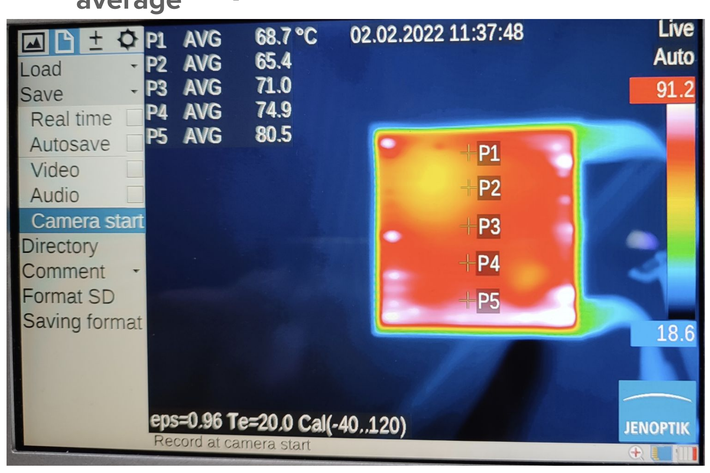


RESULTS

Tested 1-6 W/cm^2

- Results with 6 W/cm^2
- Theoretical Power: **96 W**
- 51.9 V; 1.87 A = **97.1 W** real
- Liquid pressure:
- **Inlet 3.42 bar; Outlet -0.02 bar**

$T_{average}$ 5 points hot side: 72.1°C

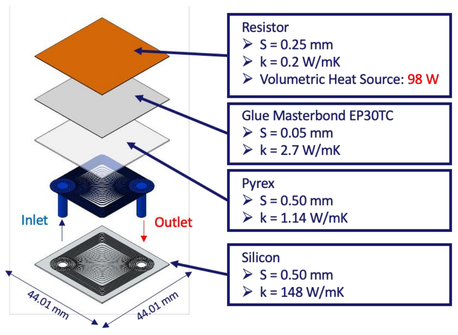


SIMULATIONS

Novec 7100
- ρ = 1510 kg/m^3
- µ = 0.00058 kg/(m·s)
- C_p = 1183 J/(kg K)
- k = 0.069 W/mK
- Laminar flow

Inlet:
- Velocity Inlet
- V_{in}= 0.29 m/s*
- T_{in}= 5°C

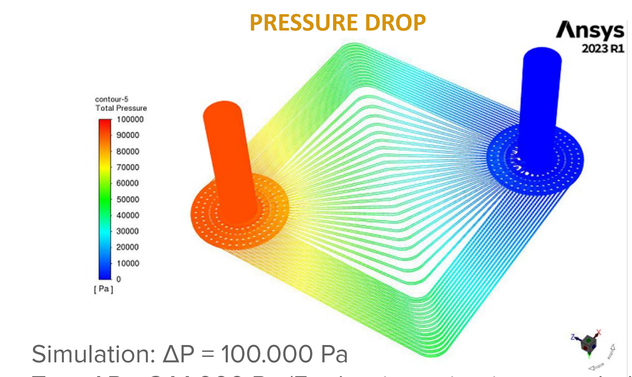
Outlet:
- Pressure Outlet



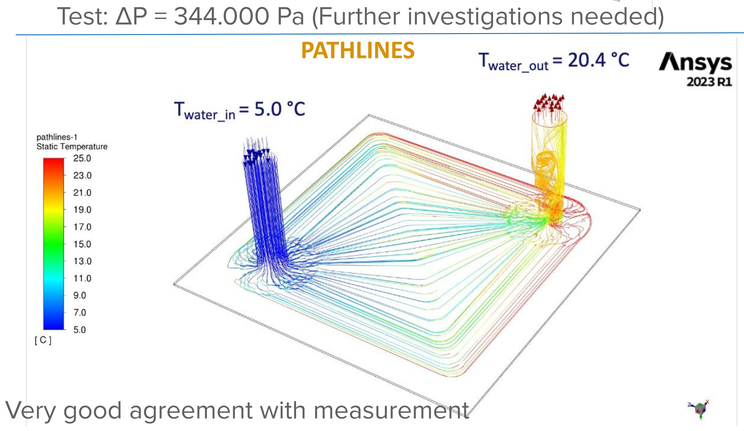
- Total volume for the model is 2.23 cm^3
- Each channel must be divided into a fairly large number of cells.
  - The width of the channel is the smallest dimension, equal to 0.1 mm.
- Would need ≃$2{\cdot}10^9$ cells with 0.01 mm edge, not sustainable by calculators.
  - Elongated parallelepiped instead of cubes where possible
  - Bigger element size in the silicon volume.

7'060'226 cells are created in the grid

SIMULATIONS - RESULTS

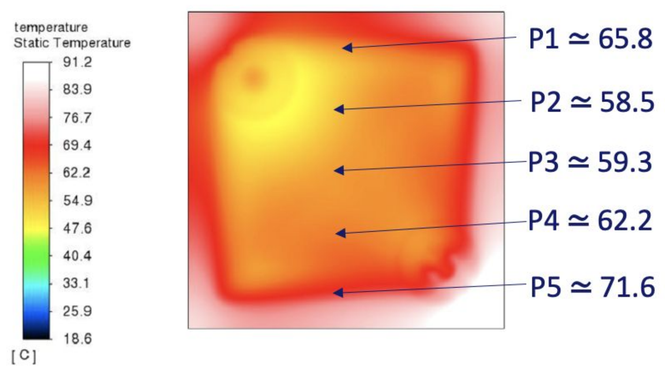


Simulation: ΔP = 100.000 Pa
Test: ΔP = 344.000 Pa (Further investigations needed)



Very good agreement with measurement

SIMULATIONS - RESULTS



CONCLUSIONS

- Tests on the performance of microchannels on the surface of the die;
  - Fragility of the bond between the two layers of silicon;
- **Good performance tested up to 6 W/cm2.**
- **Preliminary CFD simulations** repeated in the same conditions
  - Good agreement with data (investigation ongoing for the pressure drop)
- **Future investigations on different geometries** for microchannels path (easier) and their shape (harder), trying to go to higher heat fluxes.