



STCF Detector Design and R&D

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On behalf of the STCF detector group

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Super Tau Charm Facility (STCF)



- $E_{\rm cm}$ = 2-7 GeV, $\mathcal{L} > 0.5 \times 10^{35}$ cm $^{-2}$ s $^{-1}$
- **Potential for luminosity upgrade and a polarized** electron beam
- Site: Suburban "Future Big Science City" in Hefei
- 14th five-year plan (2021-2025): Design studies and R&D on key technologies, ~0.4 B CNY
- 15th five-year plan (2026-2030): Construction to start during this period, ~6 years, ~4.5 B CNY
- Operating for 15 years to be followed by major upgrades

For more information about the STCF project, please see https://indico.cern.ch/event/1291157/contributions/5890162/



STCF can produce an enormous amount of "clean" tau leptons and charm hadrons, allowing a full exploration of the unique and great physics potential in the tau-charm energy region: QCD, exotic hadrons, flavor physics and CPV, new physics...

STCF Detector Layout



Physics Requirements

Requirements

- Highly efficient and precise reconstruction of exclusive final states produced in 2-7 GeV e+e- collisions
 - ▶ Precise measurement of low-p particles (<1GeV/c) → low mass</p>
 - **Excellent PID**: π/K and μ/π separation up to 2 GeV

Physics Interest

Process

Optimized







Beam-induced Backgrounds



Inner most detector layer: ~3.5 kGy/y, ~2×10¹¹ 1MeV n-eq/cm²/y, ~1 MHz/cm²

The major challenge is to maintain or even enhance the state of the art performance of τ -**c** detectors in much harsher experimental conditions.

STCF Detector Conceptual Design



- Inner tracker (ITK, two options)
 - MPGD: cylindrical MPGD
 - Silicon: CMOS MAPS
- Central tracker (MDC)
 - Main drift chamber
- * PID
 - Barrel: **RICH** with CsI-MPGD
 - Endcaps: DIRC-like TOF (DTOF)
- ✤ EMC
 - pure Csl + APD
- Muon detector (MUD)
 - RPC + scintillator strips
- * Magnet
 - Super-conducting solenoid, 1 T

STCF Physics & Detector CDR

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Tracking System : ITK + MDC



Inner-outer separate designs to accommodate different levels of radiation background

PID, EMC, MUD

 Barrel PID: A RICH detector using MPGD (THGEM with CsI + MM) for photon detection



Material budget < 0.3X₀

 Endcap PID: A DIRC-like high-resolution TOF detector (DTOF ~ 30ps), quartz plate + MCP-maPMT

EMC: A pure-CsI crystal calorimeter to tackle a high level of background (~1MHz/ch)



- Crystal size
 28cm (15X0)
 5×5cm²
- ~ 8670 crystals
- 4 large area APDs (1×1cm²) to enhance light yield
- MUD: A RPC-scintillator hybrid detector to optimize muon and neutral hadron ID



Expected Performance





Pion/K separation capability



Photon energy resolution



Photon position resolution



Muon identification efficiency



STCF R&D Project Kick-Off and Review Meetings





Kick-off Meeting, Aug. 2023, USTC More than 30 academicians of CAS, as well as government officials of Anhui province and Hefei city, along with representatives from various domestic research institutions, totaling 170 attendees. **R&D Project Review, Dec. 2023, USTC** Organized by Development and Reform Commissions of Anhui province and Hefei city. The R&D project was approved for a budget of 364 M CNY and is jointly funded by Anhui, Hefei and USTC.

ITK-MPGD: μRGroove

 μRGroove : A single-stage MPGD involving no stretching or tensioning, 2D strip readout without charge sharing (large S/N), high rate with fast grounding, easy to make a cylinder, low mass, low production cost



• High-rate readout ASIC for MPGD (averaged hit rate of 400 kHz/ch)



ASIC Specs	Demands	
Charge Range	40 fC	
Charge precision	\sim 1 fC RMS	
Time precision	< 10 ns RMS	
Max. event rate	4 MHz	

ITK-MPGD R&D

Development of low mass electrodes





Fabricating cylindrical structure



ASIC design and development



3.9999971 MHz

7.105 ns

detector output pulses to the chip at 4MHz with 35pF

Inner Layer Prototype

- Built a cylindrical µRGroove prototype for the ITK inner most layer
- Tested the prototype with ⁵⁵Fe source in lab and SPS muon beam at CERN
- Effective gain~5000-10000 for most sectors
- Spatial resolution < 100 um and efficiency > 95%
- The detector design and fabrication will be optimized in many aspects based on the prototyping experience







ITK-MAPS

- Aiming for a low-power MAPS chip design (required for a low-mass system) with timing and charge measurement capability: position, time and charge (TOT)
- Low mass outweighs position resolution: exploring large pixel size to reduce power density

ullet



Super Pixel Design

- Combining non-adjacent pixels: avoid ToT loss
- Super pixel with 6×12 pixel array
 - 6 sets of digital readout logic
 - When cluster size < 3X4, no ToT loss occurs



Combining adjacent pixels

 \rightarrow ToT loss



Providing both high position and high time resolutions for low power consumption

Additional 3-bit for group address

ITK MAPS Designs



NexChip FCIS/BCIS 90nm Taped out in May 2024 Services Services Chip2 Chip3 Chin Chip2 to be taped out in July 2024



Simulated performance

	TJ-MAPS	GSMC-MAPS	
Current	800 nA/pix	120*6 nA/pix	
Supply Voltage	1.8 V	1.2 V	
Threshold	309.0 e⁻	153.8 e⁻	
ENC	11.4 e⁻	5.1 e⁻	
Mismatch	5.7 e⁻	5.8 e⁻	
<i>t_r</i> @400 e ⁻	200 ns	81 ns	

Power	Notes	
consumption		
~26 mW/cm ²	Strip-based	
~15 mW/cm ²	Pixel-based	
12.2 mW/cm ²		
2.4 mW/cm ²	with a data rate of 8.7	
	MHz/cm ²	
23.5 mW	32MHz event rate	
39 mW	x 2 data/clock output	
20 mW		
222.6 mW	Strip-based	
184.6 mW	Pixel-based	
	Power consumption ~26 mW/cm ² ~15 mW/cm ² 12.2 mW/cm ² 2.4 mW/cm ² 23.5 mW 39 mW 20 mW 222.6 mW 184.6 mW	

- Strip-based: 55.7 mW/cm2

- Pixel-based: 46.2 mW/cm2

Main Drift Chamber

- Preliminary mechanical design and structural analysis
- Big challenges from super-small cells (5mm*5mm, distance between wires ~2.5mm)
- Ongoing R&D on feedthroughs, wires and chamber stringing











MDC Readout Electronics

- Challenge: irregular pulse signals overlapping at high rates
- Attempt to separate overlapping pulses with waveform digitizing readout. A lot of effort on separation algorithm development and readout optimization.
- Developed readout circuit with discrete components (TIA + shaper + ADC). ASIC design also underway.

Optimized ADC specs: 14 bit, sampling rate 125 MSPS, bandwidth 650 MHz









Readout board (16 chs) being tested

PID Barrel: RICH Detector R&D

Fabrication of 30cm*30cm RICH prototype



Cosmic-ray tes



Very weak light observed Investigation ongoing



Measured OE @ 0V offset

Measured QE @ 9V offset Provided OE

250

Wave length / nm

Measured OE @ 7V offset, retry



Radiator purifying



CsI coating and QE measurement



RICH Readout ASIC

Design specs: $\sigma_t < 1$ ns @20fC&20pF, event rate ~ 100 kHz, 32 channels





Test results



5

10

Input rate per channel (kHz)

Design iterations



Second version





512-channel readout board using the self-developed ASIC



Design with 64 channels is underway

PID Endcap: A full-sized DTOF prototype







组装清洗装置





放入超声水箱

Quartz radiator cleaning

and mounting

吊装搬运晶体

人工搬运至洁净间

5000



招声清洗

Dtof-SpeT

Entries

Std Dev

 χ^2 / ndf

0q

Mean

73093

-1.562

86.49

484.7 / 70

 63.3 ± 0.3

5096 ± 26.2

1.745 ± 0.281

131.1±14.8

 -12.1 ± 6.4

 173.2 ± 7.0

200F

180F



Dtof-SpeT



Cosmic-ray test

Detector assembling



搬运至宇宙线测试平台







安装柔性背板

用吸盘将晶体放入清洗装置

晶体侧边涂黑





洁净室拆卸清洗装置

- 灵敏面积: 23×23 mm² 4×4 阵列
- 像素大小: 5.5×5.5 mm²
- 响应范围: 200-850 nm

· 博兰非均匀性 14% (σ/u)

- 量子效率: 25%@λ=400 nm 单光子灵敏
- 高增益: >106



See https://indico.cern.ch/event/1291157/contributions/5888464/ for details

single photon time resolution



Single track time resolution

DTOF R&D on MCP-maPMT and Readout ASICs

ALD 厚度: D2

8000

10000

- **MCP-maPMT: a critical component of** the DTOF technology
- **Designed and produced 1-inch MCP**maPMT with 16 annodes, TTS < 40 ps
- Intensive R&D on techniques (ALD and electron scrubbing) to produce long-life MCP-PMT (target >10 C/cm²)

- Two ASICs designed for MCP-maPMT readout.
 - FET (to be taped out in July) ~ 15 ps
 - TDC (taped out) ~ 15 ps









Application of DTOF in Barrel

- Conceptual design of barrel PID based on the DTOF technology
- Design optimization by scanning a variety of key design parameters
- Performance with full simulation mostly meet PID requirements
- More studies and work are planned



MCP-PMT

pCsI EMC : Light yield and timing studies

A major R&D task : enhancing light yield



pCsI EMC : Pileup mitigation and electronics

■ Waveform fitting to remove pileup noise (~1 MHz/ch) and extract signals



Development of waveform digitization electronics (CSA + shaper + ADC)





Dynamic range: 3 MeV ~ 3 GeV ENE: ~ 0.4 MeV Time resolution : < 150 ps@1GeV

5×5 pCsI EMC Prototype



















MUD R&D

• Fabrication and performance studies of large-sized scintillator strips and glass RPC



 Design of readout ASICs (FEE +TDC) is underway. Readout electronics with discrete components has been developed for detector testing and characterization







Trigger and DAQ

Physics event rate ~ 400 kHz



Component	Num. of channels	Readout time window	Event size (B)	Total (B/s)
ITK (Silicon)	50M	500 ns	14300	5.72G
ITK (µRWELL)	10552	500 ns	17232	6.89G
MDC	11520	$1 \mu s$	20400	8.16G
PID (RICH)	518400	500 ns	15600	6.24G
PID (DTOF)	6912	500 ns	7380	2.95G
EMC	8670	500 ns	15000	6.00G
MUD	41280	500 ns	262	105M
Total(Silicon)	50.6M	-	72.9k	29.2G
Total(µRWELL)	594k	-	75.9k	30.4G

Raw data rate > 200 GB/s , triggered data rate ~ 30 GB/s



Trigger Algorithms and hardware Development

- MDC 2D and 3D tracking algorithms, EMC clustering algorithms, global trigger algorithms.
- PFGA programming to realize the algorithms







Design of trigger electronics and development of core hardware components





DAQ Software Design and Hardware Development

FPGA XCKU115

板 载DDR4

0

- Software and firmware architecture based on Data-Matrix: flow processing, heterocomputing, standard interfaces and protocols, global pipeline
- Development of core electronics boards: CROB-PXI, CROB-PCIe, FMCP optical interface board



CROB-PXI board FMCP interfa

FMCP optical interface board









FPGA KU15P-1517 → 板上光模块

Clock and Data Transmission

 Master-slave clock distribution scheme : ~ 5ps









TIA跨导接收芯片单通道模拟核心基本完成



Clock management block

Test Beam Campaign

DTOF and EMC prototypes are combined in a single TDAQ system for test beams The past two months were a frenzy of preparing and tunning the combined system, and packaging everything.









Starting from July 31 Lasting for 2 weeks CERN PS T9 beam line

Offline Software of Super Tau-Charm Facility (OSCAR)

- OSCAR is based on light-weight and flexible SNiPER framework and adopted some state-of-the-art software and computing techniques
 - Podio for Event Data Model
 - DD4hep for detector description
 - TBB for multi-threading
 - ONNX for machine learning
- Established the Full Chain of the STCF offline data processing





Architecture of OSCAR: three layers

Summary

- STCF detector conceptual design studies in the past few years have culminated with the publication of the physics and detector CDR.
- The STCF project has moved on to the technology R&D stage with strong support from local governments and USTC. A full STCF R&D program has been established and is rapidly moving forward.
- Intense R&D activities are underway on the baseline detector concept targeting key technologies of all sub-detectors. Significant progress has been made and some systems have reached milestones.
- It is crucial to expand collaboration and explore synergies with other projects.

Thank you !