DRS4 based SiPM readout electronics for the Cosmic Muon Veto Detector at IICHEP

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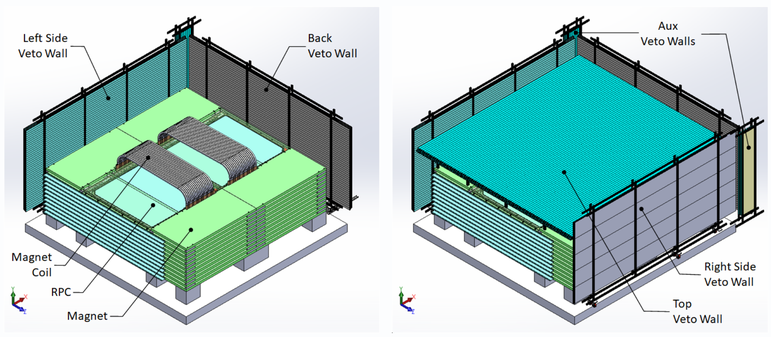
Introduction

A cosmic muon veto detector (CMVD) is being built around the mini-ICAL detector at the IICHEP, which aims to study the feasibility of building a muon veto for a shallow depth neutrino detector. For this, it needs to have a muon detection efficiency $> 99.99\%$ & false positive rate $< 10^{-5}$. The CMVD consists of veto walls made of extruded plastic scintillator (EPS) strips.

The proper identification of muons requires SiPM charge measurement. SiPM signals are converted to voltage pulses by trans-impedance amplifiers. A DRS4 based readout system is being designed to sample the signals at a rate of 1 GS/s. The samples are digitised on receiving an external trigger generated by RPC signals in the mini-ICAL, and zero suppressed data are transmitted to the back-end data server. An FPGA based Data Acquisition (Daq) board consisting of 5 DRS4 ASICs and a network interface is being designed for this purpose.

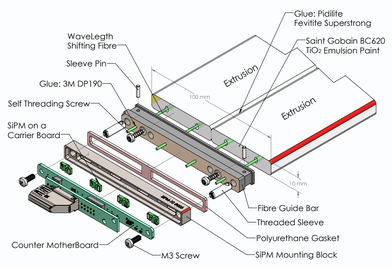
The Mini-ICAL + CMV Detector



The mini-ICAL detector shown partially and fully covered by the veto walls

EPS & Di-Counter

EPS Strips



Di-counter assembly

DAQ Requirements

The CMVD Daq will be required to tag every muon passing through it. This task and can be simplified, by requiring the Daq to tag only those muons that triggered the mini-ICAL's Daq system, since the mini-ICAL won't be able to record every muon because of its dead time. Muons can be identified reliably by measuring the charge value of the muon signal in the SiPMs of the corresponding scintillators, at least during the intial phase.

Thus, the CMVD Daq system should record the charge collected by the SiPMs whenever there is a trigger in the mini-ICAL system.

The CMVD will require 380 di-counters, with each DC having 8 SiPMs, 4 on each end. Therefore the Daq system needs to cater to 3040 SiPMs.

Can We Use DRS4?

Charge measurement of muon signals generated by the SiPMs requires the Daq to integrate the signal for a specific time period, after identifying the arrival of a muon through a trigger. This is non-trivial since the muon signal which generates the trigger, is already lost due to the trigger generation delay. This problem can be overcome either by the use of delay lines, or having a device with analog memory to store the pulse profile. With DRS4 we are looking at the latter option.

A typical SiPM signal for a muon, after amplification has a rise time of $8 - 10$ ns, amplitude of about $10 - 1000$ mV & pulse opening up to 150 ns. A pulse with 8 ns rise-time can be reliably sampled at a frequency of 1 GHz, & with 1024 cells, a DRS4 channel can store pulse profile for the last 1024 ns. This history is long enough to accommodate a trigger latency of 300 ns & pulse profile time of 300 ns. The DRS4 can accept a maximum input of 1 V & the front-end amplifier gain can be adjusted to cover the full dynamic range.

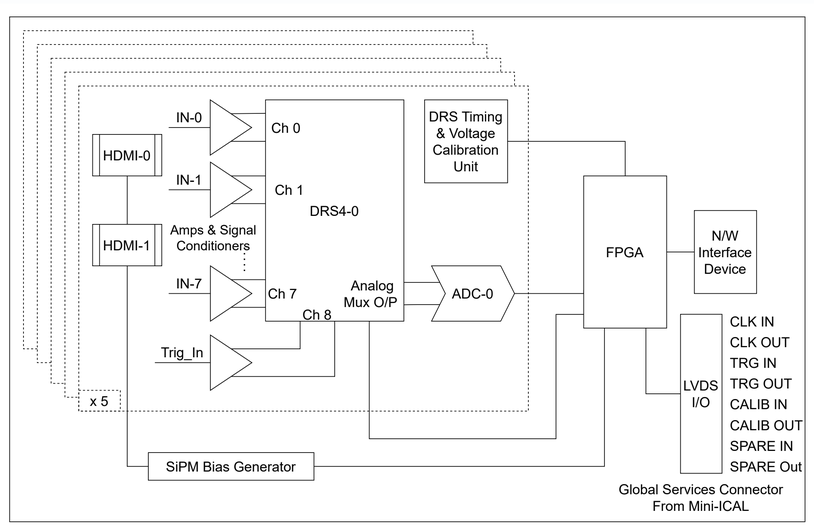
Principle of Operation

The DAQ system has to measure and store the value of the charge produced by every relevant SiPM in the CMVD on every mini-CIAL trigger. For doing this we use the DRS4 chip for sampling the SiPM signal. The DRS4 is a switched capacitor array which can sample 8 input channels at up to 5 GSa/s and store the input analog waveform in 1024 cells per channel. Whenever required the DRS4 can be stopped to readout this stored waveform for external digitization. Thus, at any point of time we can readout the last 1024 ns of the analog waveform if we are sampling the input channels at 1 GSa/s.

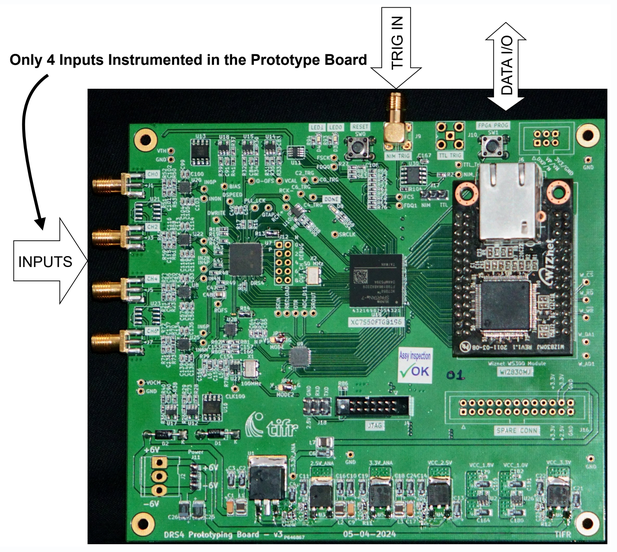
Upon a mini-ICAL trigger, the DAQ boards will stop the DRS4 sampling process and readout the stored waveform for digitization, so that the status of the SiPM during the trigger can be read and stored if found relevant. Since the trigger latency can be measured, the DAQ can readout only the region of interest (ROI) from the 1024 ns of the stored waveform. The ROI will be adjusted to have the full pulse width of the SiPM signal for a typical muon event, plus some overhead to accommodate the jitter owing to the 4.7 m long plastic scintillator, the trigger latency and some part of the waveform before the pulse to determine any baseline offset. The stored digitized data will be processed online in the FPGA to perform baseline offset correction and zero suppression to reduce the data size. It can be further processed to find the charge value of the SiPM pulse so as to reduce the data size by a factor of about 100.

DRS4 Based DAQ board for the CMVD

Following is the block diagram of a DRS4 based Daq board for the CMVD. A prototype of the same has been made around a Xilinx Spartan-7 FPGA. The final DAQ board will cater to 40 SiPM channels and will therefore, incorporate 5 DRS4 chips. The front-end is a trans-impedance amplifier with a common-base transistor front followed by an op-amp stage.

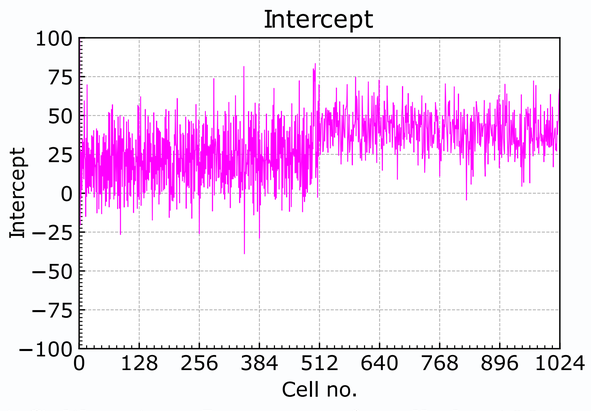


DRS4 based SiPM-DAQ Board Block Diagram for the CMVD

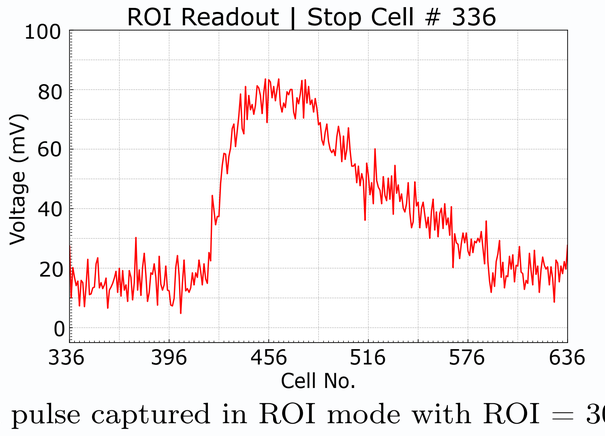


Prototype of DRS4 based DAQ Board using a Xilinx Spartan-7 FPGA

Results



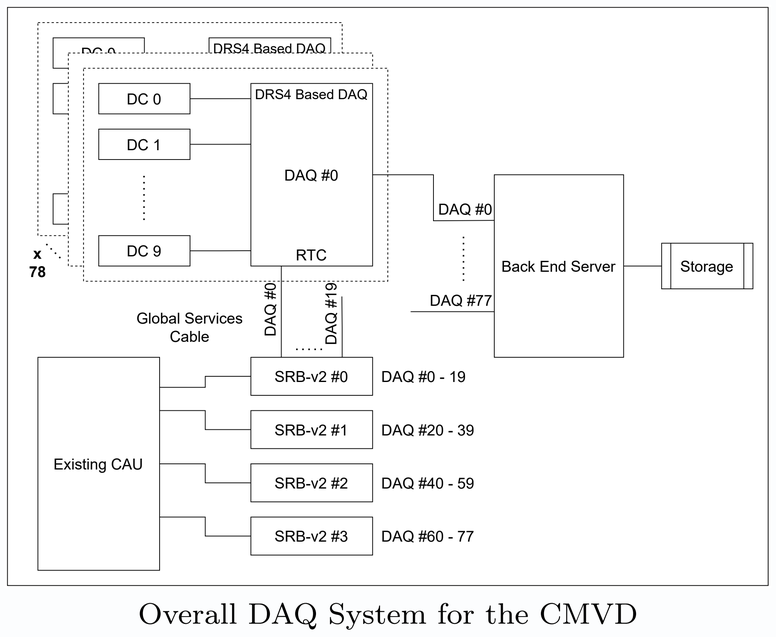
DRS4 Calibration: Intercepts for all the 1024 cells of channel 3



A tail pulse captured in ROI mode with ROI = 300 ns

Further Work

The prototype board is working successfully. This work can now be expanded to the final Daq board which will have 5 DRS4 chips for catering to 40 SiPMs. About 78 such boards will be required for the full instrumentation of the CMVD. The figure below shows a simplified block diagram of the overall Daq system for the full CMVD.



Overall DAQ System for the CMVD