

Intelligent pixel detectors: towards a radiation hard ASIC with on-chip machine learning in 28nm CMOS

Saturday 20 July 2024 09:04 (17 minutes)

Detectors at future high energy colliders will face enormous technical challenges. Disentangling the unprecedented numbers of particles expected in each event will require highly granular silicon pixel detectors with billions of readout channels. With event rates as high as 40 MHz, these detectors will generate petabytes of data per second. To enable discovery within strict bandwidth and latency constraints, future trackers must be capable of fast, power efficient, and radiation hard data-reduction at the source. We are developing a radiation hard readout integrated circuit in 28nm CMOS with on-chip machine learning for future intelligent pixel detectors. We will show track parameter predictions using a neural network within a single layer of silicon and hardware tests on the first tape-outs produced with TSMC. Preliminary results indicate that reading out featurized clusters from particles above a modest momentum threshold could enable using pixel information at 40 MHz.

Alternate track

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Authors: YOUNG, Aaron (Oak Ridge); BEAN, Alice (The University of Kansas (US)); BADEA, Anthony (University of Chicago (US)); P ARPILLON, Benjamin (Fermi National Accelerator Lab. (US)); SYAL, Chinar (Fermi National Accelerator Lab. (US)); MILLS, Corrinne (University of Illinois at Chicago (US)); WEN, Dahai (John Hopkins University); BERRY, Douglas Ryan (Fermi National Accelerator Lab. (US)); FAHIM, Farah (Fermilab); Ms PRADHAN, Gauri; DI GUGLIELMO, Giuseppe (Fermilab); DICKINSON, Jennet Elizabeth (Fermi National Accelerator Lab. (US)); Ms YOO, Jieun (UIC); HIRSCHAUER, Jim (Fermi National Accelerator Lab. (US)); DI PETRILLO, Karri Folan (University of Chicago); GRAY, Lindsey (Fermi National Accelerator Lab. (US)); VALENTIN, Manuel; NEUBAUER, Mark Stephen (Univ. Illinois at Urbana-Champaign); SWARTZ, Morris (Johns Hopkins University (JHU)); TRAN, Nhan (Fermi National Accelerator Lab. (US)); MAKSIMOVIC, Petar (Johns Hopkins University (US)); LIPTON, Ronald (Fermi National Accelerator Lab. (US)); KULKARNI, Shruti R (Oak Ridge National Laboratory)

Presenter: BADEA, Anthony (University of Chicago (US))

Session Classification: Detectors for Future Facilities, R&D, Novel Techniques

Track Classification: 13. Detectors for Future Facilities, R&D, Novel Techniques