Development of a vertex detector prototype for the CEPC

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(On behalf of the CEPC physics and detector group)

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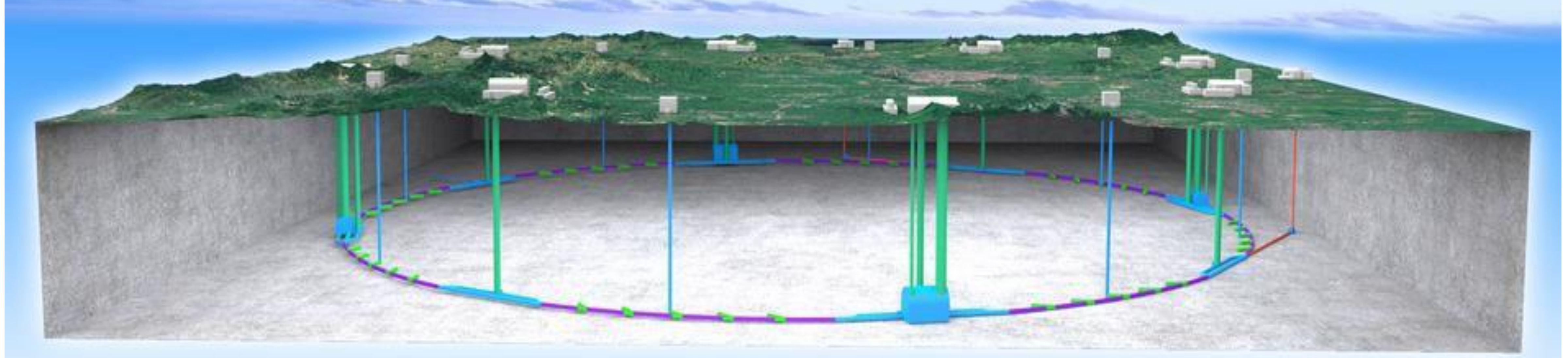
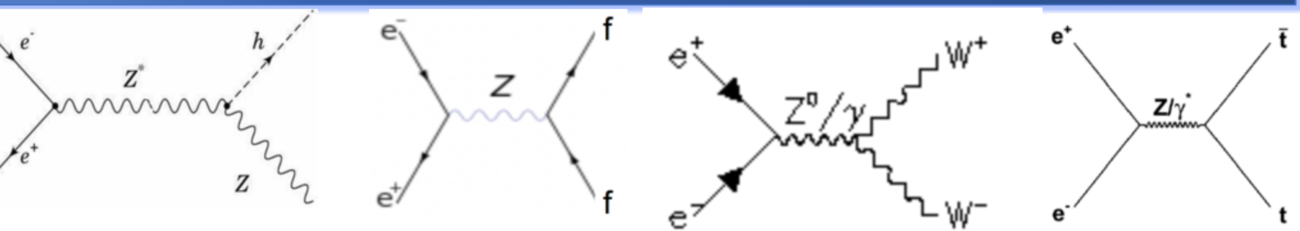


CEPC physics program

An extremely versatile machine with a broad spectrum of physics opportunities

→ Far beyond a Higgs factory

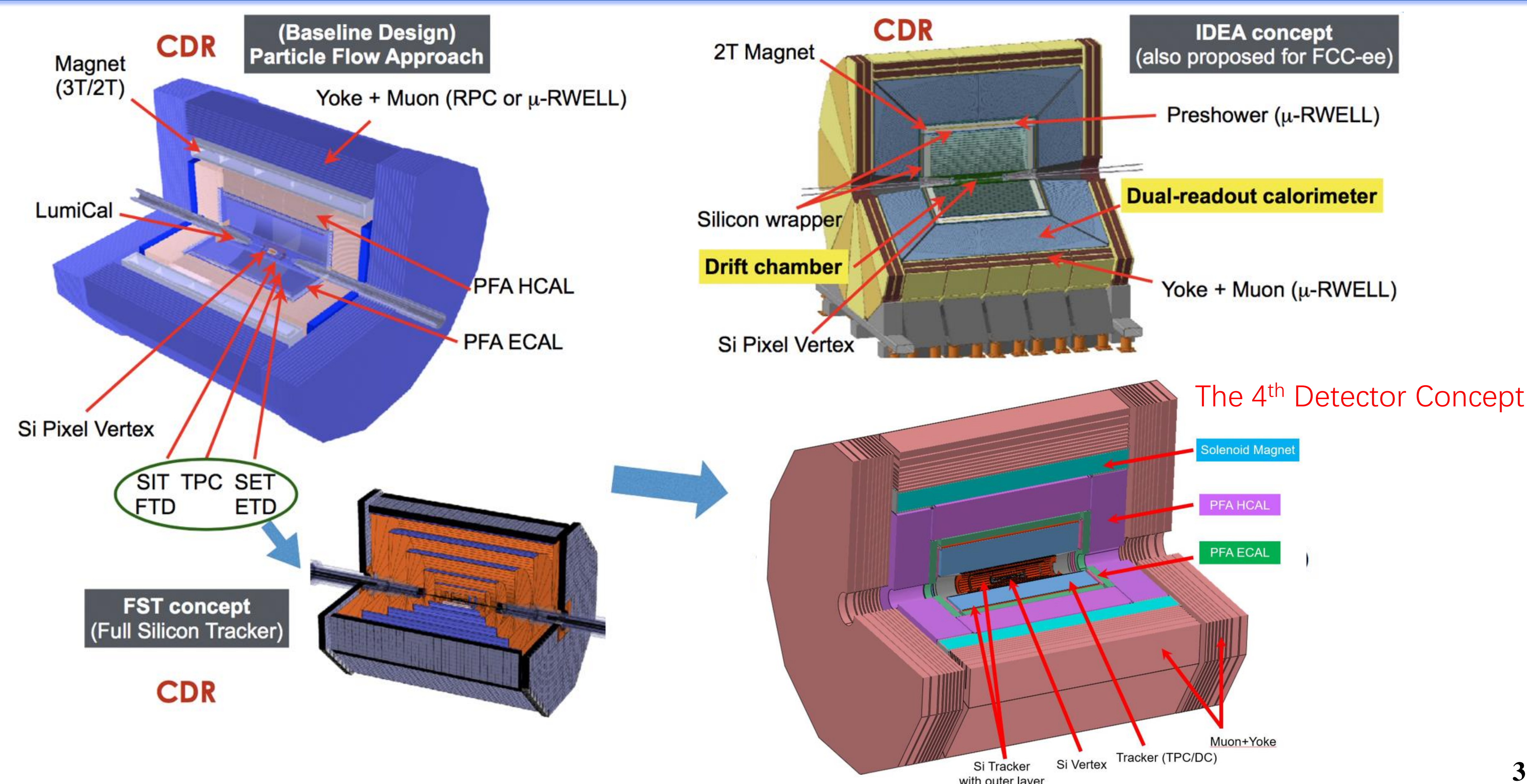


Operation mode			ZH	Z	W^+W^-	$t\bar{t}$
$\sqrt{s}$ [GeV]			~240	~91.2	~160	~360
Run time [years]			10	2	1	5
CDR (30 MW)		L / IP [$\times10^{34}$ cm^{-2}s^{-1}]	**3**	**32**	**10**	-
		$\int L\,dt$ [ab^{-1}, 2 IPs]	5.6	16	2.6	-
		Event yields [2 IPs]	1×10^6	7×10^{11}	2×10^7	-
Run Time [years]			10	2	1	~5
Latest	30 MW	L / IP [$\times10^{34}$ cm^{-2}s^{-1}]	**5.0**	**115**	**16**	**0.5**
	50 MW	L / IP [$\times10^{34}$ cm^{-2}s^{-1}]	8.3	191.7	26.6	**0.8**
		$\int L\,dt$ [ab^{-1}, 2 IPs]	20	96	7	1
		Event yields [2 IPs]	4×10^6	4×10^{12}	5×10^7	5×10^5

- **Huge measurement potential for precision tests of SM: Higgs, electroweak physics, flavor physics, QCD/Top**
- **Searching for exotic or rare decays of H, Z, B and τ, and new physics**
- **CEPC community joined ECFA Phy focus**

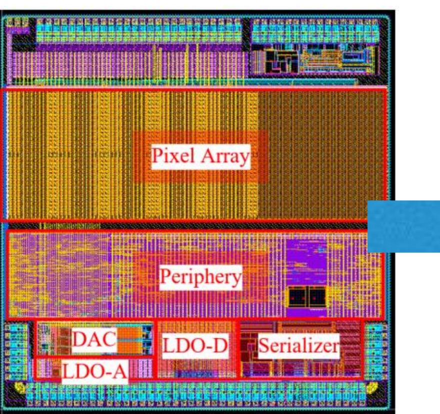
Both 50 MW and $t\bar{t}$ modes are currently considered as CEPC upgrades.

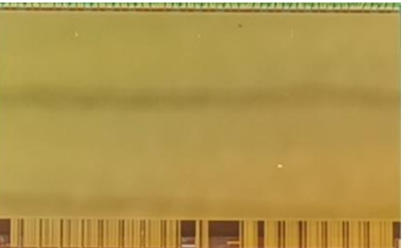
CEPC Detector Conceptual Designs



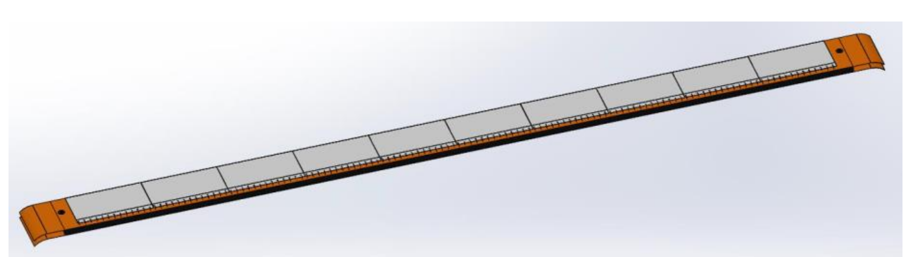
Overview of CEPC vertex detector prototype R & D

CMOS Sensor chip development

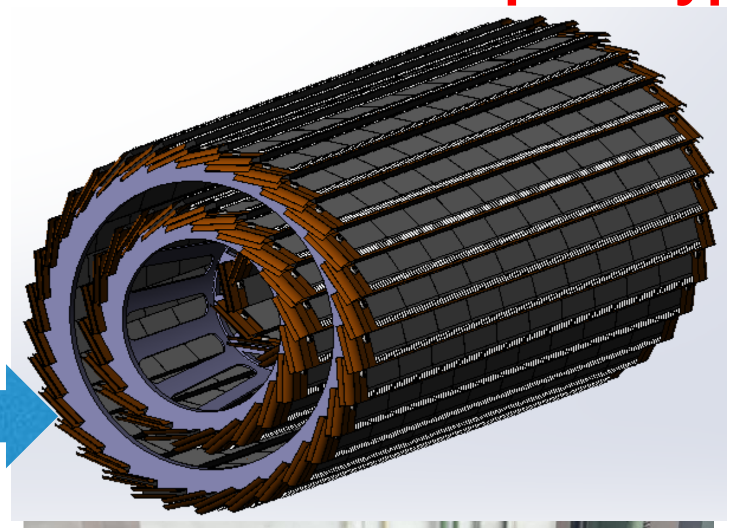


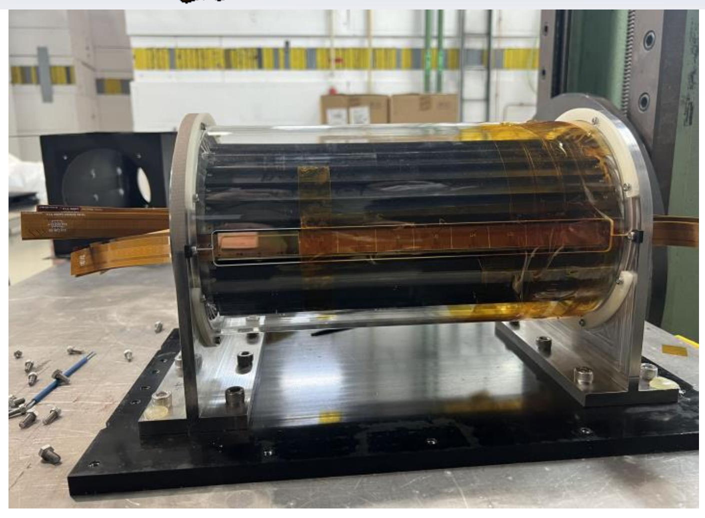


Detector module (Ladder) Prototyping

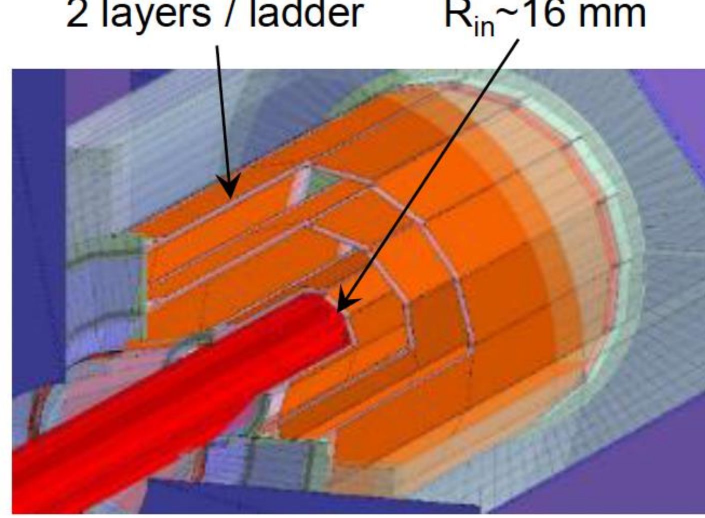


Ladder readout system





Silicon Pixel Chips for Vertex Detector

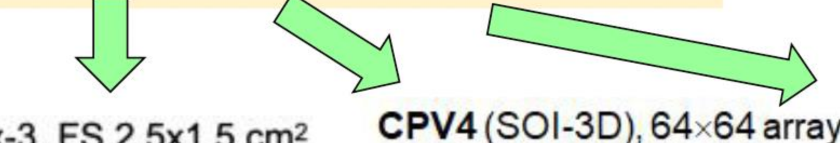


Goal: σ(IP) ~ 5 μm for high P track

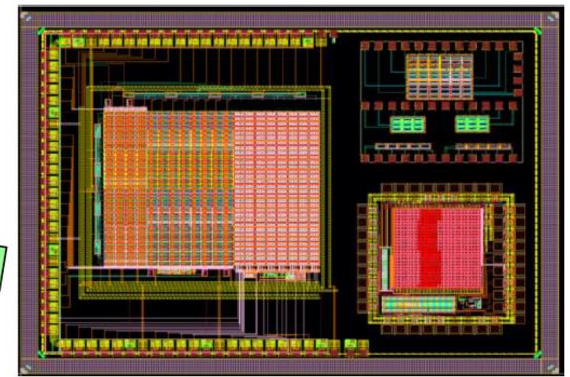
CDR design specifications

- Single point resolution ~ 3μm
- Low material (0.15% X_0 / layer)
- Low power (< 50 mW/cm²)
- Radiation hard (1 Mrad/year)

Silicon pixel sensor develops in 5 series:
JadePix, TaichuPix, CPV, Arcadia, COFFEE



Develop **COFFEE** for a CEPC tracker using SMIC 55nm HV-CMOS process

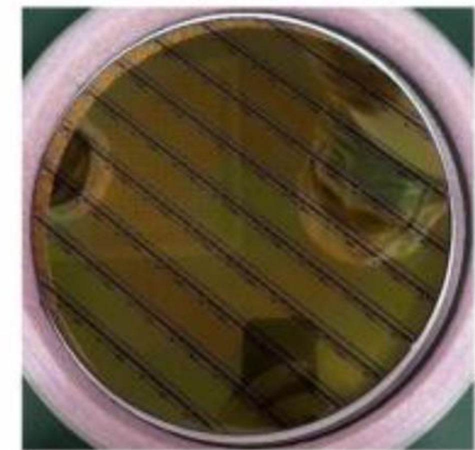


JadePix-3 Pixel size ~16×23 μm²

Tower-Jazz 180nm CiS process
Resolution 5 microns, 53mW/cm²

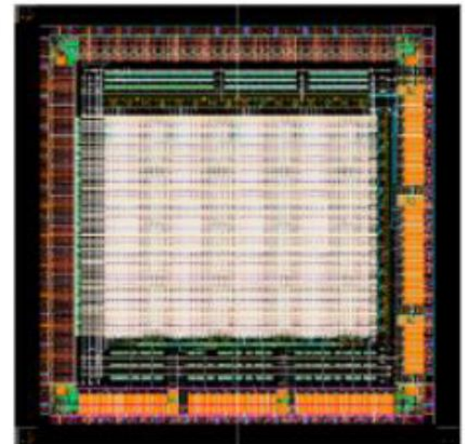
MOST 1

TaichuPix-3, FS 2.5x1.5 cm²
25×25 μm² pixel size



MOST 2

CPV4 (SOI-3D), 64×64 array
~21×17 μm² pixel size

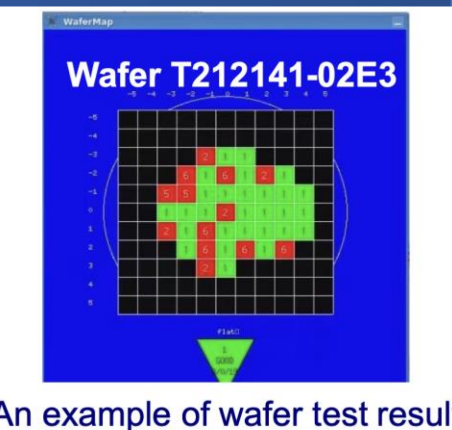


Arcadia by Italian groups for IDEA vertex detector
LFoundry 110 nm CMOS

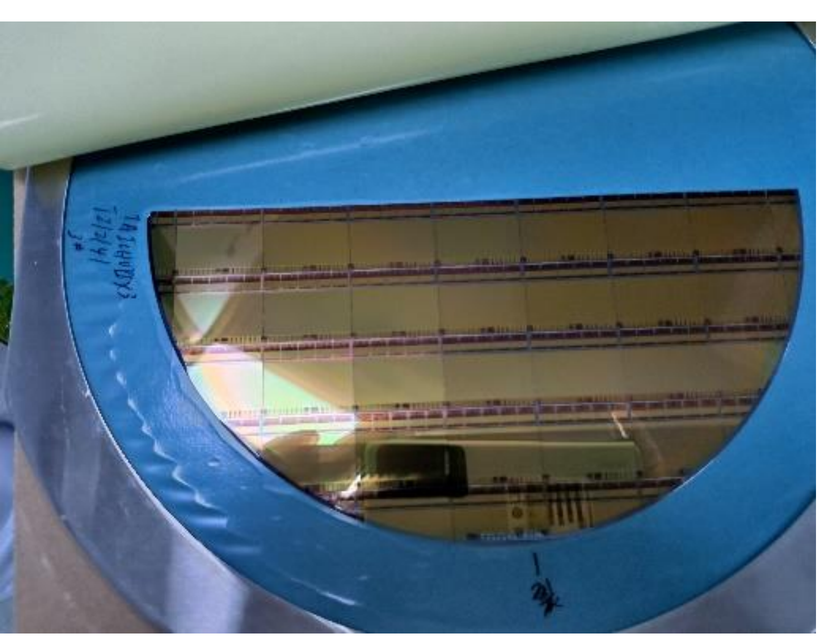
Full-size TaichuPix3 (engineering run)

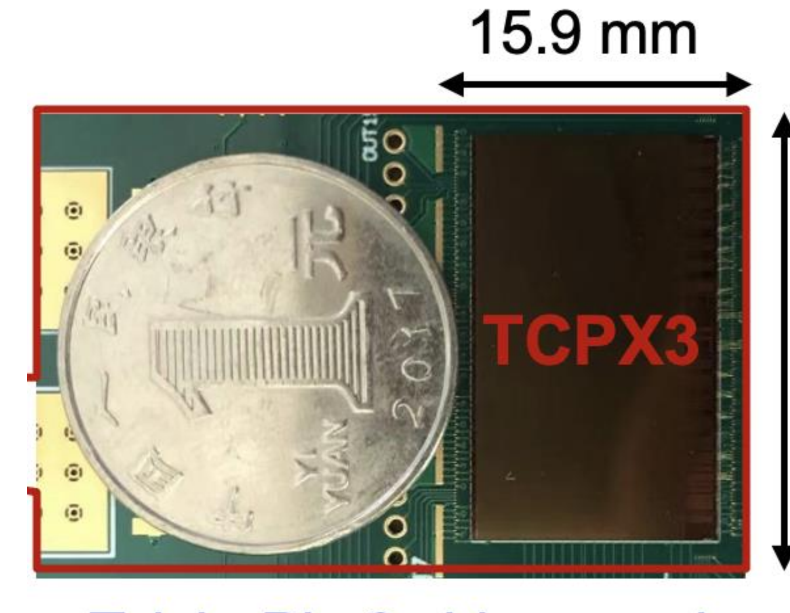
❖ **Developed the first full-size CMOS pixel sensor**

- **Full size 1024×512 Pixel array, Chip Size: 15.9×25.7mm**
  - **25μm×25μm pixel size → high spatial resolution**
  - **Process: Towerjazz 180nm CIS process**
- **Fast digital readout to cope with ZH and Z runs (40MHz clock)**

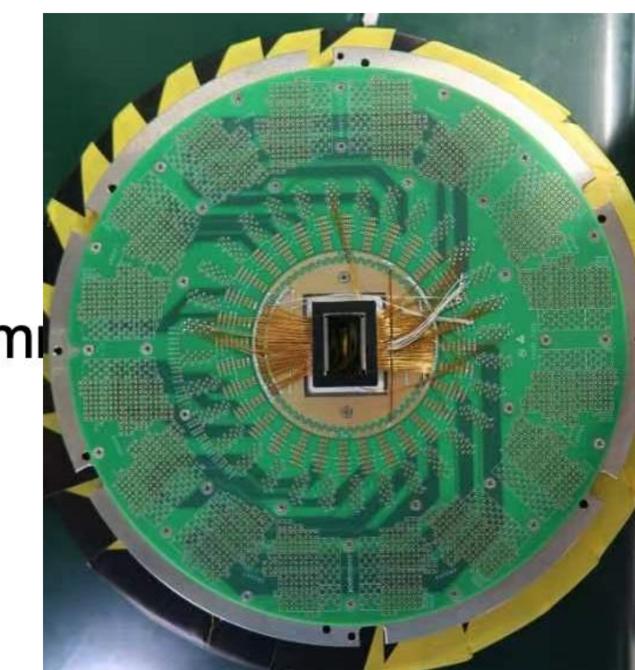


An example of wafer test result



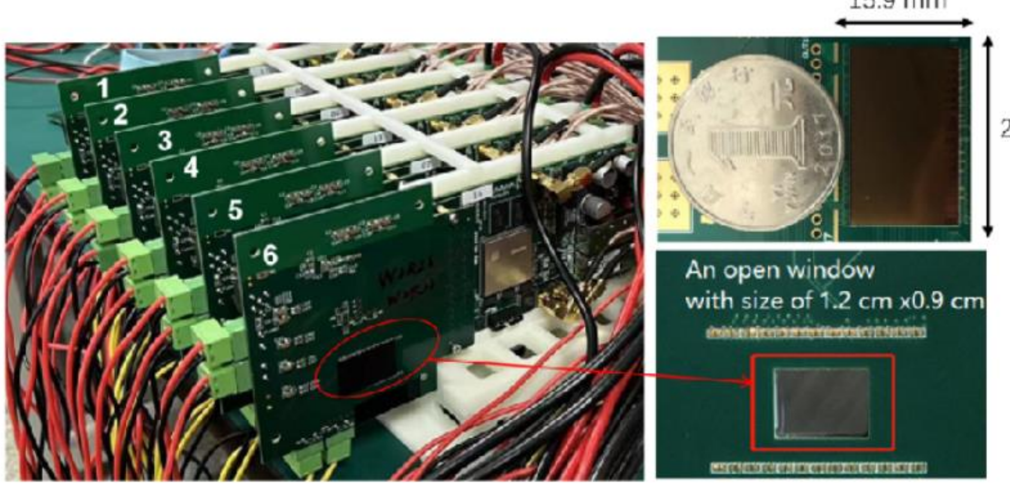


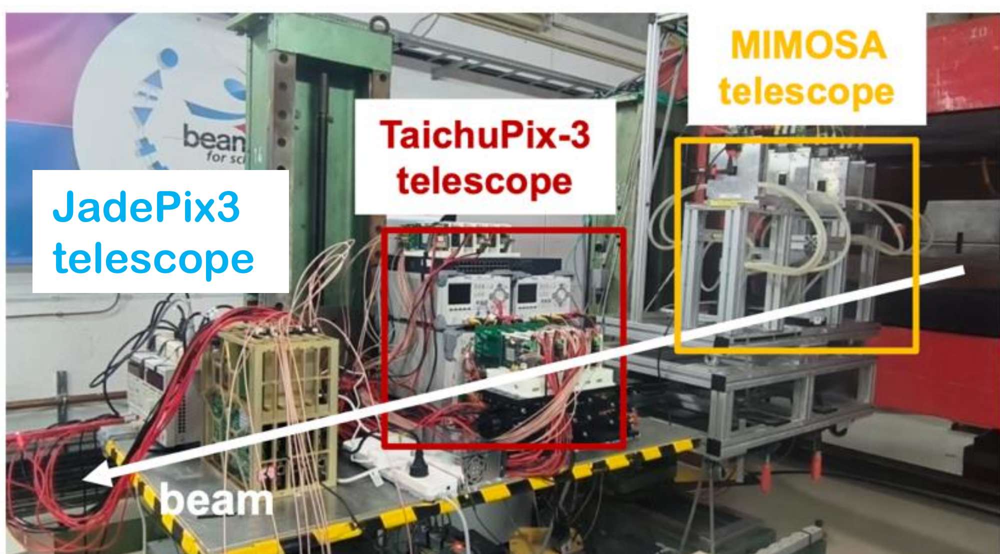
TaichuPix-3 chip vs. coin



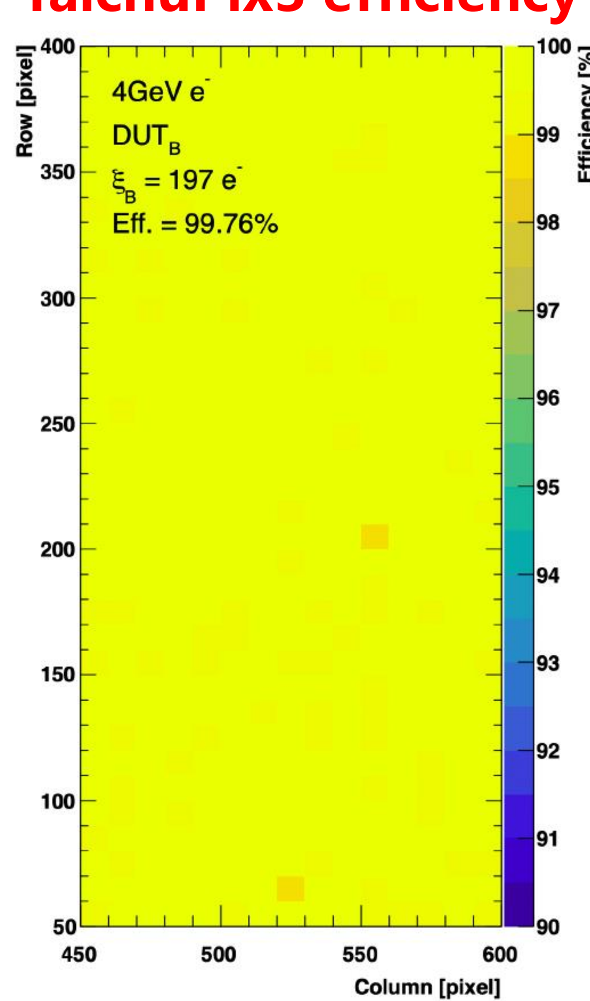
Jadepix3/TaichuPix3 beam test @ DESY

Spatial resolution 4~5um, Efficiency >99%

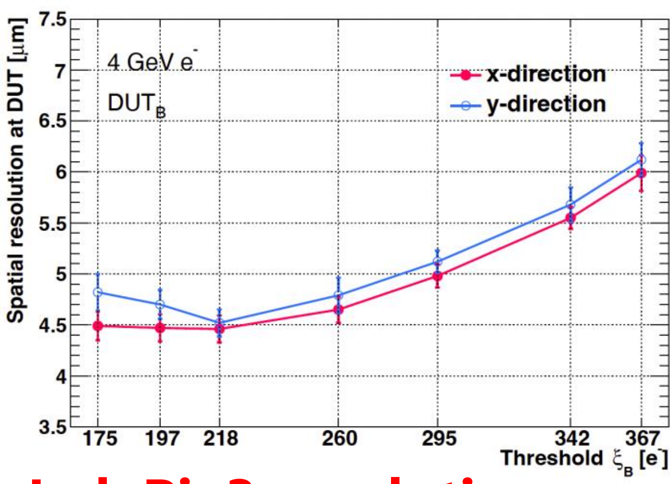




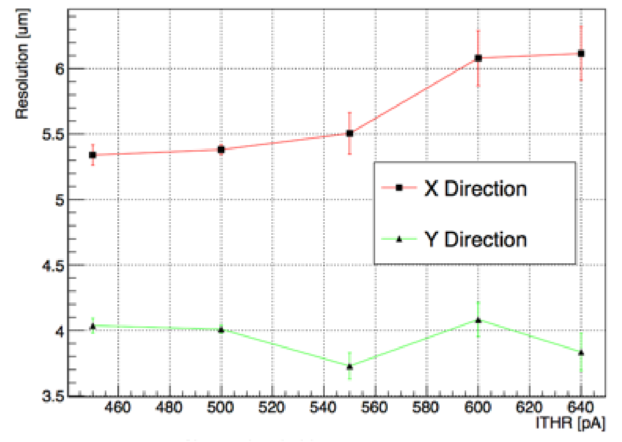
TaichuPix3 efficiency



TaichuPix3 resolution



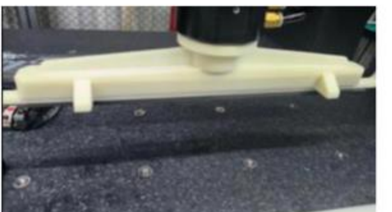
JadePix3 resolution



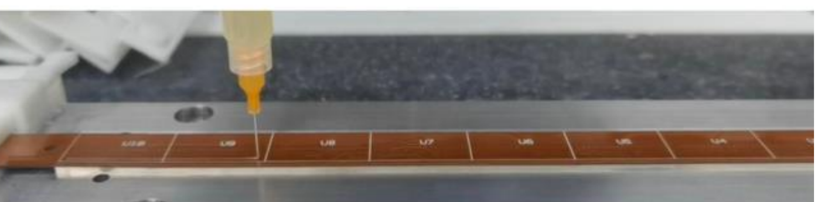
Collaboration with CNRS and IFAE in Jadepix/TaichuPix R & D

TaichuPix3 vertex detector prototype

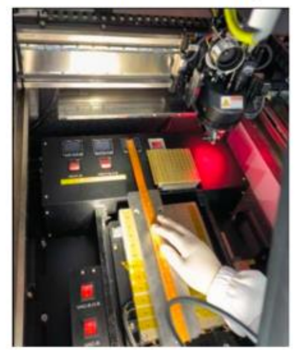
New pickup tools



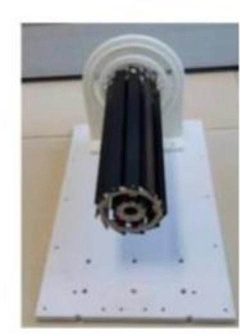
Dummy ladder glue automatic dispensing using gantry

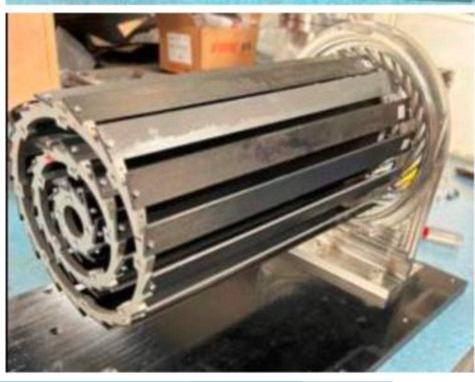


Ladder on wire bonding machine



Dummy Ladder on holder



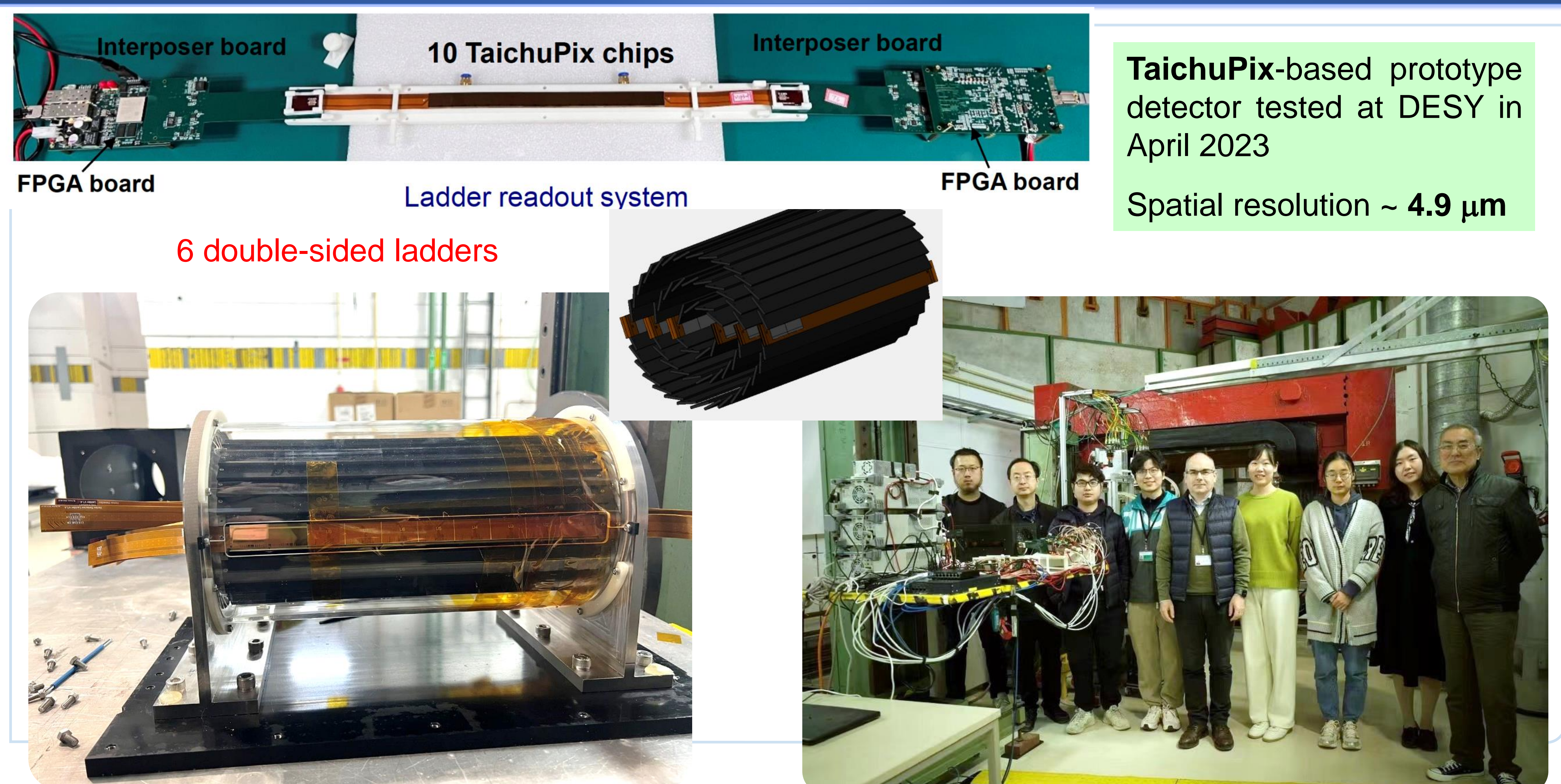


Ladder support tools

Ladder loaded on vertex detector

The first vertex detector (prototype) ever built in China

TaichuPix3 vertex detector prototype beam test @ DESY



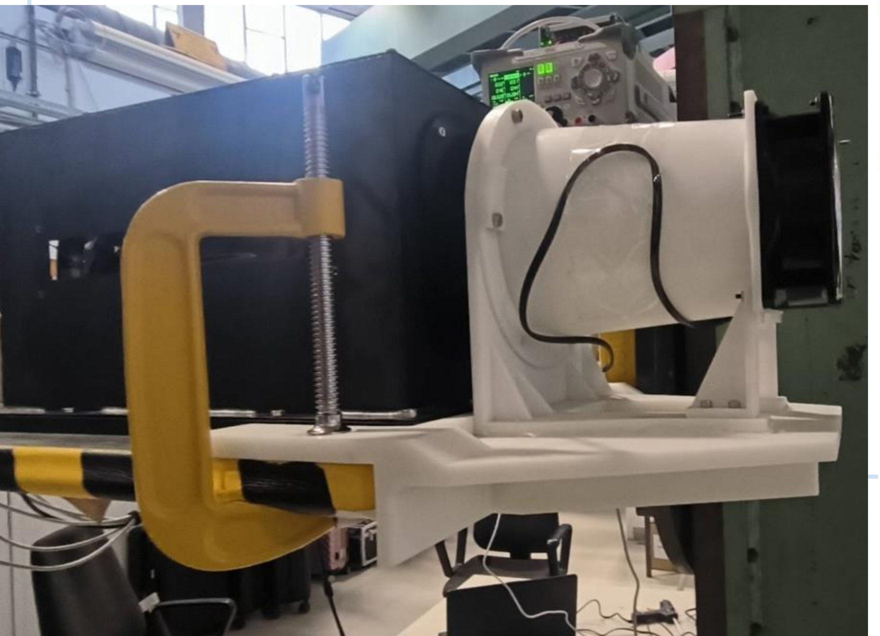
TaichuPix-based prototype detector tested at DESY in April 2023

Spatial resolution ~ **4.9 μm**

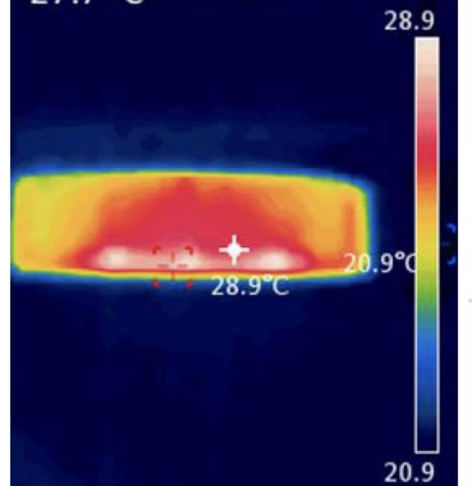
Air cooling in vertex detector prototype

❖Dedicated air cooling channel designed in prototype.

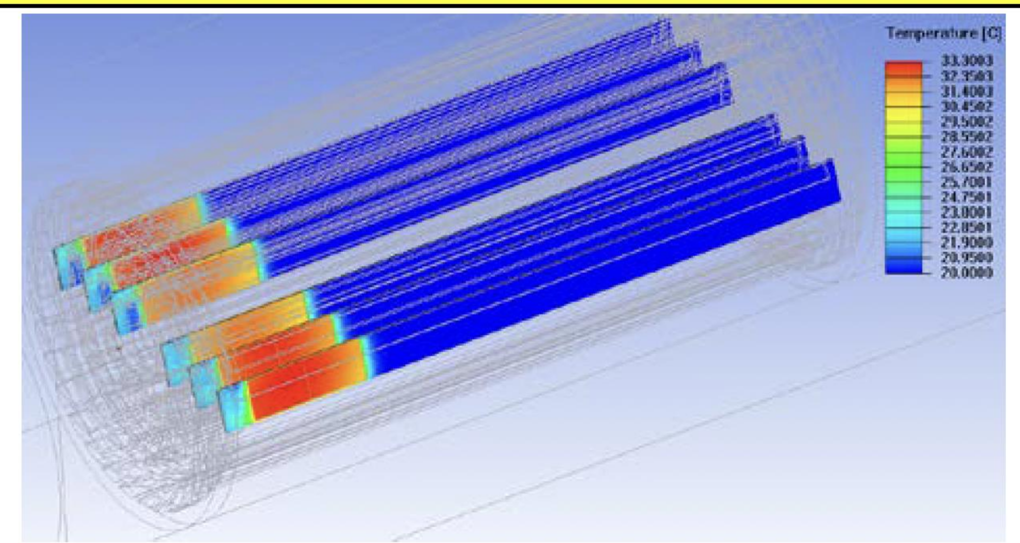
- Measured Power Dissipation of Taichu chip: ~60 mW/cm^2 (17.5 MHz clock in testbeam)
- Before (after) turning on the cooling, chip temperature 41 °C (25 °C)
  - In good agreement to our cooling simulation
  - No visible vibration effect in spatial resolution when turning on the fan



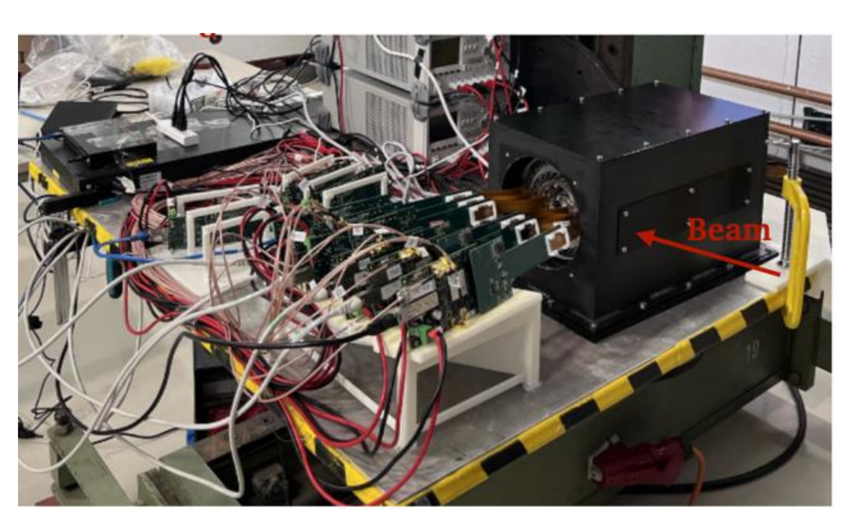
Chip temperature under cooling during beam test: Max 28.9 ℃

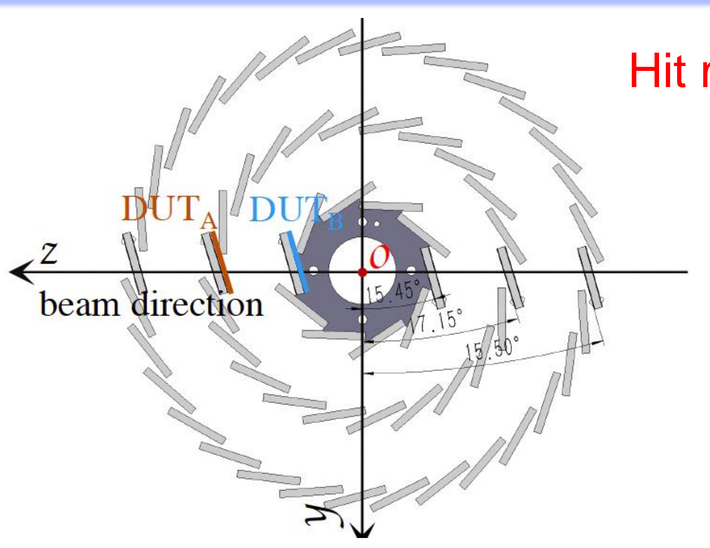


Prototype cooling simulation： Max 33.3 ℃



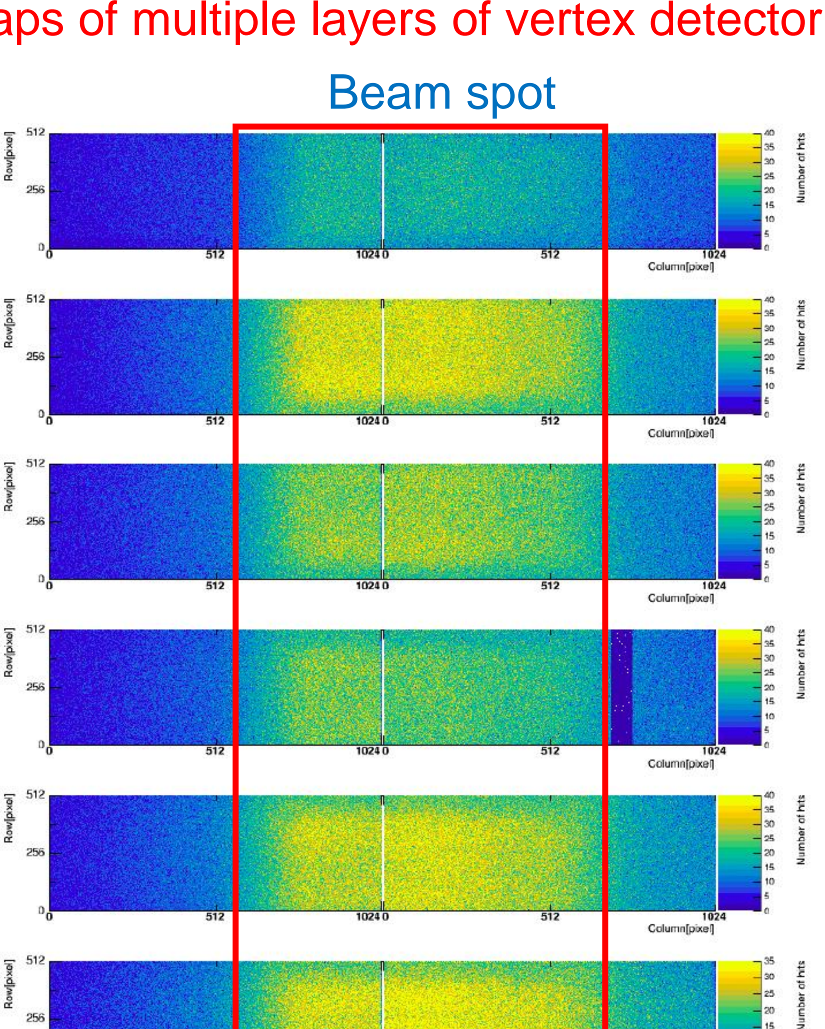
TaichuPix3 vertex detector prototype beam test @ DESY



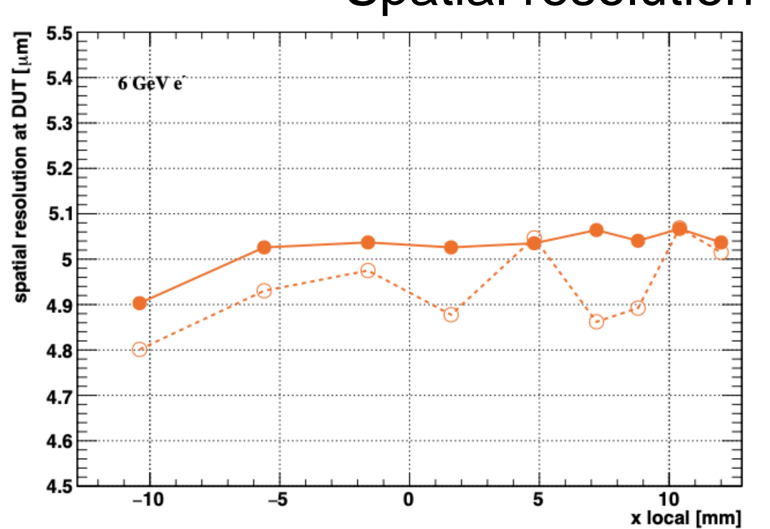


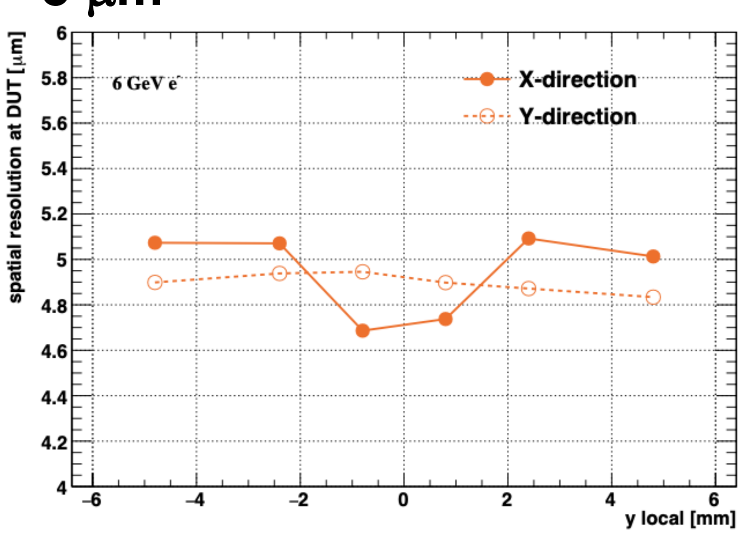
Hit maps of multiple layers of vertex detector

Beam spot



Spatial resolution ~ **5 μm**





From detector prototype to reference TDR

- **Reference detector TDR for CEPC under preparation, to be completed by the mid-2025 for the proposal of China's 15th 5-year plan.**

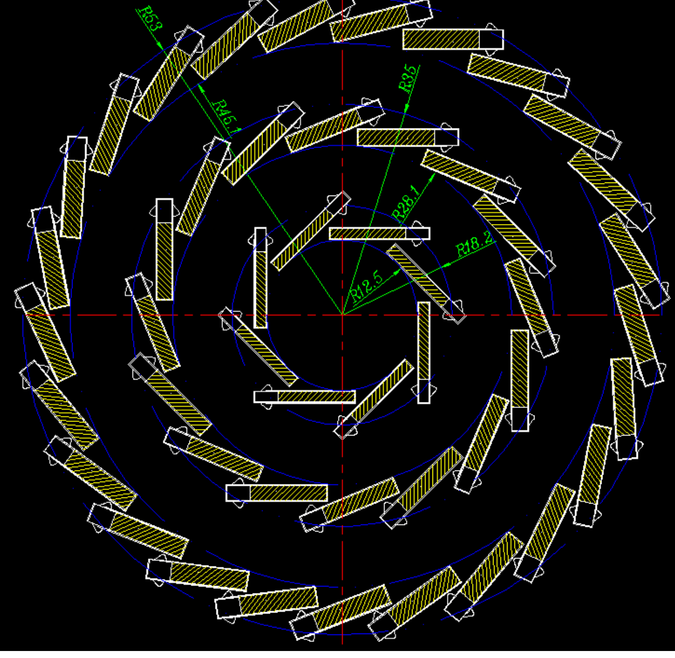
- **Vertex detector Technology selection**
  - Baseline: based on curved MAPS (Inspired by ALICE ITS3 design)
  - Alternative: Ladder design based on MAPS (prototype like design)

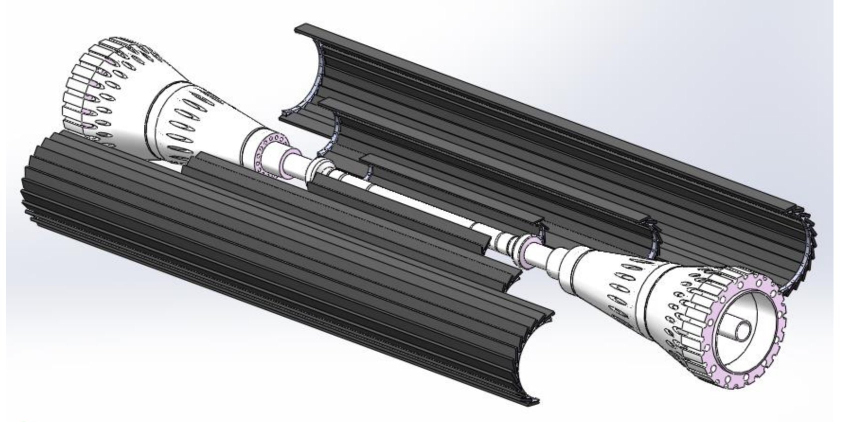
- **Challenges**
  - Closer to beam pipe (radius~11mm, High background rate (at Z pole , 40MHz, 1Gbps per chip)
  - Detector Cooling (<=40 mW/cm^2) with air cooling
  - Radiation level (~1Mrad per year in average)
  - Low material budget (~0.05%X/X0 per layer)
  - Spatial Resolution (3-5um)

Vertex technologies: alternative

❖**Alternative: CMOS chip with long ladder layout**

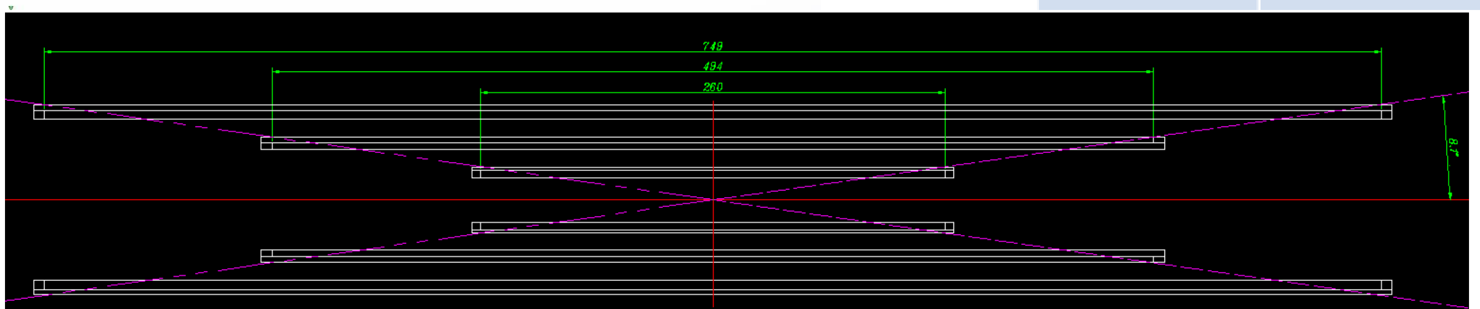
- Long ladder design to cover cos θ<=0.991 (no endcap disk)
- 3 double-side layer with ladders
- Aim to based on 65nm /55nm technology(<=40 mW/cm^2)



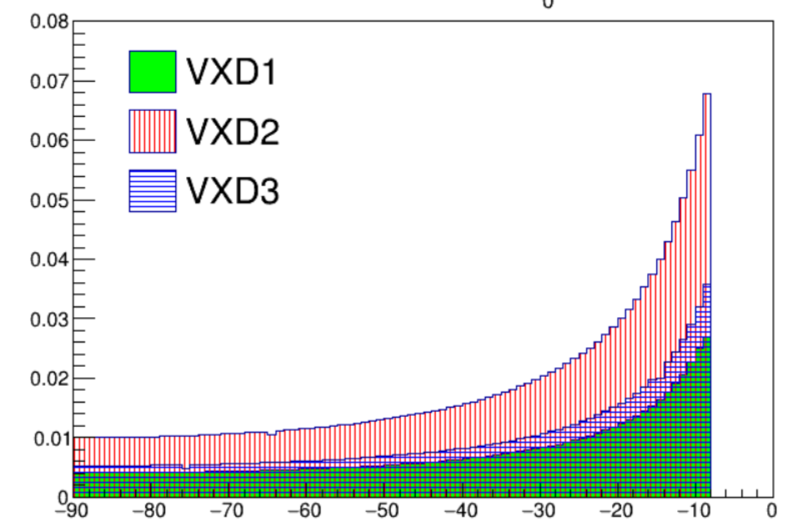


Ladder support size

layer	Size .mm (W x H x L mm)
inner	17.4x1.7x260
middle	17.4x2.5x486
outer	17.4x3.2 x749



Material budget at
Φ =33 degree



Vertex technologies: Cable and service

❖Limited space in MDI region for cable and service

- All fast signal transferred into optical fiber in service region

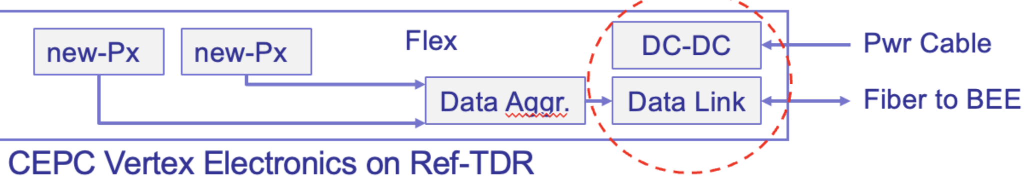
Holes for fibers

Redesigned components by VTX

Holes for air

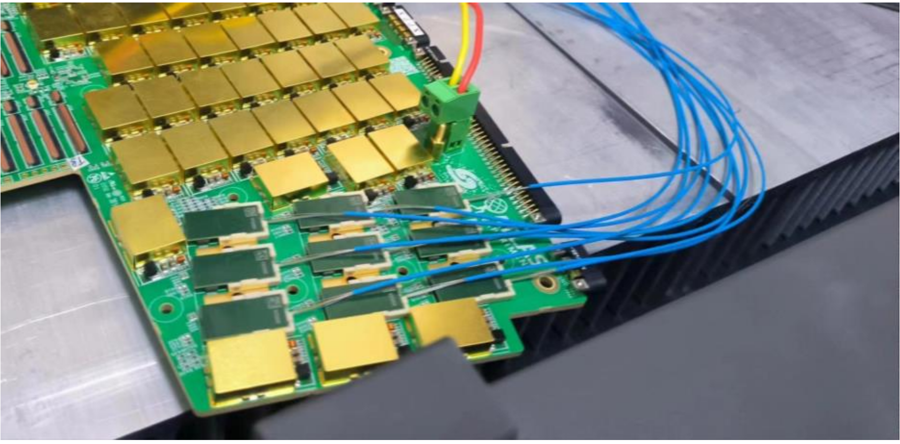
Flex holder

According to the current plan, assuming the flex will be switched to fiber where beyond and near the end of the ladder.



CEPC Vertex Electronics on Ref-TDR

Example from ATLAS HGTD upgrade



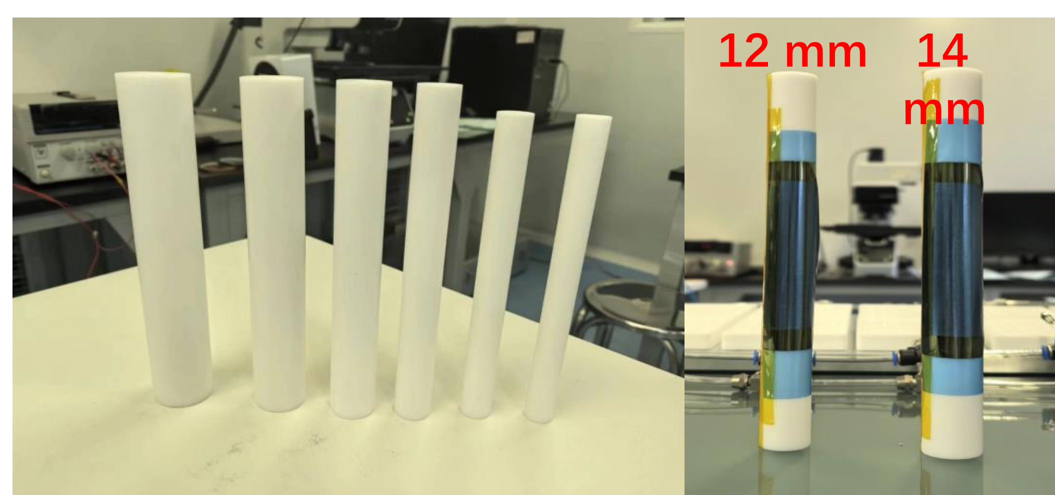
Vertex baseline for CEPC reference TDR: curved MAPS

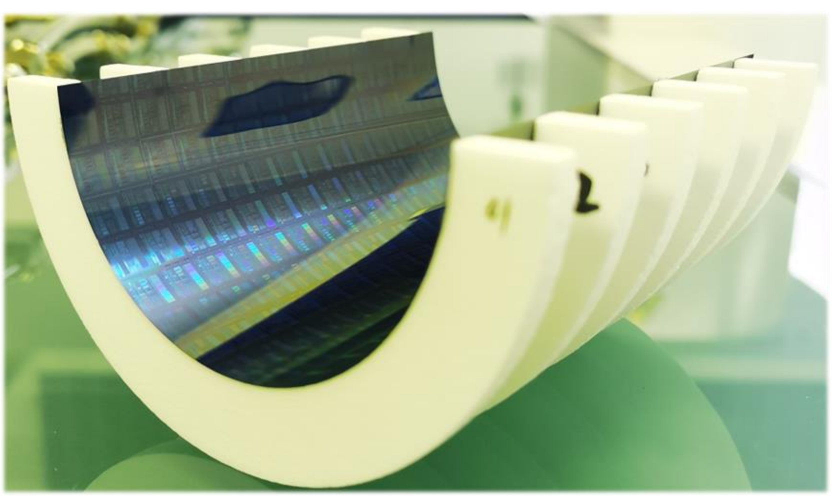
❖Baseline: curved MAPS, Inspired by ALICE ITS3 design

- Advantage: 3~5 times smaller material budget compared to alternative (ladder options)

❖Challenges

- CEPC b-layer radius (radius=11mm) smaller compared with ALICE ITS3 (radius=18mm)
- Feasibility study: Mechanical prototype with dummy wafer can curved to radius ~12mm

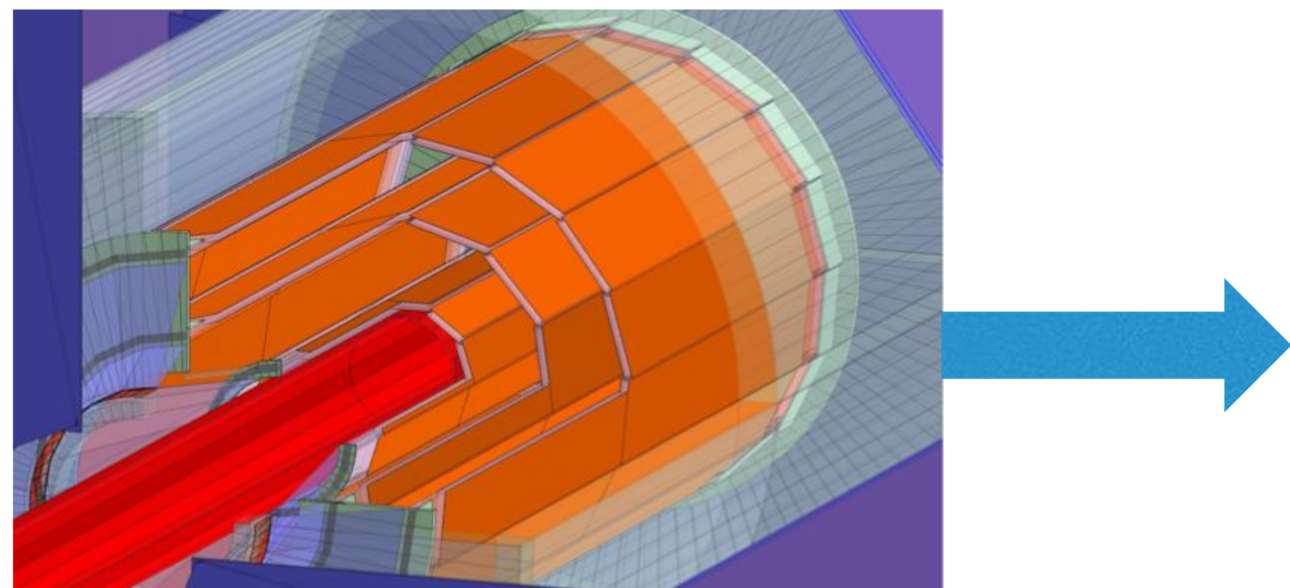




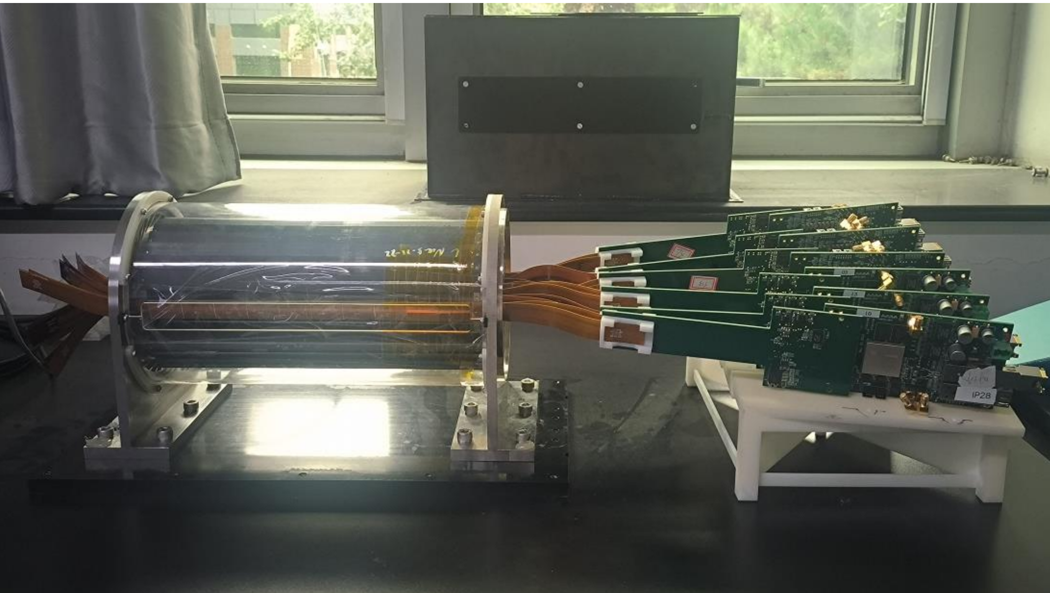
Summary

- 1st full-size Prototype for CEPC vertex detector developed
- Reference detector TDR under preparation, to be completed by the mid-2025 for the proposal of China's 15th 5-year plan.
- It is important to expand international collaboration and explore synergies with other international projects (especially framework of DRD7 (electronics) and DRD8 (mechanics and integration) more than DRD3 (solid state detectors).

CEPC vertex conceptional design (2016)



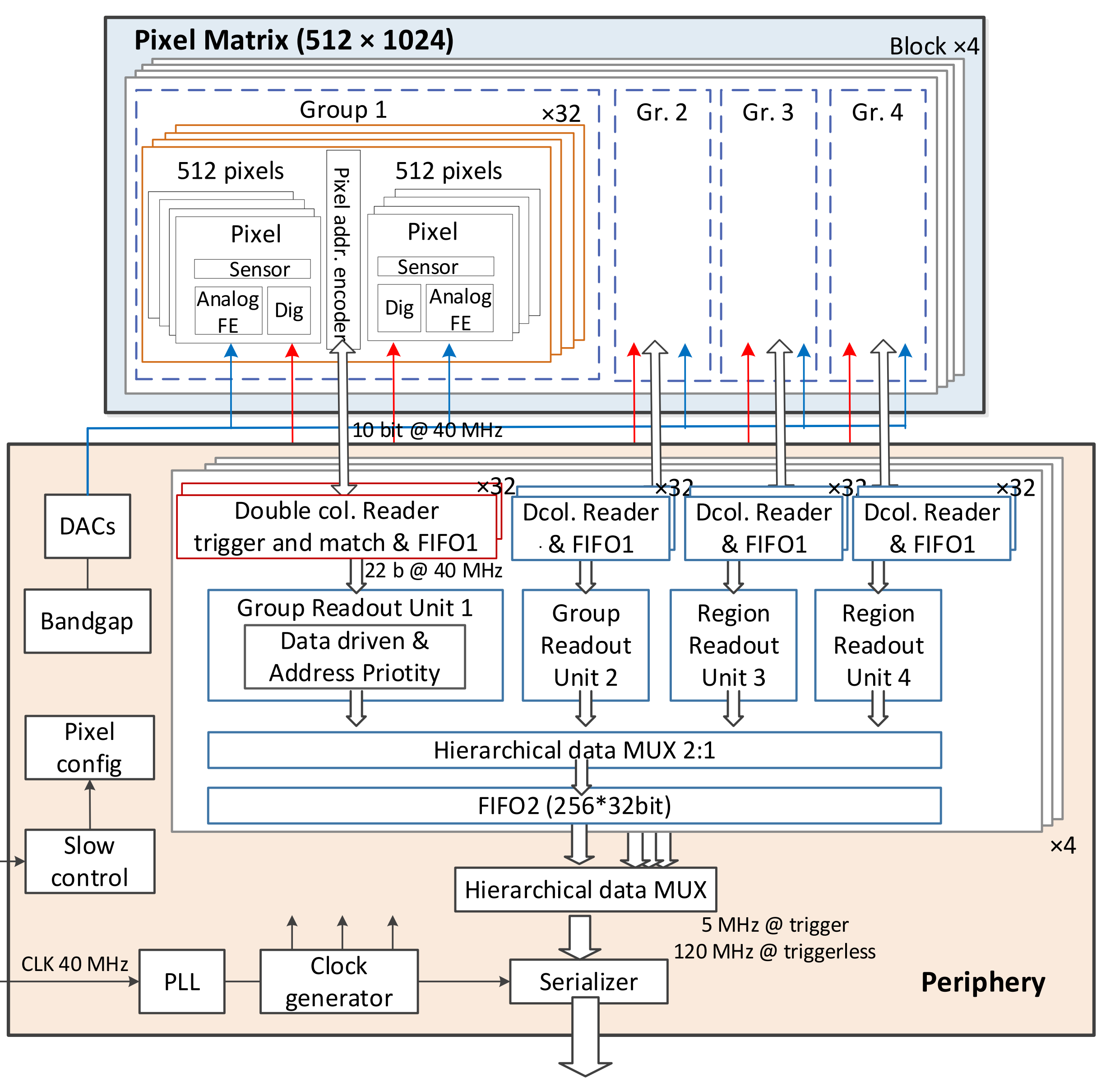
CEPC vertex prototype (2023)



TaichuPix design

- **Pixel 25 μm × 25 μm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - Readout time: 50-100 ns for each pixel
- **2-level FIFO architecture**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate
  - between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp

    only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc



scenario B: three of double-layers

R [mm]
45
40
35
30
25
20
15
10
5
0

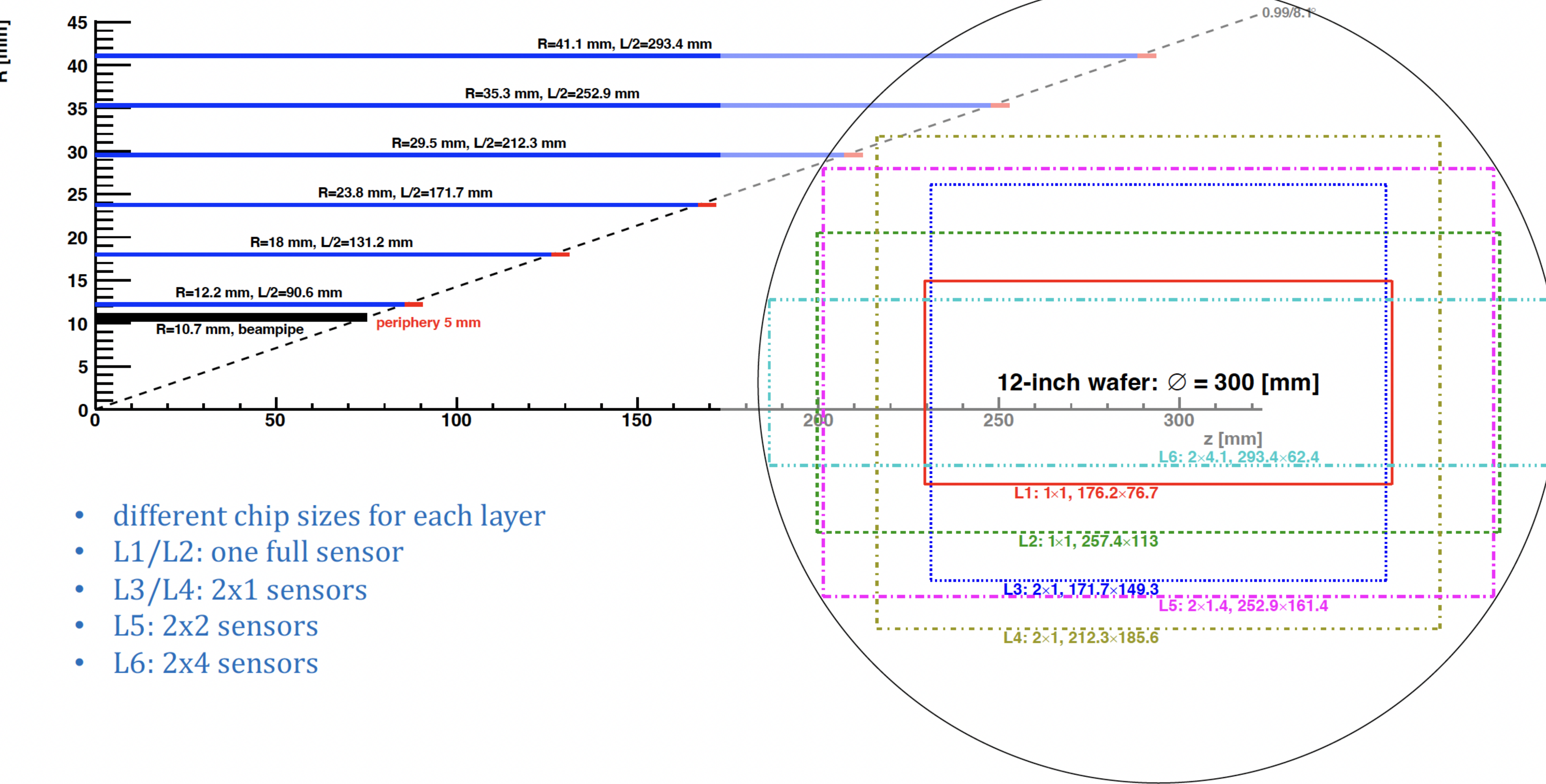
R=41.1 mm, L/2=293.4 mm
R=39.6 mm, L/2=293.4 mm
R=27.4 mm, L/2=197.3 mm
R=25.9 mm, L/2=197.3 mm
R=13.7 mm, L/2=101.1 mm
R=12.2 mm, L/2=101.1 mm
R=10.7 mm, beampipe
periphery 5 mm
0.99/8.1°

0 50 100 150 200 250 300
z [mm]

12-inch wafer: ∅ = 300 [mm]
L6: 2×4.1, 293.4×62.4
L5: 2×4, 293.4×62.4
L1: 1×1, 197.3×76.7
L2: 1×1, 197.3×86.1
L3: 2×1, 197.3×162.7
L4: 2×1, 197.3×172.2

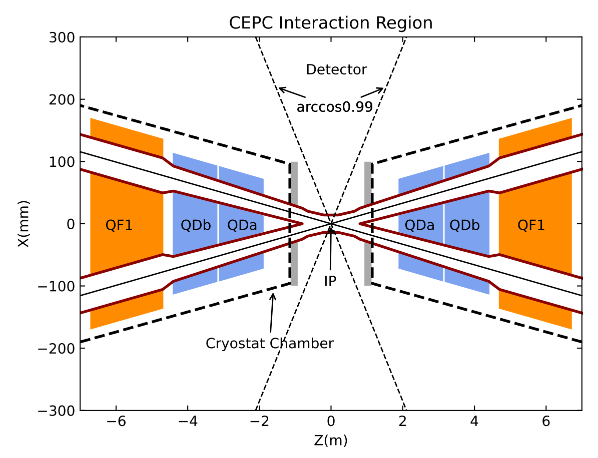
- two sizes of chips: one for L1-4, another L5/6
- L1/L2: one full sensor
- L3/L4: 2x1 sensors
- L5/6: 2x4 sensors

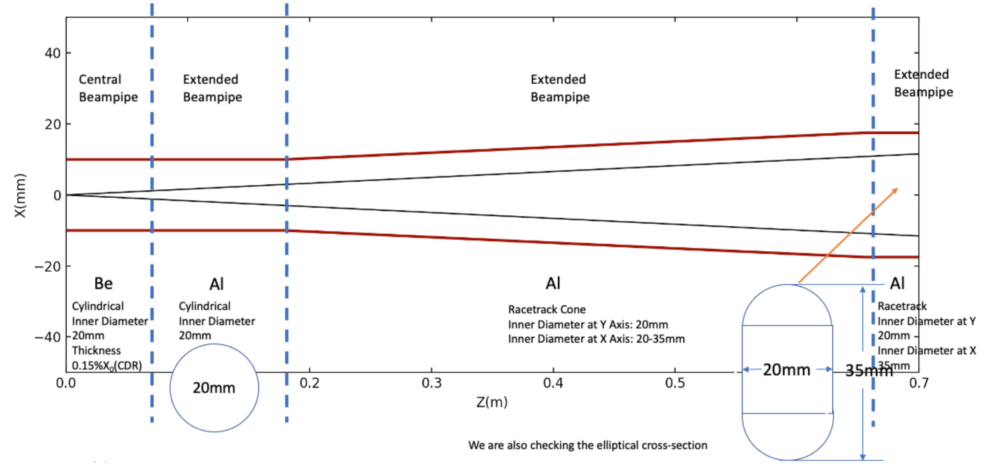
scenario A: uniform layout

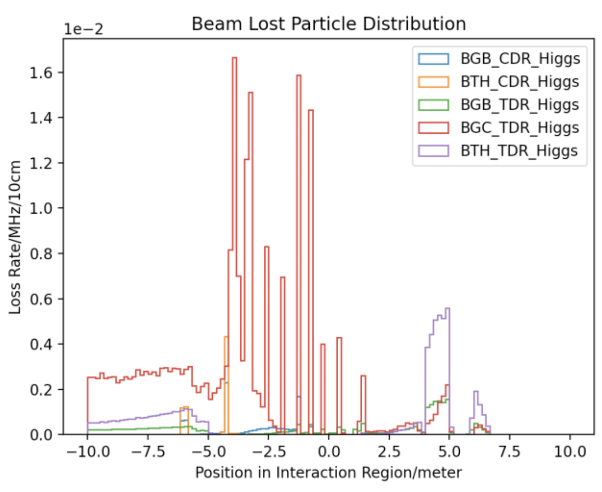


Highlights of CEPC machine detector interface (MDI)

The design based on Accelerator TDR has been done. The background simulation is performing.

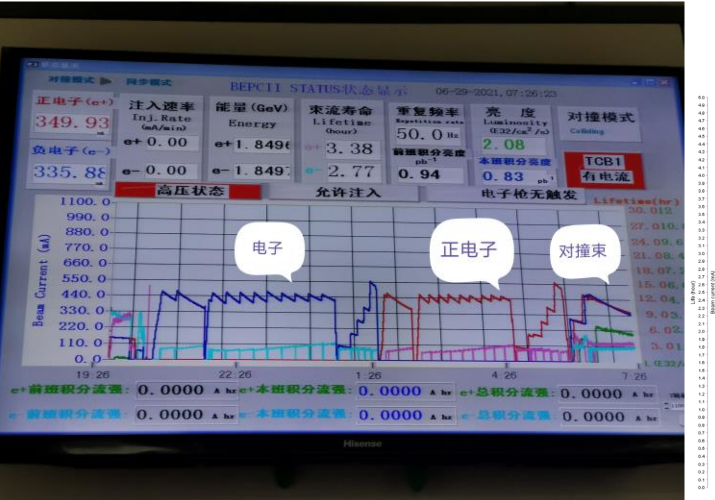


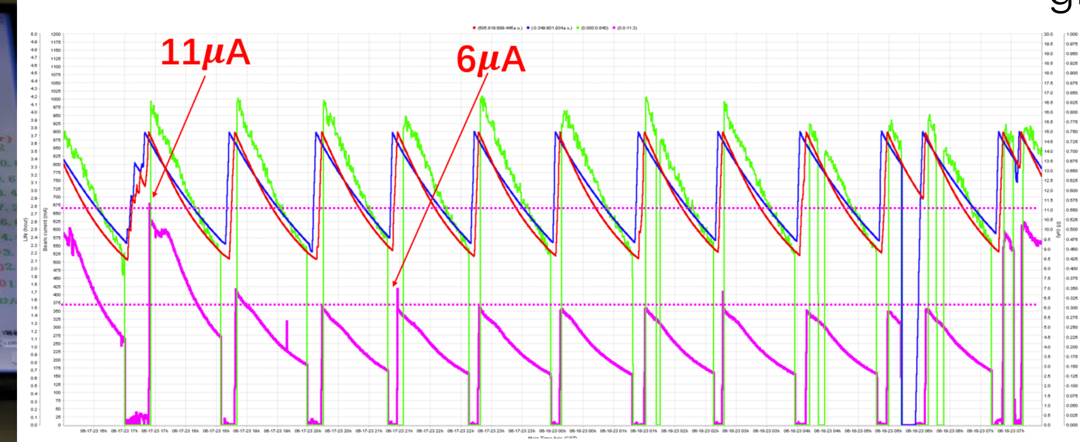




The experiment at BEPCII has been done several times to validate the code.

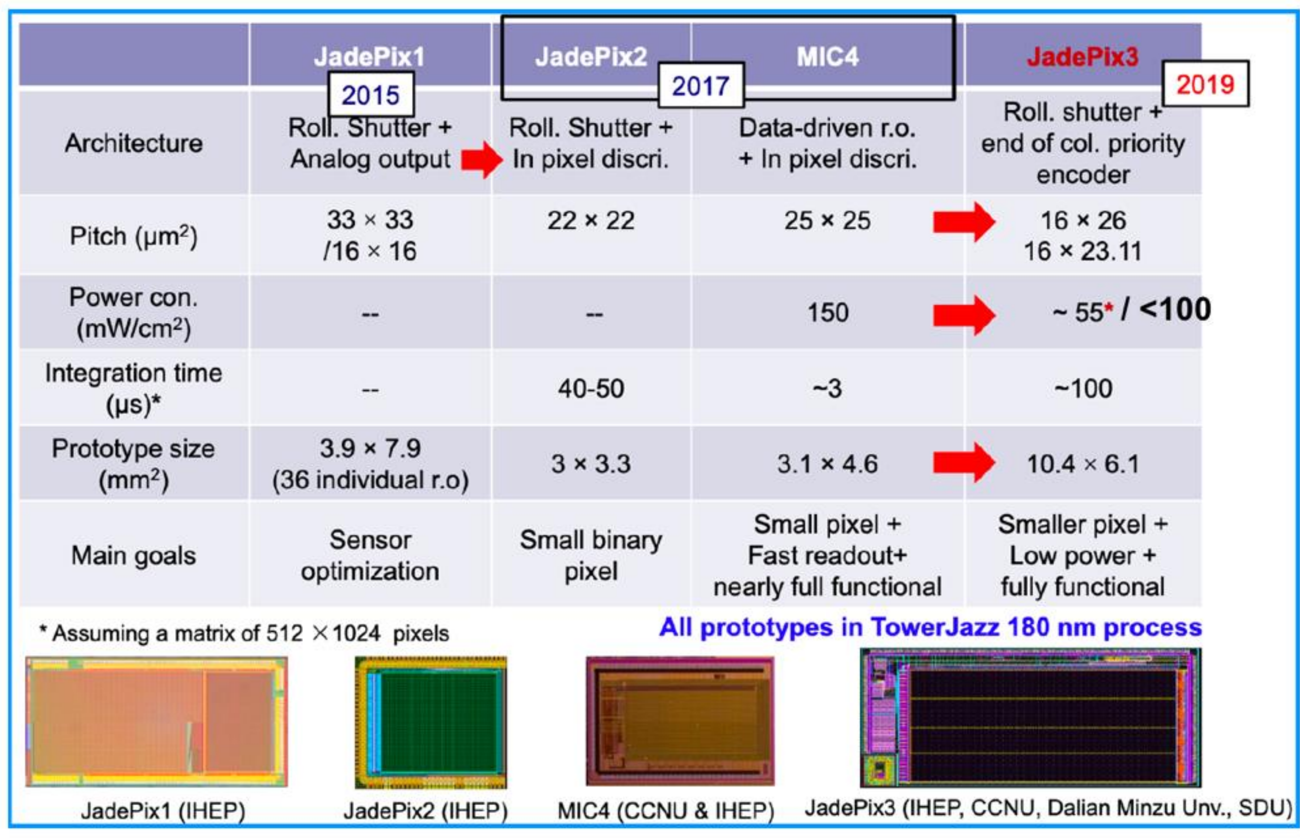
The collaboration on beam induced background study between different groups has been formed.





CMOS MAPS sensors development

All developed with TowerJazz CIS 180 nm process



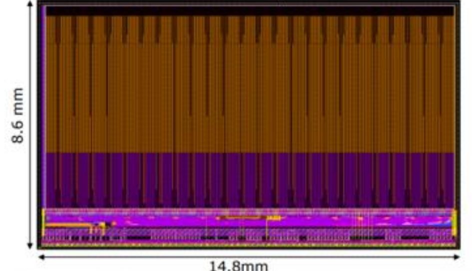
	JadePix1 (2015)	JadePix2 (2017)	MIC4	JadePix3 (2019)
Architecture	Roll. Shutter + Analog output	Roll. Shutter + In pixel discri.	Data-driven r.o. + In pixel discri.	Roll. shutter + end of col. priority encoder
Pitch (µm²)	33 × 33 /16 × 16	22 × 22	25 × 25	16 × 26 16 × 23.11
Power con. (mW/cm²)	--	--	150	~ 55* / <100
Integration time (µs)*	--	40-50	~3	~100
Prototype size (mm²)	3.9 × 7.9 (36 individual r.o)	3 × 3.3	3.1 × 4.6	10.4 × 6.1
Main goals	Sensor optimization	Small binary pixel	Small pixel + Fast readout+ nearly full functional	Smaller pixel + Low power + fully functional

* Assuming a matrix of 512 × 1024 pixels

All prototypes in TowerJazz 180 nm process

JadePix1 (IHEP) JadePix2 (IHEP) MIC4 (CCNU & IHEP) JadePix3 (IHEP, CCNU, Dalian Minzu Unv., SDU)

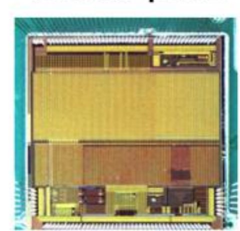
JadePix4 **Design finalized, to be taped off**



	S.P. resolution	Integration time	Average power
JadePix-4	<5 µm	~1 µs	< 100 mW/cm²
JadePix-3	<3 µm	<100 µs	< 100 mW/cm²

Optimized for fast readout

Taichupix1 Taichupix2 Full-size Taichupix



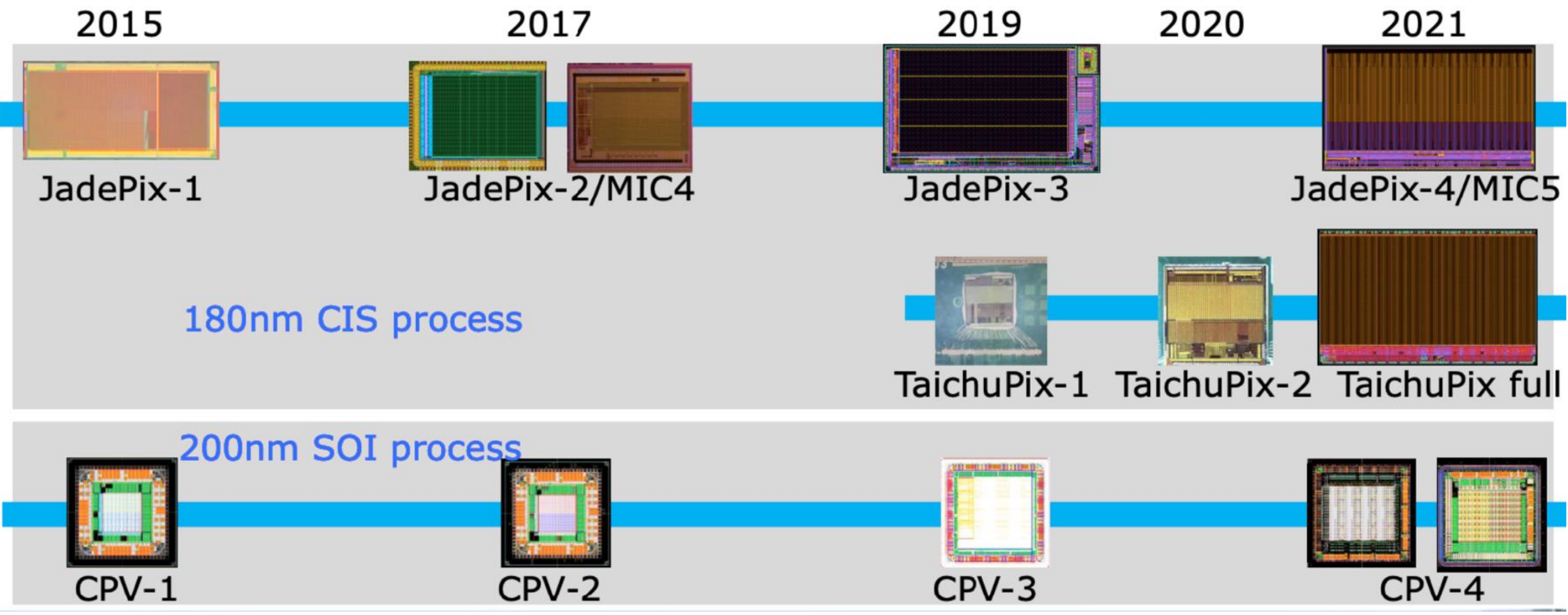
Chip size: 5 mm × 5 mm
Pixel size: 25 µm × 25 µm

1024*512 pixel array, FE-I3-like

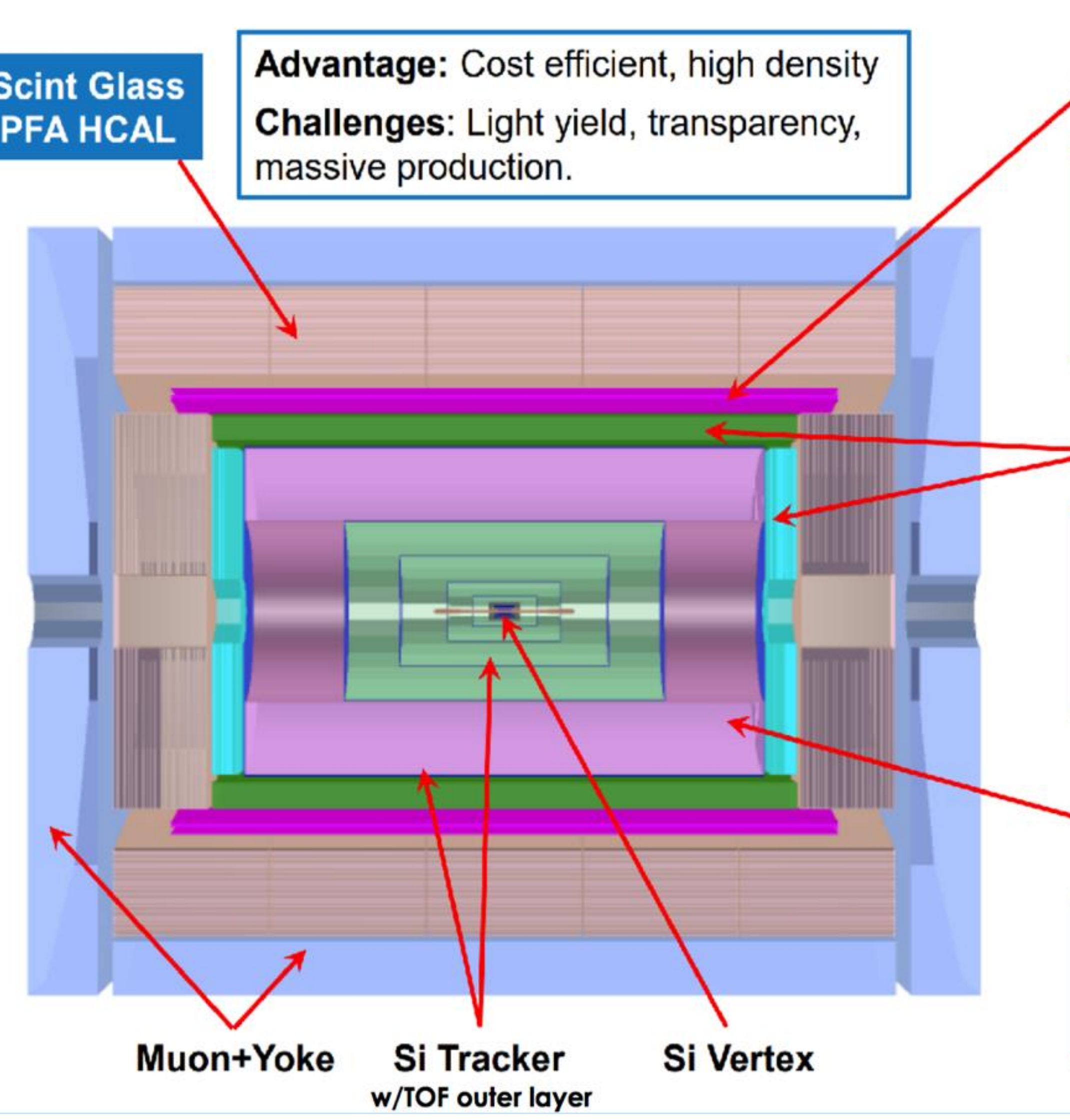
High speed, deadtime~50ns@40MHz,
time stamp precision 25/50ns

Full-size chips produced and tested

Vertex detector sensor R&D timeline



The 4th Detector Concept



Solenoid Magnet (3T / 2T)
Between HCAL & ECAL

Advantage: the HCAL absorbers act as part of the magnet return yoke.

Challenges: thin enough not to affect the jet resolution (e.g. BMR); stability.

Crystal ECAL

Advantage: better π^0/γ reconstruction.

Challenges: minimum number of readout channels; compatible with PFA calorimeter; maintain good jet resolution.

A Drift chamber
that is optimized for PID

Advantage: Work at high luminosity Z runs

Challenges: sufficient PID power; thin enough not to affect the moment resolution.

Excellent e/gamma energy resolution;

PID capability;

Better hadronic energy resolution;

Magnet in much reduced size.

BMR: 4% → 3%

Backup: Vertex alternative: expected performance