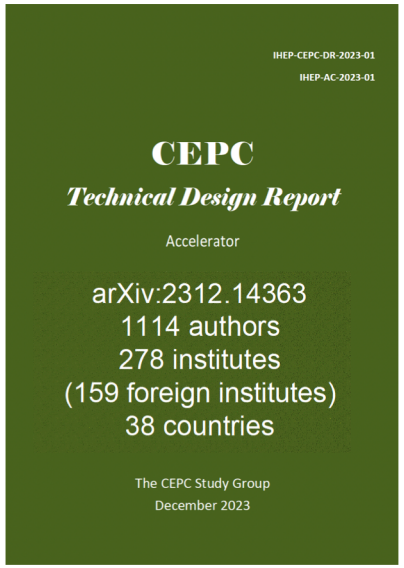
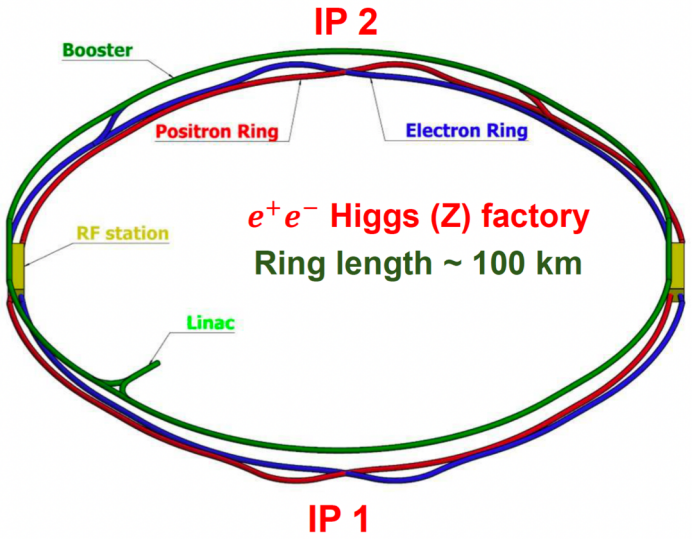
Development of CMOS-based tracker for CEPC

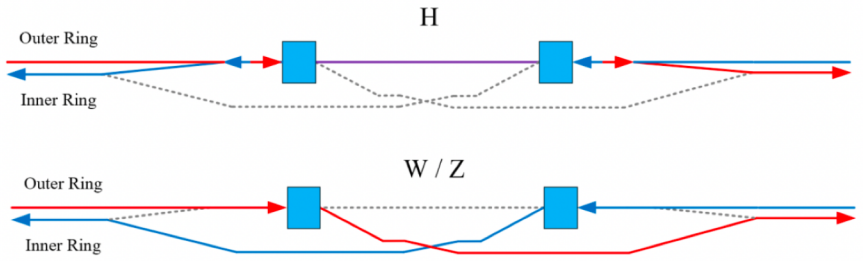
Yiming Li (IHEP, CAS)
On behalf of the CEPC silicon tracker team

CEPC

- Circular Electron-Positron Collider, as a Higgs / Z / W factory, for high-precision Higgs, EW, flavour physics, and for probe of new physics beyond Standard Model
  - Proposed by Chinese HEP community after Higgs discovery
  - CDR published in 2018
  - Accelerator TDR released in end 2023
  - Reference detector TDR under preparation







Switchable operation for H/W/Z

Particle	$E_{c.m.}$ (GeV)	L per IP (10^{34} cm^{-2}s^{-1})	Integrated L per year (ab^{-1}, 2 IPs)	Years	Total Integrated L (ab^{-1}, 2 IPs)	Total no. of events
H	240	5	1.3	10	13	2.6×10^6
Z	91	115*	30	2	60	2.5×10^{12}
W	160	16	4,2	1	4.2	1.3×10^8
$t\bar{t}$**	360	0.5	0.13	5	0.65	0.4×10^6

* Detector solenoid field is 2 Tesla during Z operation.
** $t\bar{t}$ operation is optional.

Operational plan @ 30MW
(upgradable to 50MW)

Haijun Yang's talk : Status of the CEPC Project

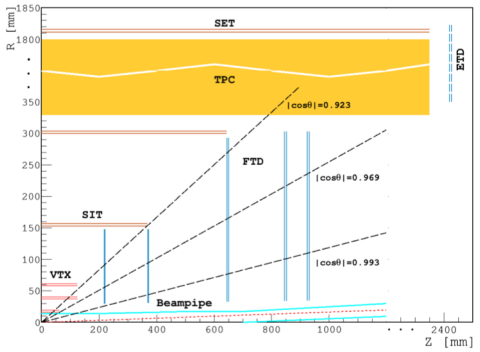
CEPC silicon tracker

- Large area silicon tracker: technical challenges
  - ~70 – 140 m^2 depending on detector concept
  - ~10 um spatial resolution imposed by requirement on momentum resolution
  - A few ns timing resolution to tag 23ns bunches at Z-pole
  - Low material budge
  - Moderate power consumption

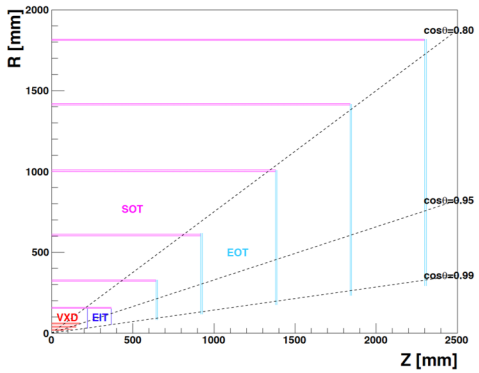
$$\sigma_{1/p_T} = a \oplus \frac{b}{p \sin^{3/2}\theta} \quad [\mathrm{GeV}^{-1}]$$

$$a \sim 2 \times 10^{-5}\ \mathrm{GeV}^{-1}$$

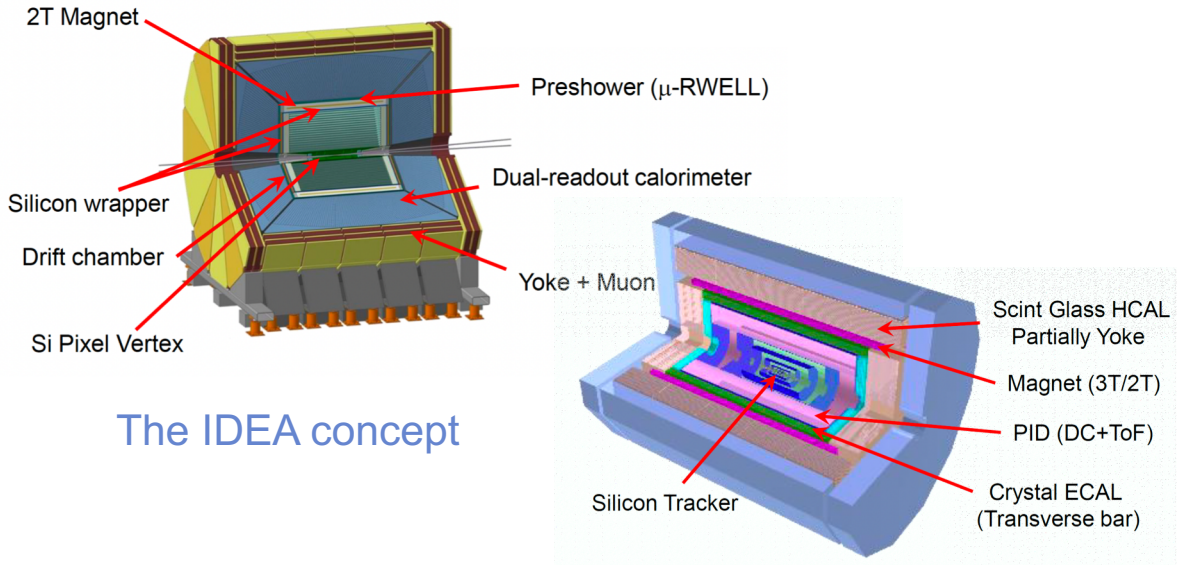
$$b \sim 1 \times 10^{-3}$$



Baseline concept (CDR)



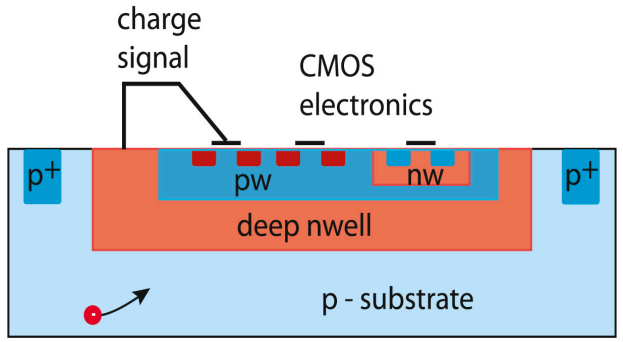
Full Silicon Tracker (CDR)



The IDEA concept

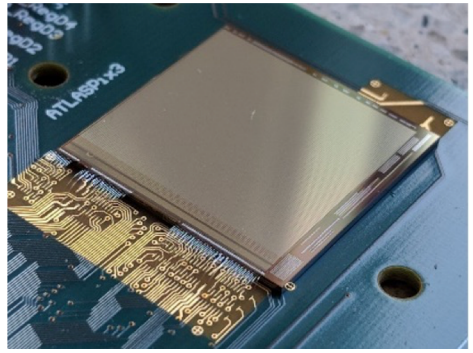
The 4th concept → reference detector (WIP)

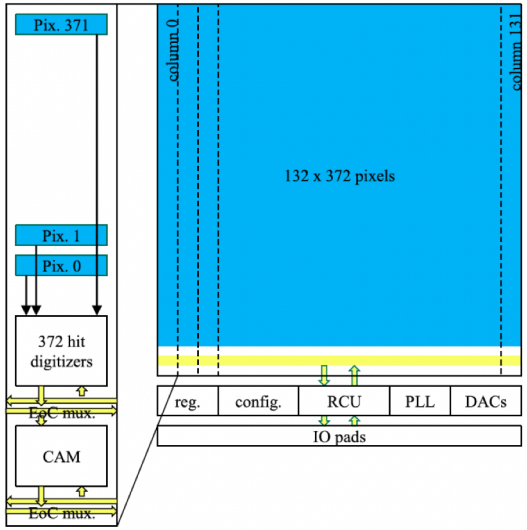
HVCMOS： a promising technology



- High-Voltage CMOS
  - Full depletion possible due to large electrode
  - Intrinsically **radiation hard**
  - **Fast charge collection**
  - Relatively larger capacitance: noise, power
  - Based on commercially available process without modification → **cost-effective**

- Current HVCMOS chips developed using 180n/150nm processes

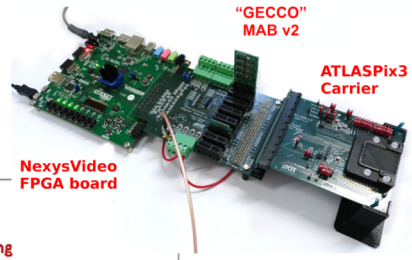


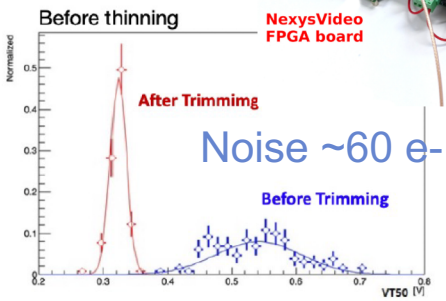


- ATLASPix3 features
  - TSI 180nm HVCMOS on 200 Ωcm substrate
  - Pixel size 50 × 150 μm^2
  - 132 columns × 372 rows
  - 20.2 × 21 mm^2 reticle size
  - Each pixel has 7-bit TOT + 10-bit timestamp
  - Continuous / triggered readout with 8b10b / 64b66b coding
  - Power consumption ~160 mW/cm^2.

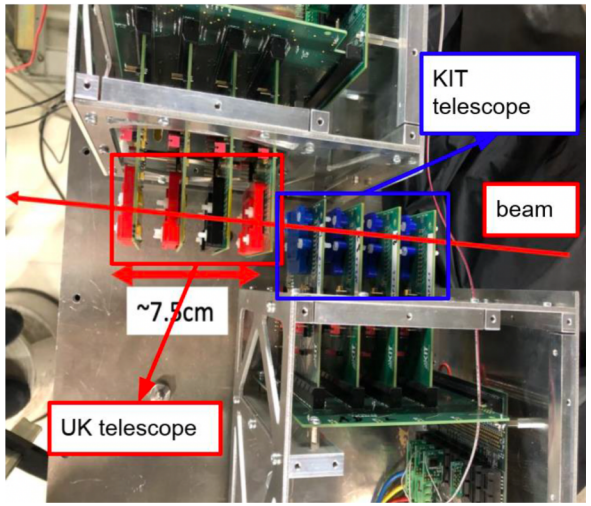
Development based on ATLASPix3

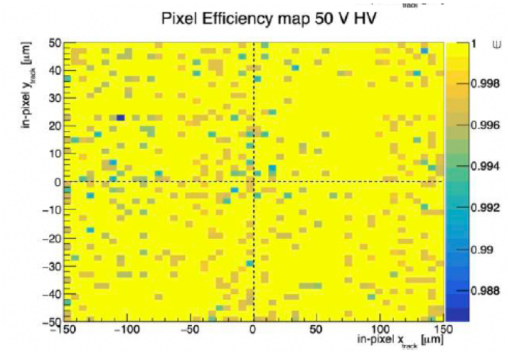
- Extensive characterization for ATLASPix3, including two test beam campaigns
- 4-chip readout unit (Quad module) developed



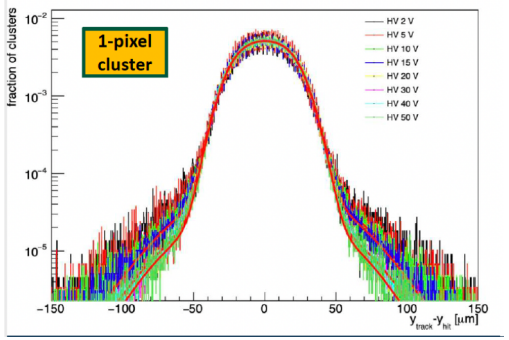


Sigma: 66.31 mV -> 12.17 mV

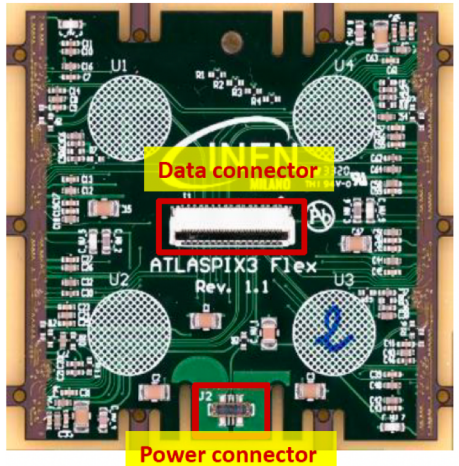


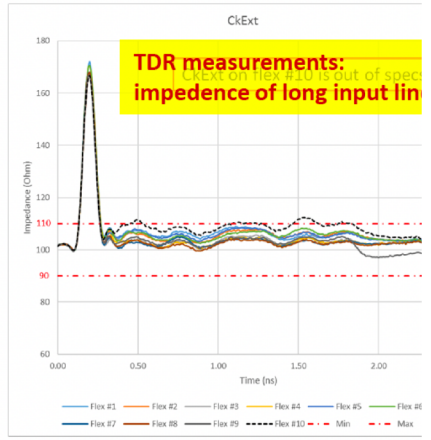


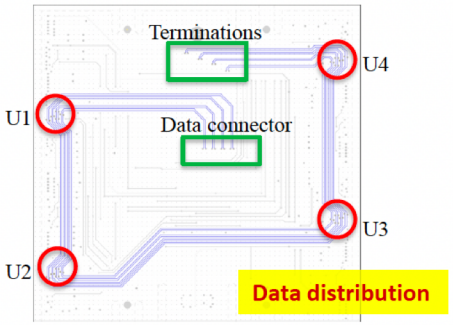
Efficiency > 99%

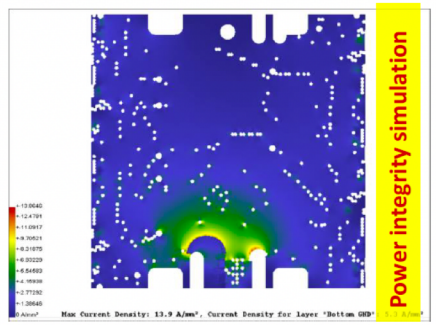


Resolution ~11um





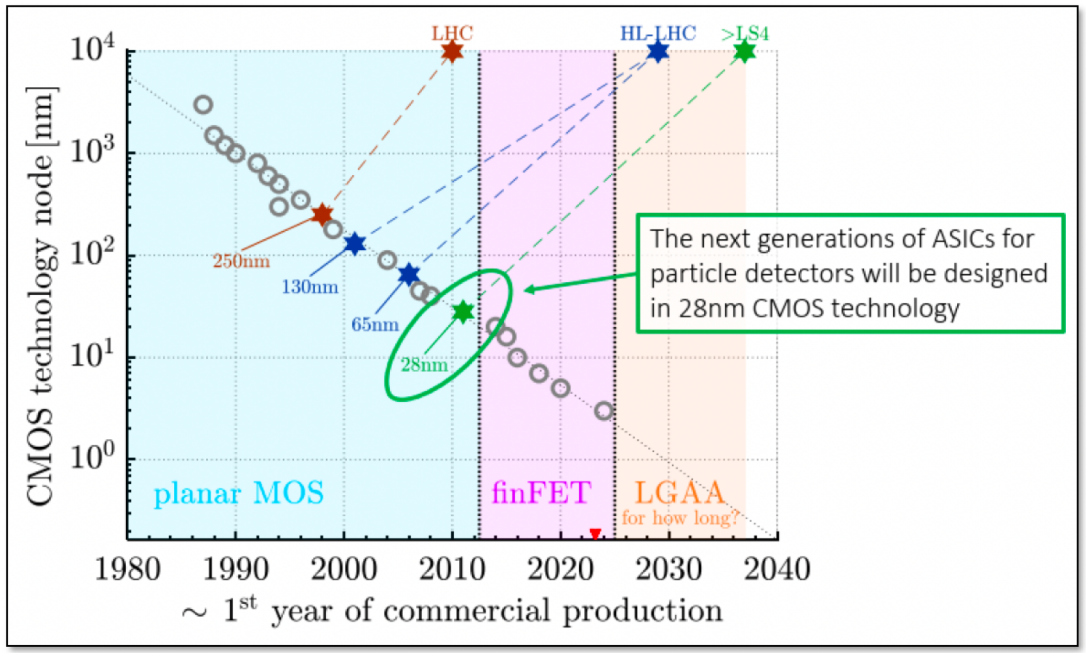




Riccardo Zanzottera's talk : The ATLASPIX3 CMOS pixel sensor performance
Attilio Andreazza's talk : The IDEA silicon tracker

Towards smaller feature size

- For better performance
  - Higher circuit density
  - More functionality in the same area
  - Less power consumption
- For higher reliability
  - R&D phase of HEP experiments are usually long (comparing to commercial world)
  - Will the process available for mass-production?
  - Example of TSI-180nm process
- Development for 65nm CMOS (MAPS of small fill-facor) has started
  - Key R&D theme in ECFA detector roadmap



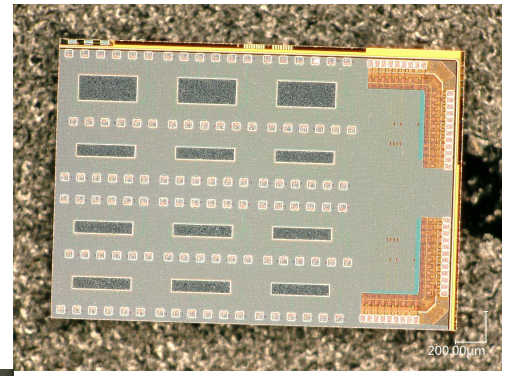
P. Moreira @ CEPC workshop, Oct 2023

Development in small feature size HVCMOS

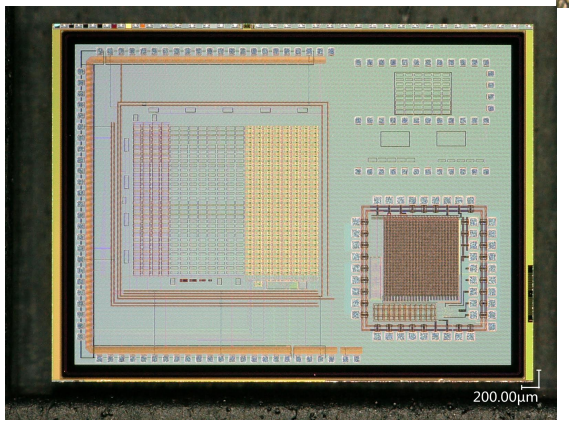
- HLMC 55nm HVCMOS process
  - Cancelled MPW plan in 2022
- SMIC 55nm Low-Leakage process
  - Not HV, yet with a similar deep n-well structure
  - MPW submitted in Oct 2022 in normal wafer
  - COFFEE1 received in Apr 2023
- SMIC 55nm HVCMOS process
  - HVCMOS process, with 1kΩ ·cm wafer
  - MPW submitted in Aug 2023
  - COFFEE2 received in Dec 2023

CMOS SENSOR IN FIFTY-FIVE NM PROCESS

COFFEE1



COFFEE2

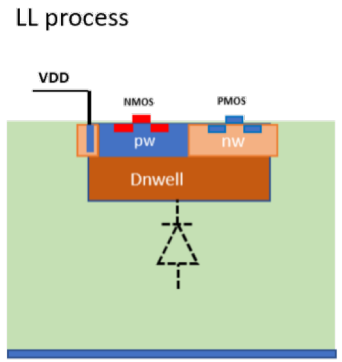


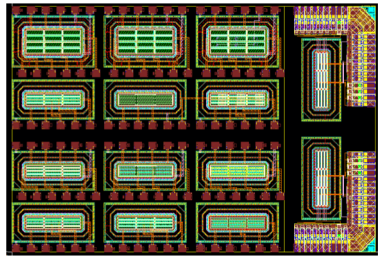
Karlsruher Institut für Technologie

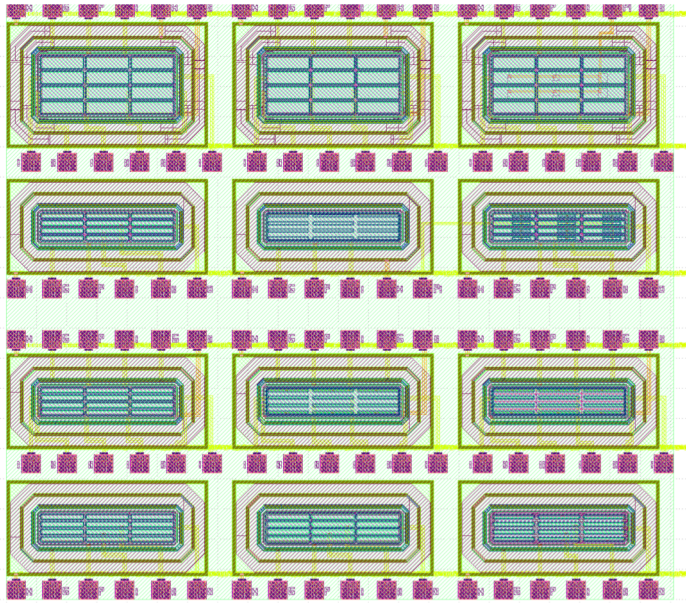
NB: All dimensions mentioned in 55nm process always has a scale factor of 0.9.
As it is scaled down from 65nm masks

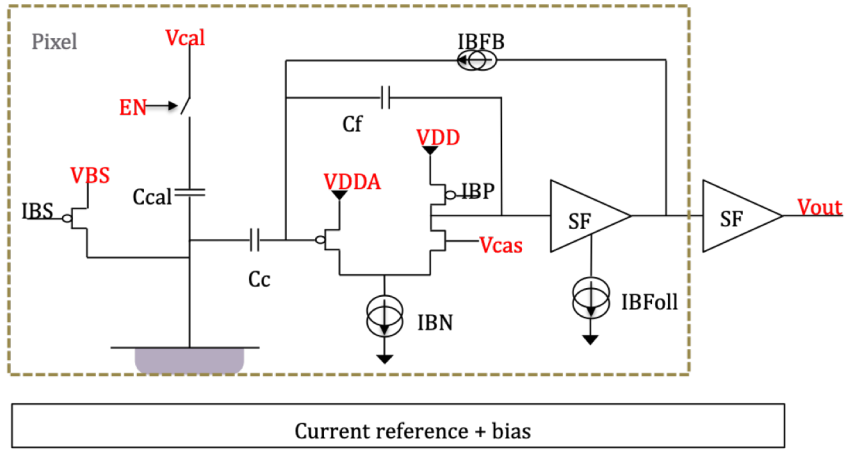
COFFEE1: MPW in LL process

- MPW submitted in Oct 2022 with SMIC 55nm Low Leakage process
  - NB: not an HV process! Yet it has similar deep N well separating the transistors and the sensor part
  - 3 × 2 mm² in area
  - Low resistivity wafer
- Variation of passive diode arrays
  - Pixel size: 25×150 μm^2 or 50×150 μm^2
  - With/w.o. p-stop
  - Space between pixels: 5/ 10/ 15 um
- Simple amplifiers added



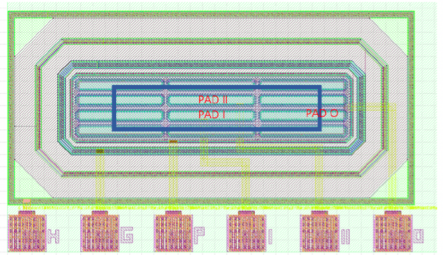


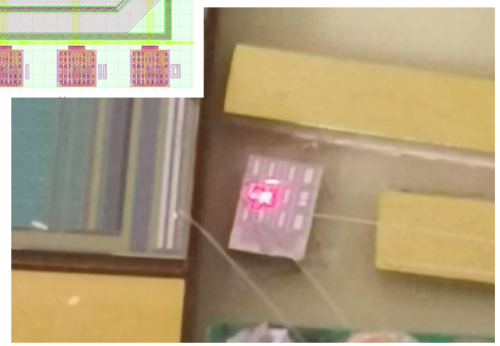


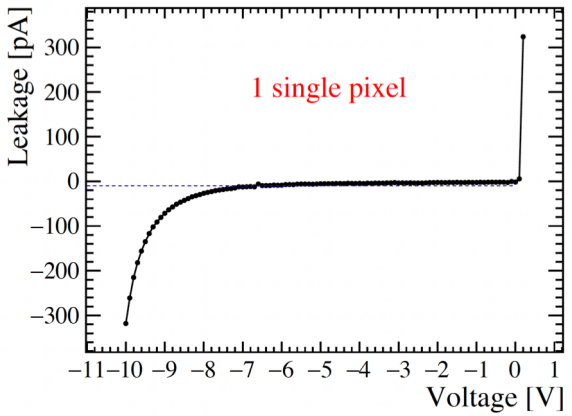


COFFEE1 tests

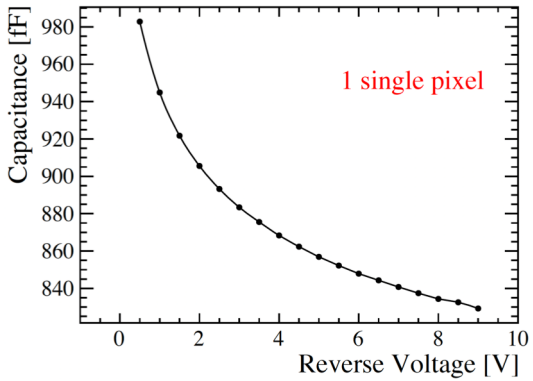
- IV curves show breakdown voltage ~ $-8\ V$
  - Expected for low-resistance wafer
- CV curves measured for 1 pixel or 10 pixels connected
  - With offset subtracted the capacitance of a single pixel of $25\times150\ \mu m^2$ is 150~200 fF
- Small yet clear signal response to laser
  - Corresponding to charge of ~2400 e-



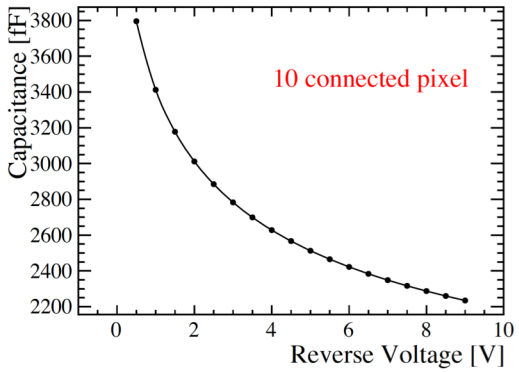


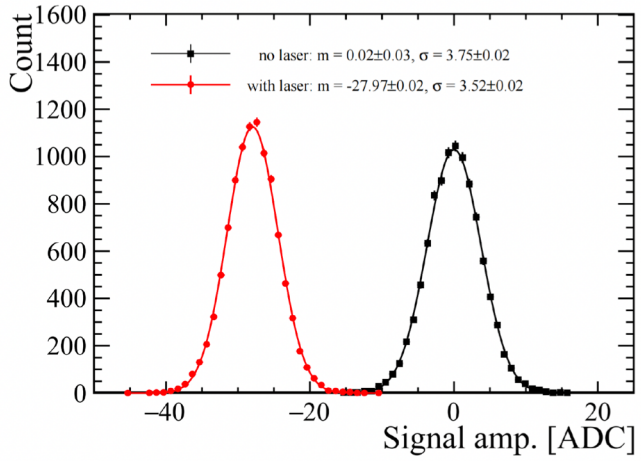


1 single pixel
$C \sim (180\times1 + 500)$ fF



10 pixels in parallel
$C \sim (180\times10 + 500)$ fF

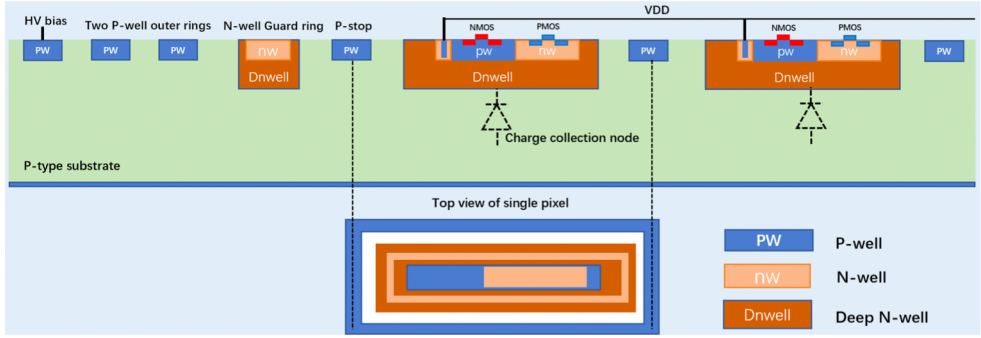




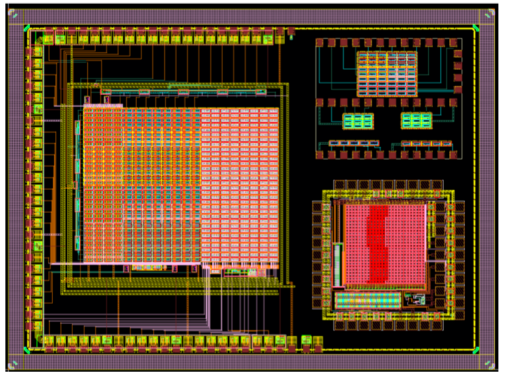
COFFEE2: MPW in HVCMOS process

- MPW with SMIC HV 55nm
  - High-res wafer of 2k or 1k Ωcm available
  - Real validation of the sensor
  - 4mm * 3mm in area
  - Passive arrays similar as COFFEE1
  - Two pixel arrays with in-pixel amplifier and more digital design
  - Submitted in Aug 2023
  - Received in Dec 2023

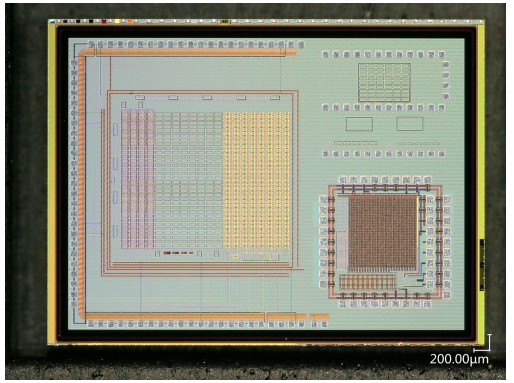
Cross-section of pixel strucure



COFFEE2 floorplan



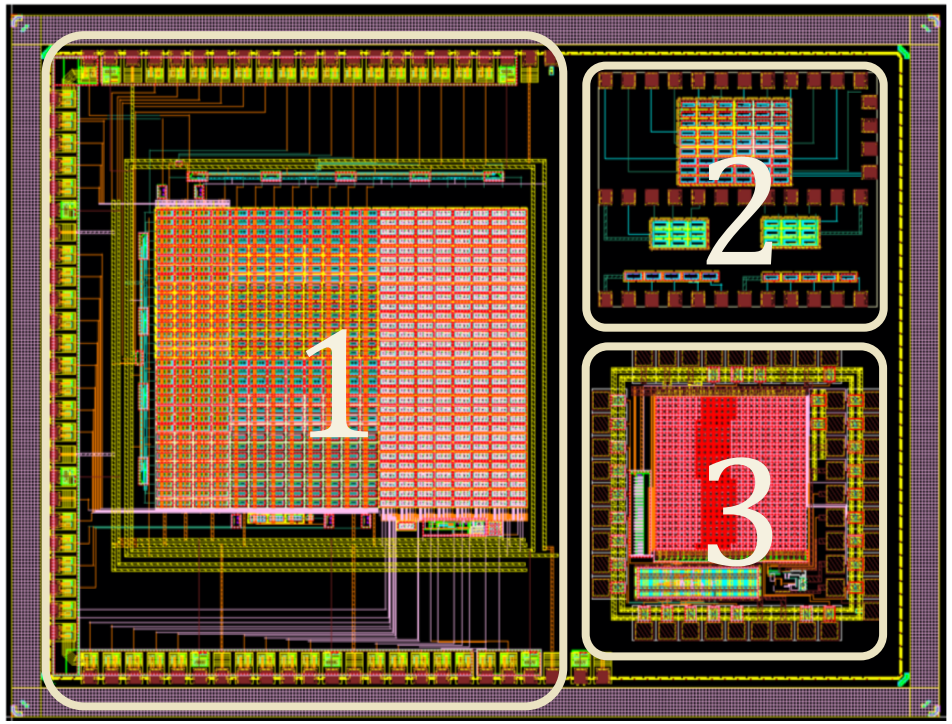
COFFEE2 photo



COFFEE2 design

1. 32 × 20 pixel matrix with various diodes and in-pixel amplifier or discriminator designs for process validation
   - $40 \times 80\ \mu m^2$
   - 5/10/15um gap btw pixels
   - With/ w.o. p-stops
   - 2 version in-pixel electronics

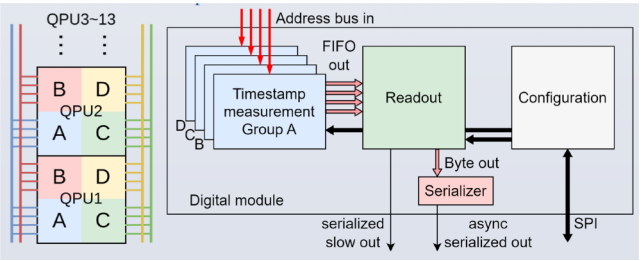
2. passive diode arrays, each has 3×4 pixels of size $40 \times 80\ \mu m^2$ for study on sensing diode and charge sharing



* Pixel size choice: similar area as $25 \times 150\ \mu m^2$ but less elongated

IHEP, Shandong Univ., Zhejiang Univ.

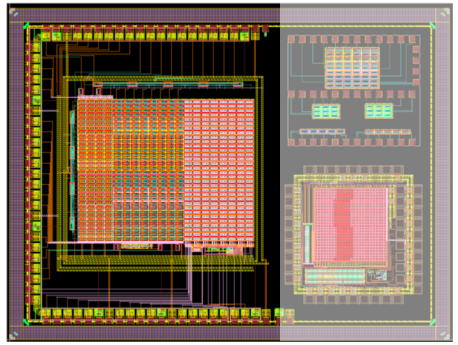
3. 26 × 26 pixel matrix of $25 \times 25\ \mu m^2$ pixels with digital readout periphery for novel electronics structure study

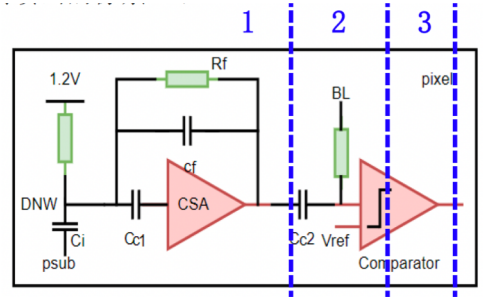


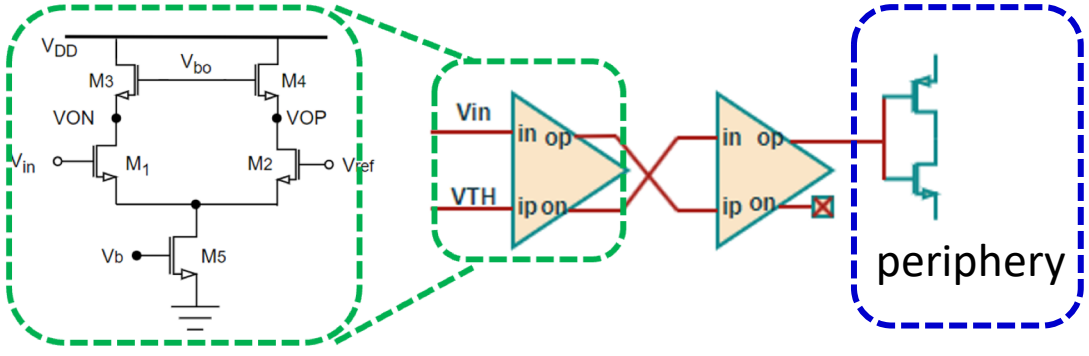
KIT, IHEP

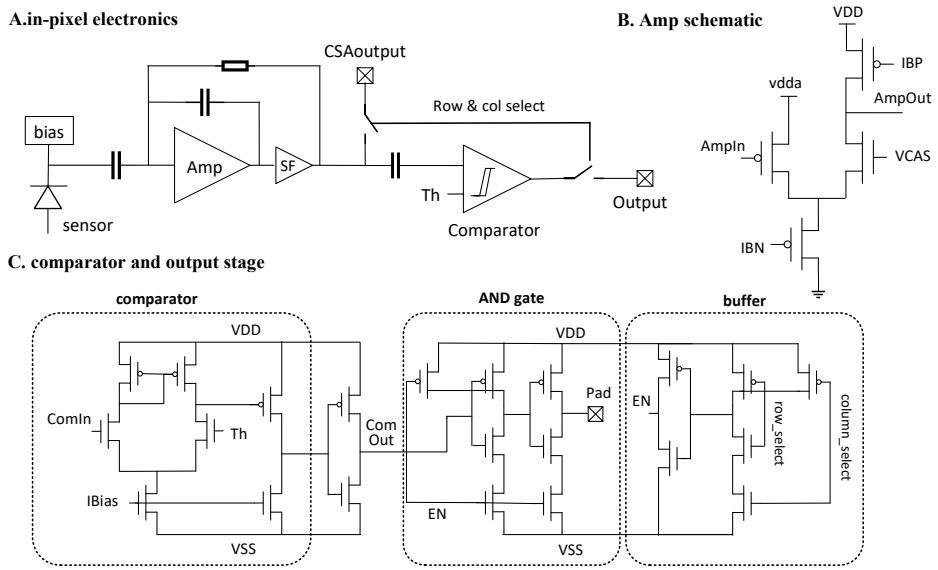
Design and test of in-pixel circuit

- Three types of in-pixel electronics
  - 1 – analog readout only
  - 2 – CSA + NMOS comparator -> ADC in periphery
  - 3 – CSA + CMOS comparator, digital output
  - A pixel is read out by row/column selector



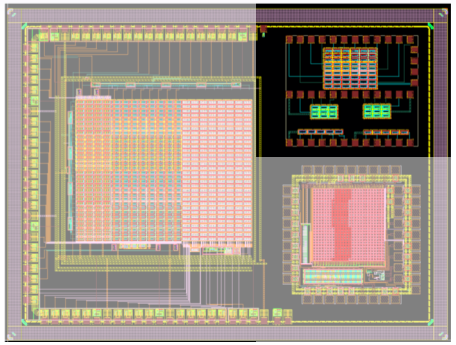


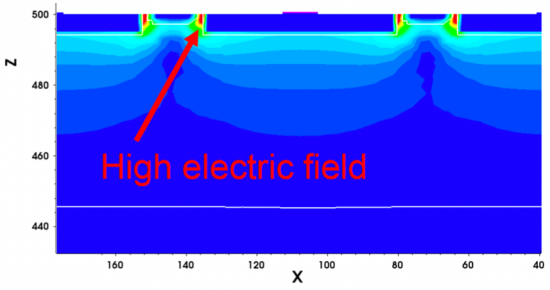


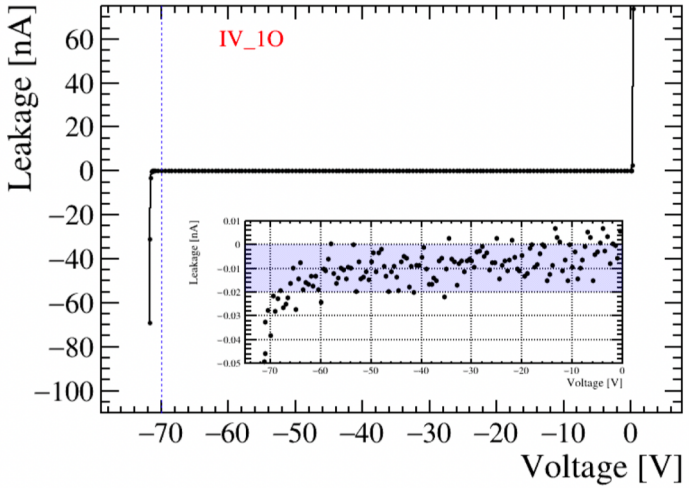


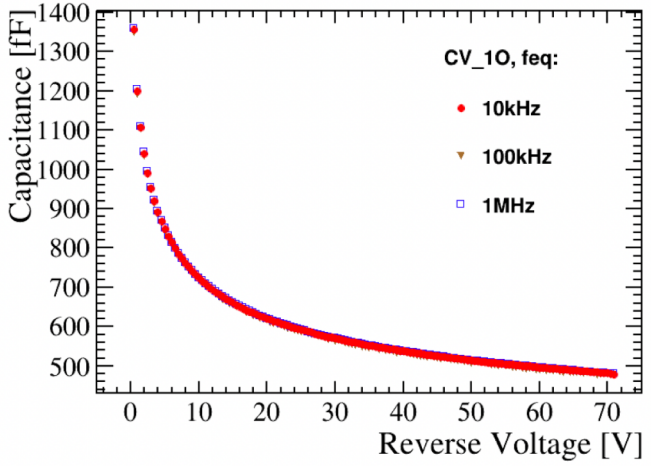
First tests of COFFEE2 sensors

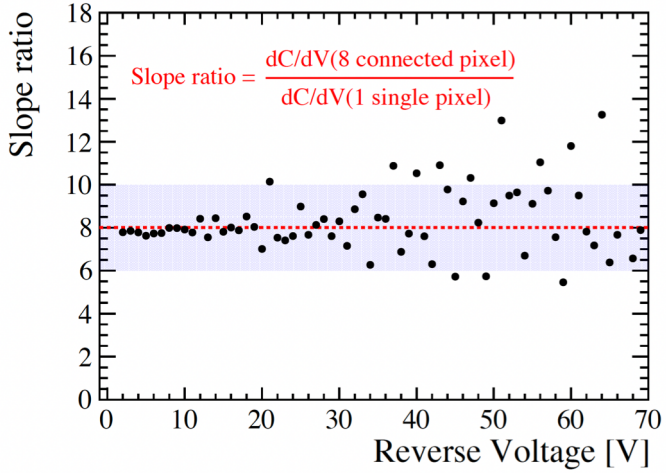
- Breakdown voltage up to – 70V
- Full depletion not yet reached at breakdown
  - Confirmed by simulation
  - Due to p-well right next to the edge of deep n-well
- Capacitance (with offset subtracted) scales with sensor area







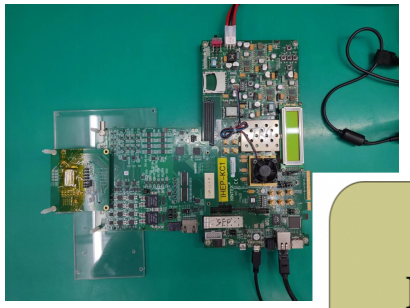


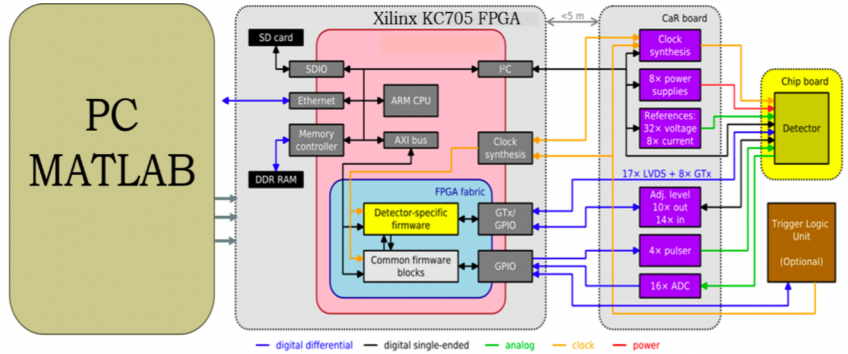


dC(8)/dV = 8* dC(1)/dV

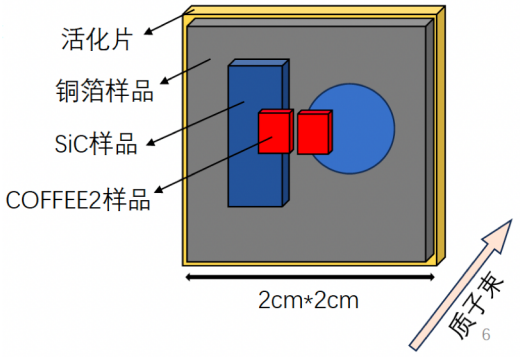
Future R&D using 55nm process

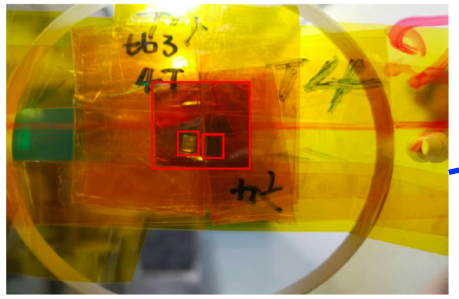
- Thorough characterization of COFFEE2
  - Test board ready, firmware being tuned
  - Sensor irradiated up to ~ $1\times10^{15} n_{eq}/cm^2$

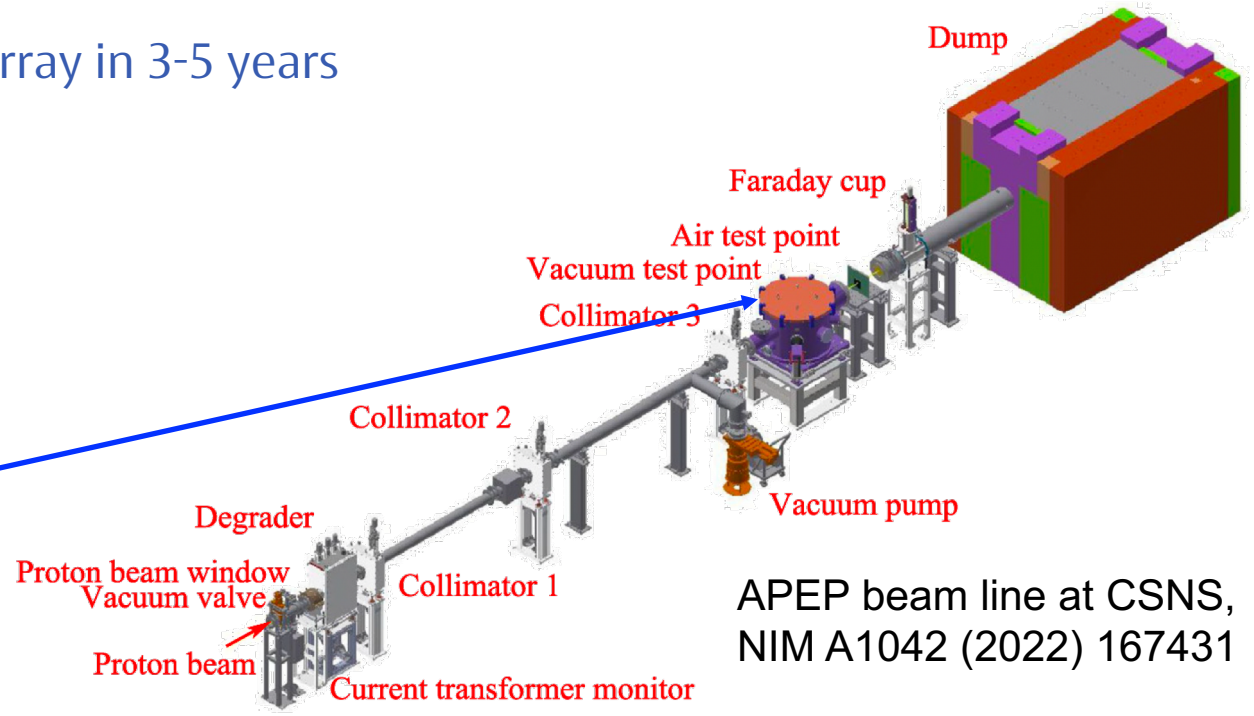




- MPW to implement small pixel array, with more in-pixel functions (eg. Timestamping)
  - Earliest MPW opportunity in Oct 2024
  - Eventually a prototype chip with larger array in 3-5 years



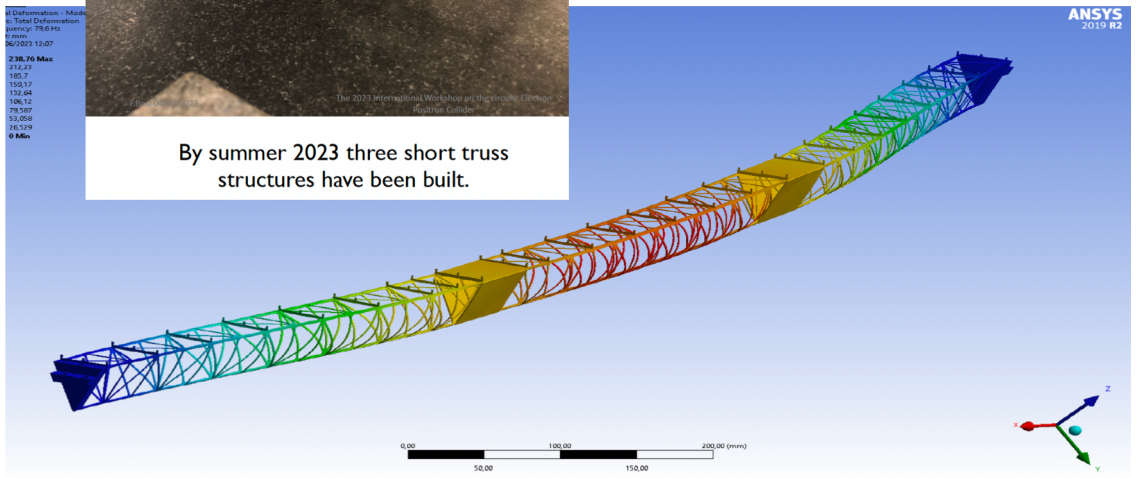




APEP beam line at CSNS, NIM A1042 (2022) 167431

Mechanical design

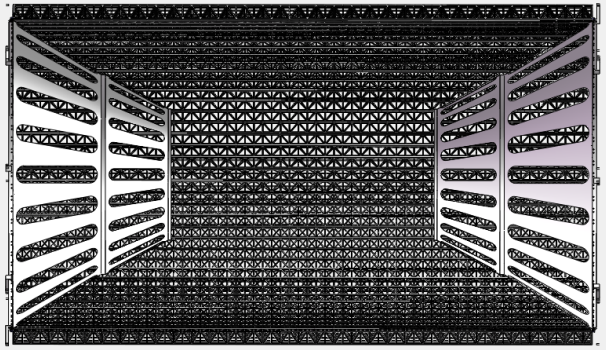
- Design, simulation and prototyping for 2nd SIT layer in CDR baseline
- Dedicated mechanical design ongoing for rdTDR



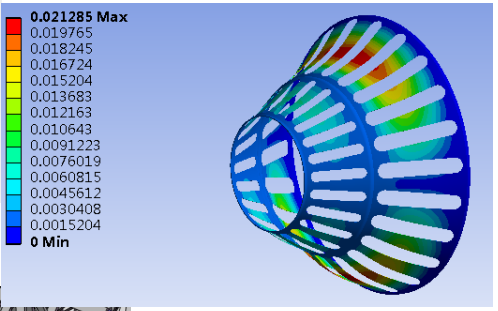
Simulated sagitta is 582 μm for two 200g loads

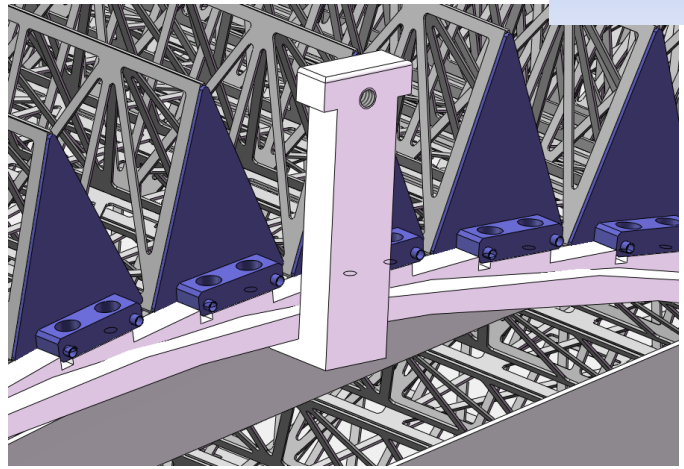
INFN Pisa

Supporting structure for 3-layer inner barrel



Simulated deformation under self weight





Outermost layer can be attached to the gas detector

IHEP CAS

Summary

- To tackle the technical challenges of CEPC silicon tracker, a lot of R&D work ongoing

- HVCMOS is a most promising technology under study
  - Prototyping has been going on with chip in 180nm process
  - Development for 55nm HVCMOS started with 2 MPWs, first results promising
  - Module and mechanical design are progressing

Thank you for your attention

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Your participation is welcome!