The IDEA Silicon Tracker

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For the IDEA Detector Concept Community

INFN MILANO

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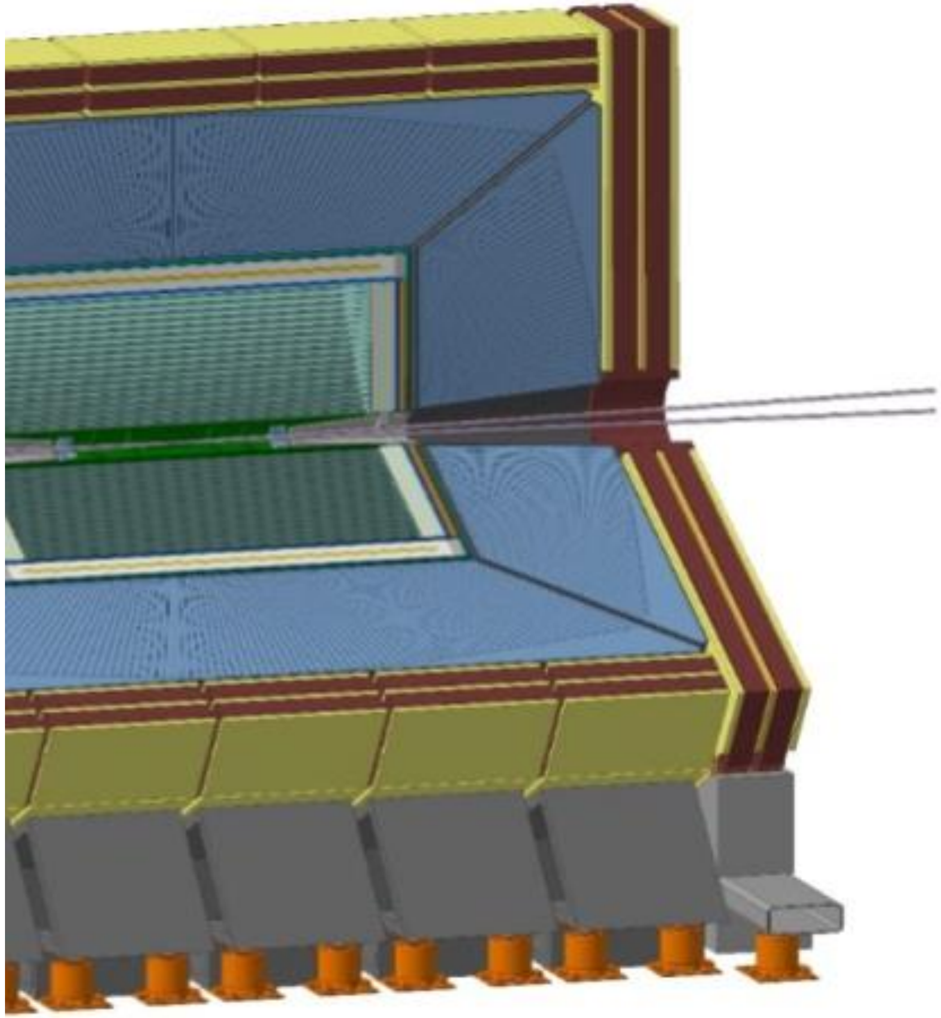
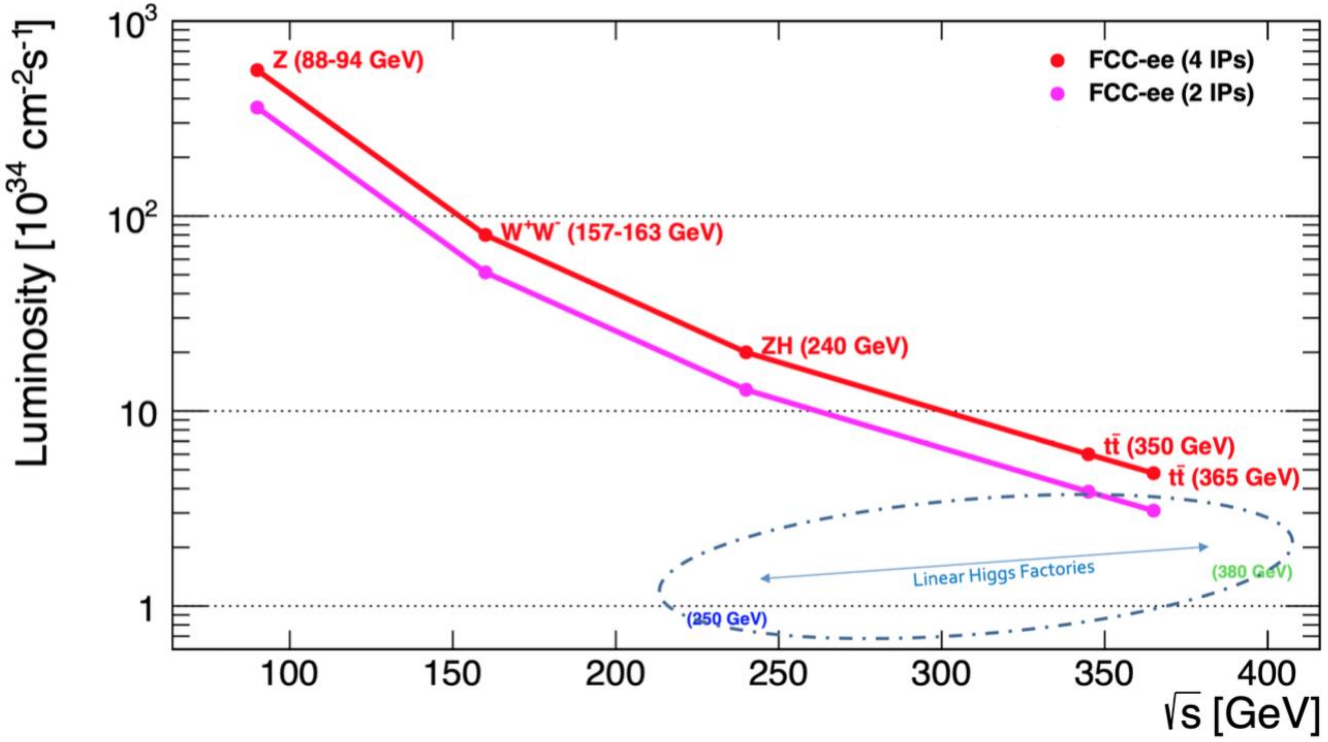
Outline

- Requirement for operation at future Higgs factories
- The IDEA Detector concept
- Silicon tracking in IDEA:
  - Technologies
  - Inner Vertex Detector
  - Outer Vertex Detector
  - Silicon Wrapper
- Conclusions and outlook



Physics requirement at Higgs Factories

- Rich physics program at future Higgs Factories
  - ZH, but also tera-Z, WW and tt threshold
- Physics performance mostly determined by the Higgs physics program
- Operating condition (data rate, background) from the high-luminosity at the Z pole



- Impact parameter resolution

$$\sigma_d < 3\ \mu\text{m} \oplus \frac{15\ \mu\text{m} \cdot \text{GeV}}{p\sin^{3/2}\theta}$$

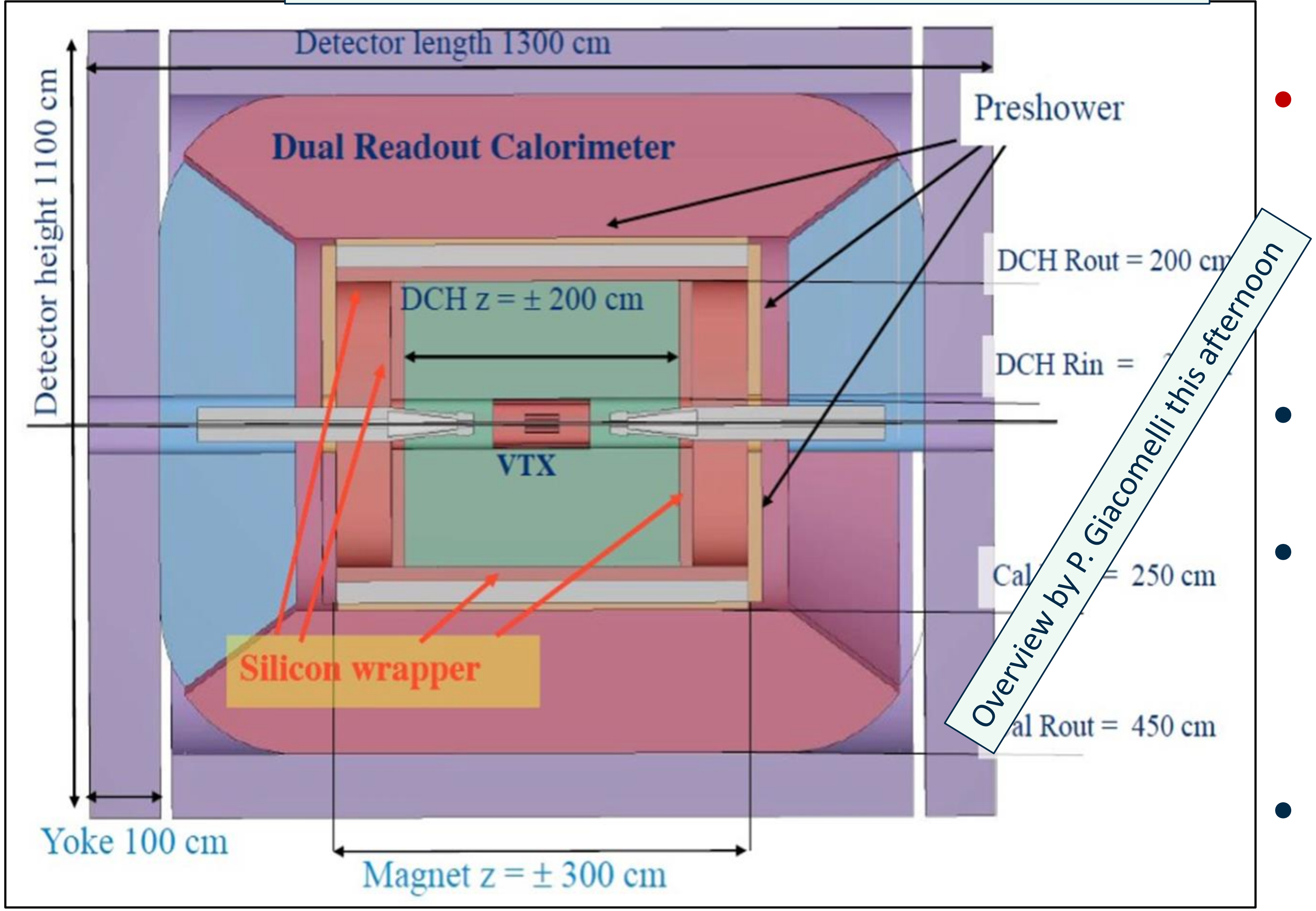
- Momentum resolution

$$\frac{\sigma_p}{p} < 2 \cdot 10^{-5}\text{GeV}^{-1}p \oplus \frac{b}{\sin\theta}$$

- Hit rate near to the beam-pipe **250 MHz/cm²** (background dominated)
- Bunch spacing: **20 ns**
- Z production rate **O(10 kHz)**

The IDEA Detector Concept

Innovative Detector for e^+e^- Accelerator



- Central tracking device:
  - light Drift CHamber
- **Silicon detectors for precision measurements**
  - **inner vertex detector**
  - **outer vertex detector**
  - **silicon wrapper/TOF**
- Thin solenoid with 2T field (according to MDI limits)
- Dual readout calorimeter
  - supplemented by a pre-shower

A. Loeschcke Centeno's and R. Santoro's talks this afternoon

- Muon chambers in the solenoid return yoke

F.M. Melendis's talk yesterday

Si Detector Technologies

- Focus on **depleted monolithic CMOS detectors**
  - High-Voltage/High-Resistivity CMOS processes commercially available
  - CMOS Foundries are able to produce large volume of detectors at a convenient price
  - Depleted region provide fast rising and "high-amplitude" signals
  - No need of the complex and costly interconnection technique used in hybrid detectors
- Two baseline technologies presented in this talk:
  - **ARCADIA** – INFN/LFoundry driven development, collaborations with PSI
    - fully depleted sensors, with high granularity and low power consumption for the **Inner Vertex Detector**
  - **ATLASPIX3** – KIT, China, INFN, UK collaboration
    - full reticle size detector, implementing most features needed for deployment in the **Outer Vertex Detector and Si Wrapper**
- **Options under consideration**
  - **Curved layout**, ALICE ITS3 inspired, for the Inner Vertex Detector
  - **Resistive Silicon Detectors**, with **tens of ps time resolution** are considered as an opportunity for the Silicon Wrapper (showing results from Torino, Trento, Perugia and FBK collaboration)

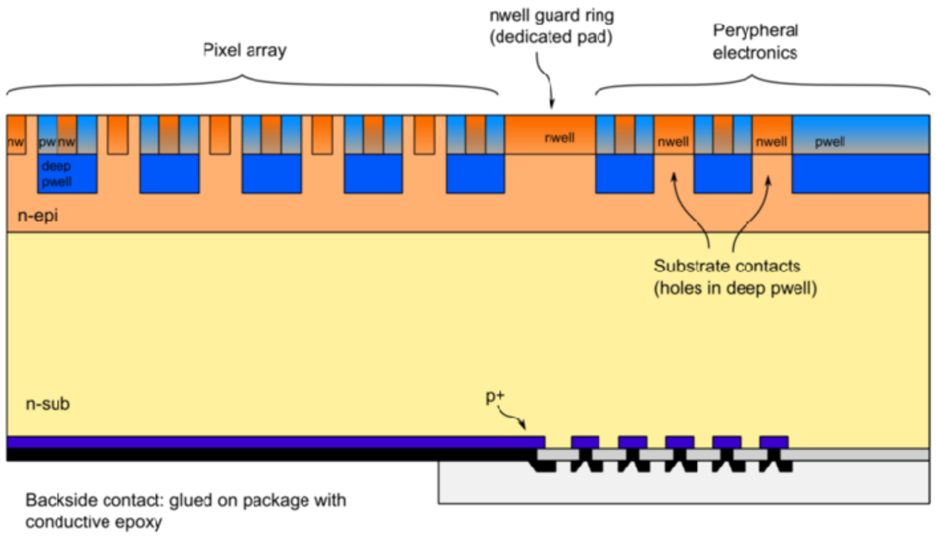
INNER VERTEX DETECTOR

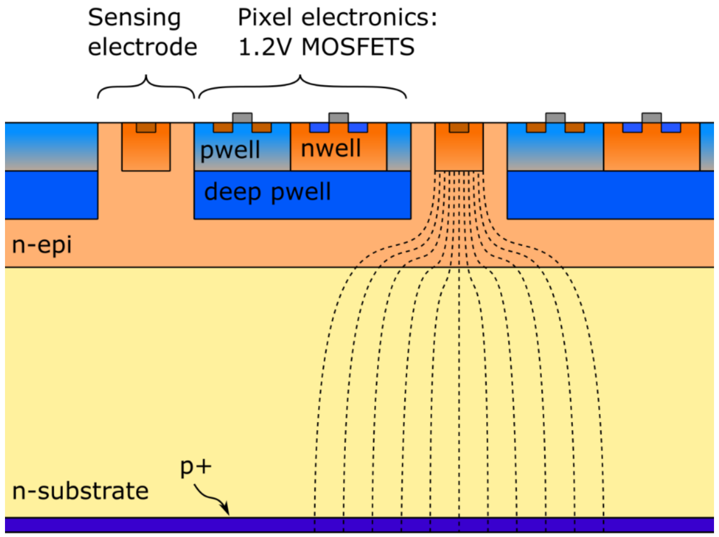
ARCADIA

Advanced **R**eadout **C**MOS **A**rchitectures with **D**epleted **I**ntegrated sensor **A**rrays

Fully Depleted Monolithic Active Pixel CMOS sensor technology platform allowing for:

- Active sensor thickness in the range 50 μm to 500 μm;
- Operation in **full depletion** with fast charge collection by drift
- **Small collecting electrode** for optimal signal-to-noise ratio;
- Scalable readout architecture with ultra-low power capability O(**10 mW/cm^2**);
- Compatibility with standard CMOS fabrication processes: concept study with small-scale test structure (SEED), technology demonstration with large area sensors (ARCADIA)
- Technology: **LF11is** 110nm CMOS node (quad-well, both PMOS and NMOS), high-resistivity bulk
- Custom patterned backside, patented process developed in collaboration with LFoundry





ARCADIA: MD3 demonstrator

- Demonstrator layout:
  - **Top Padframe** Auxiliary supply, IR Drop Measure
  - **Matrix**
    - 512x512 pixels, Double Column arrangement
    - 25x25 μm^2 pixels
    - Clockless
  - **End of Sector (x16)** Reads and Configures 512x32 pixels
  - **Sector Biasing (x16)** Generates I/V biases for 512x32 pixels
  - **Periphery**
    - SPI, Configuration, 8b10b enc, Serializers
    - Triggerless data-driven readout
    - Event rate up to 100 MHz/cm^2
    - High-rate operation (16 Tx): 17-30 mW/cm^2
    - **Low-power operation (1 Tx): 10 mW/cm^2**
  - **Bottom Padframe** Stacked Power and Signal pads

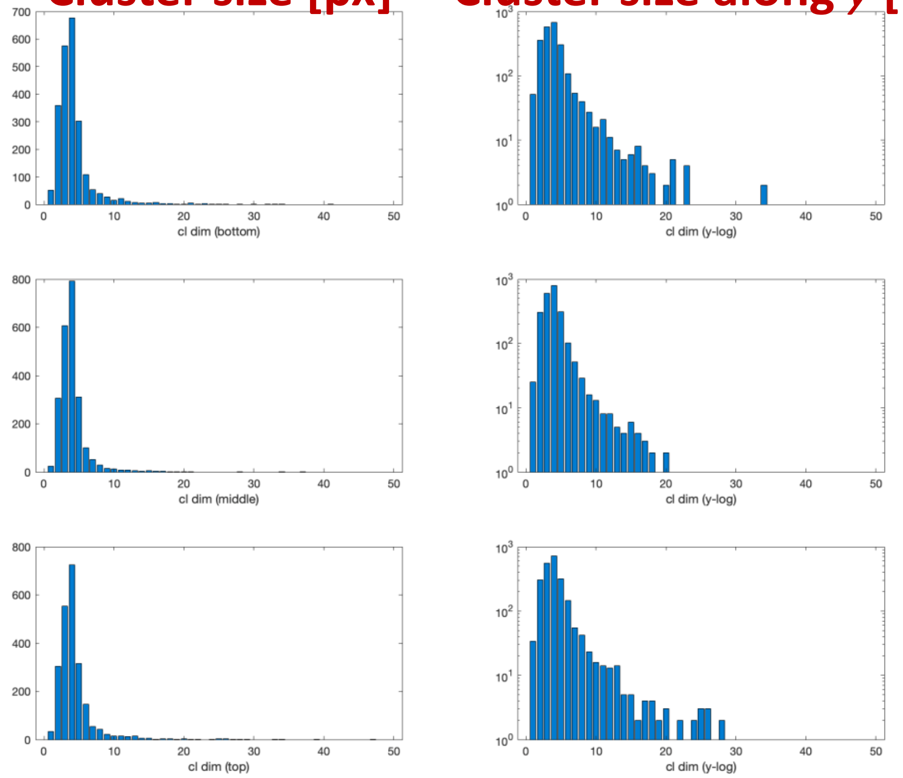
ARCADIA: MD3 Results with cosmics

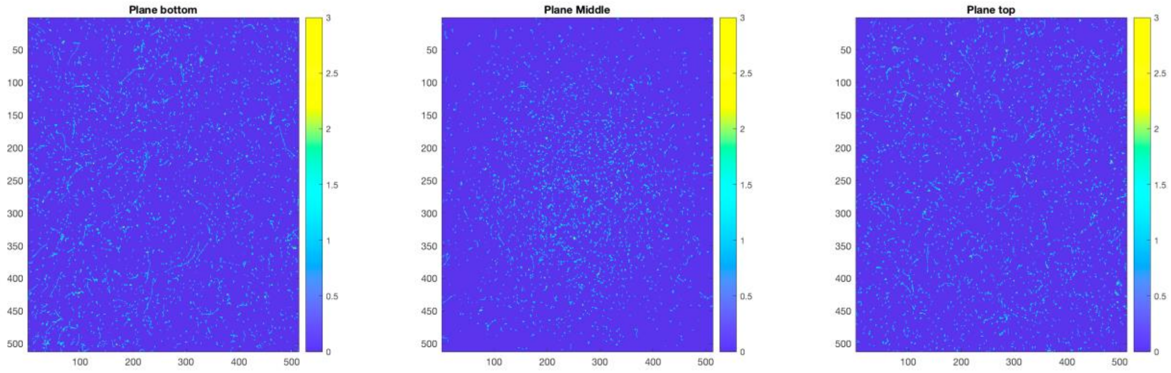
Cluster size [px] **Cluster size along *y* [px]**

Bottom layer

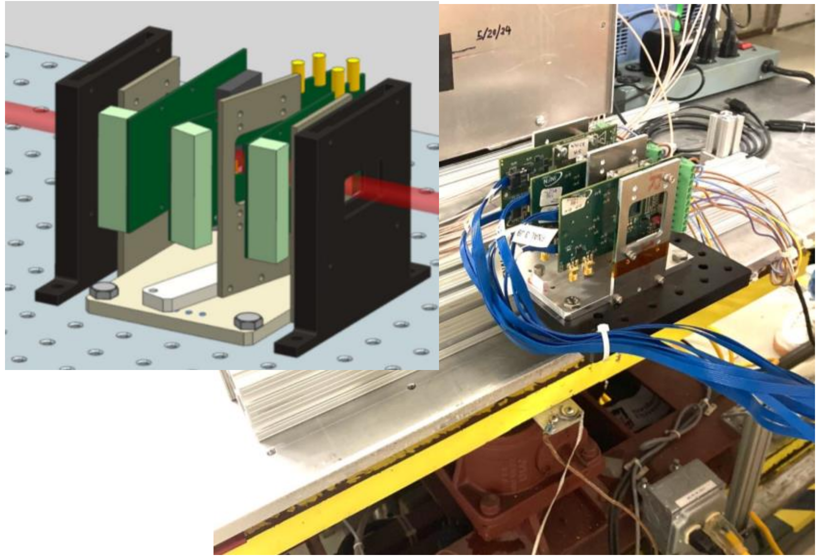
Middle layer

Top layer



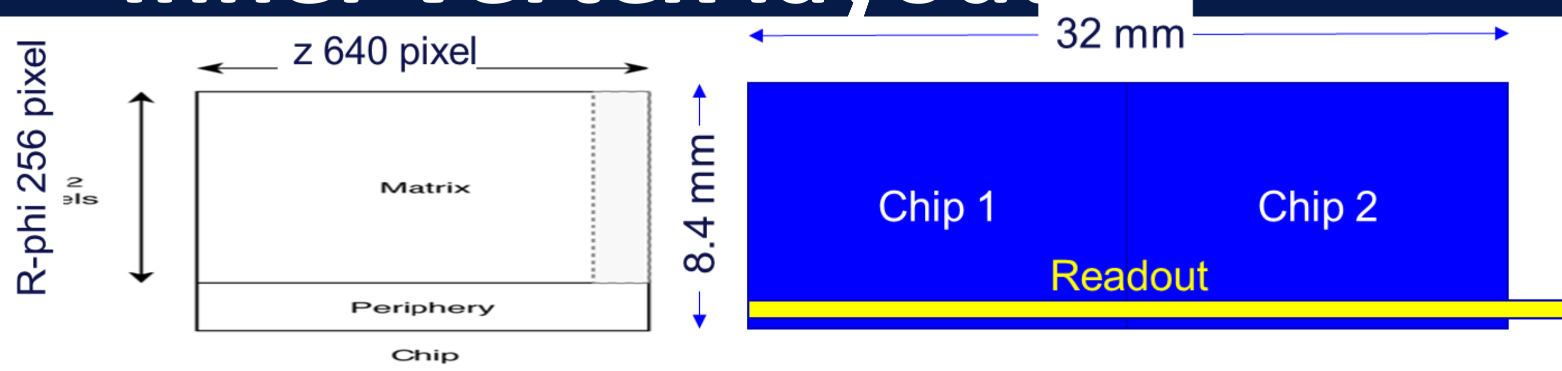


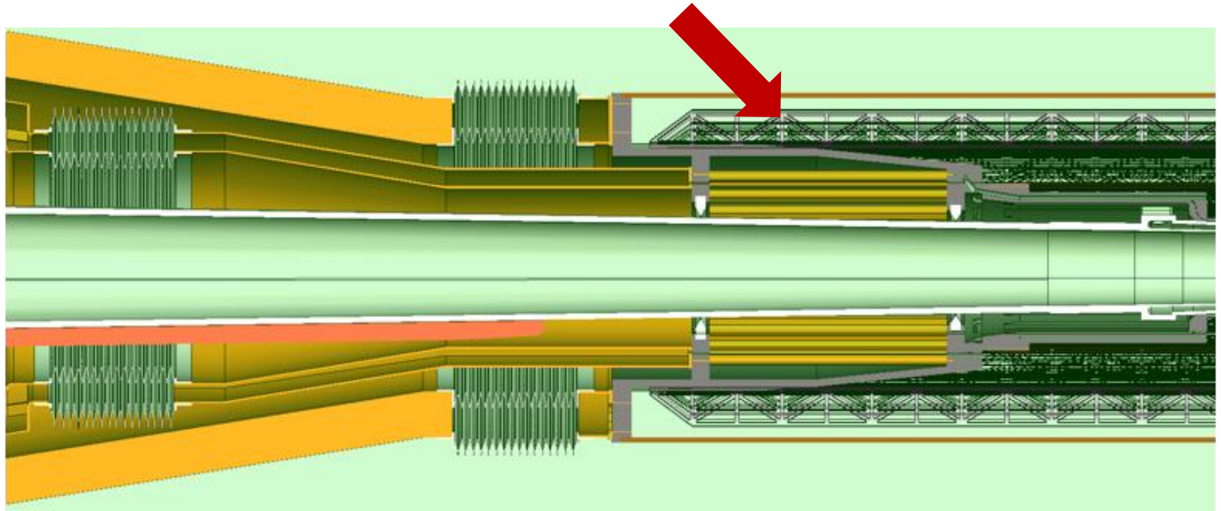
- Cosmic ray data taking: 1 week
- 3-plane MD3 installed on a black box
- Threshold 290 e-, MPV = 4 pixels
- More than 90% of clusters with less than 6 fired pixels
- Preliminary results on residuals show a standard deviation of 12-14 μm (multiple scattering...)
- **Testbeam just completed at Fermilab**



Inner vertex layout

- Module based on ARCADIA MD3 layout
- 3 barrel layers
  - 13.7, 23.7, 34/35.6 mm radii
- Sensor loaded on thin carbon-carbon support and flex PCB for powering and readout
  - Alice/Belle2 like stave approach
- Light truss structure to provide mechanical rigidity to the stave

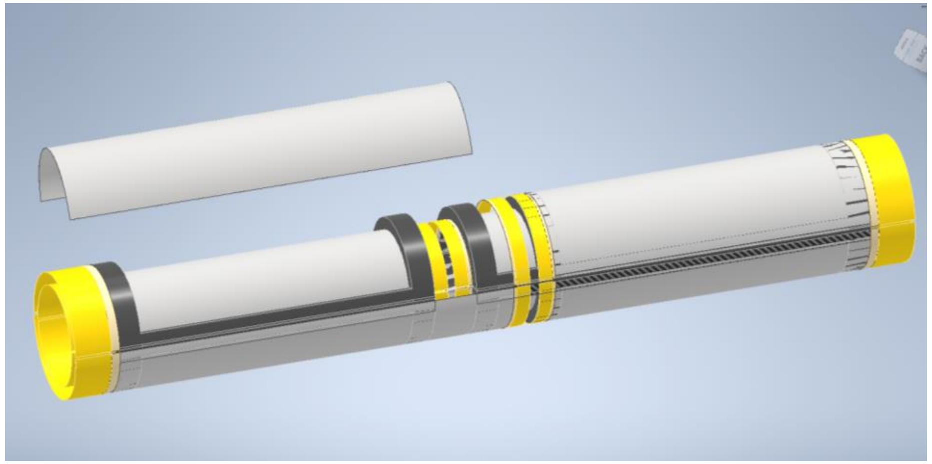


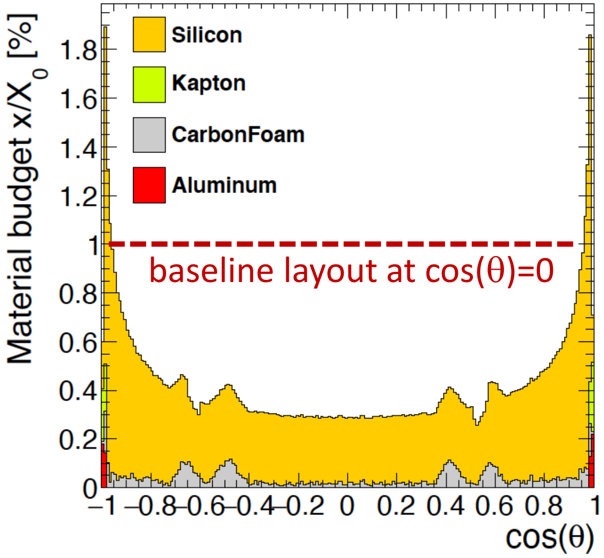


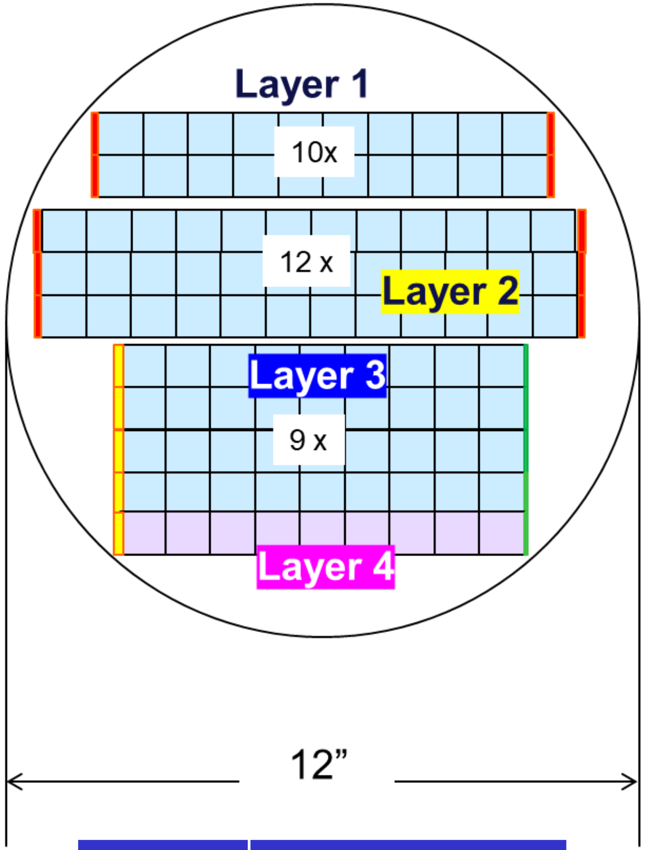
- Total detector weight 285 g
- 0.25% X_0 thickness per layer
  - Chips ~0.05% X_0, readout and power bus ~0.06% X_0
- Total power consumption 121 W
- **Air cooling is possible**
- Mockup construction and testing of the concept ongoing (LNF, Pisa, Perugia)

Alternative layout (stitched sensors)

- Curved layout inspired by ALICE ITS3 developments
  - adapted to the FCCee interaction region geometry and tracking coverage
  - 20.5x21.7 mm^2 pixel-matrix cell
  - 4 layers
  - Highest radii layers split in two sections due to wafer size and staggered to recover hermeticity
  - drastic improvement in material budget







Layer	Radius [mm]
1	13.7
2	20.2
3	26.8
4	33.3

OUTER VERTEX DETECTOR

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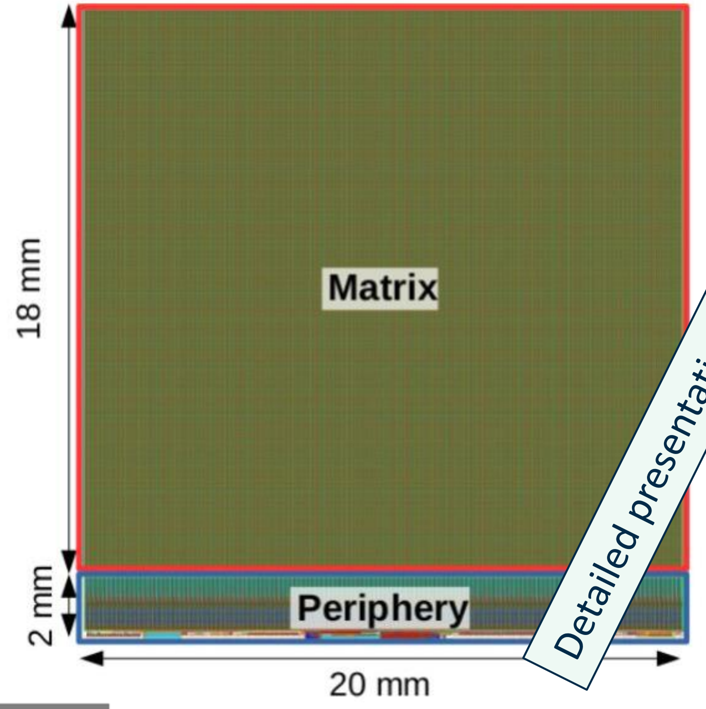
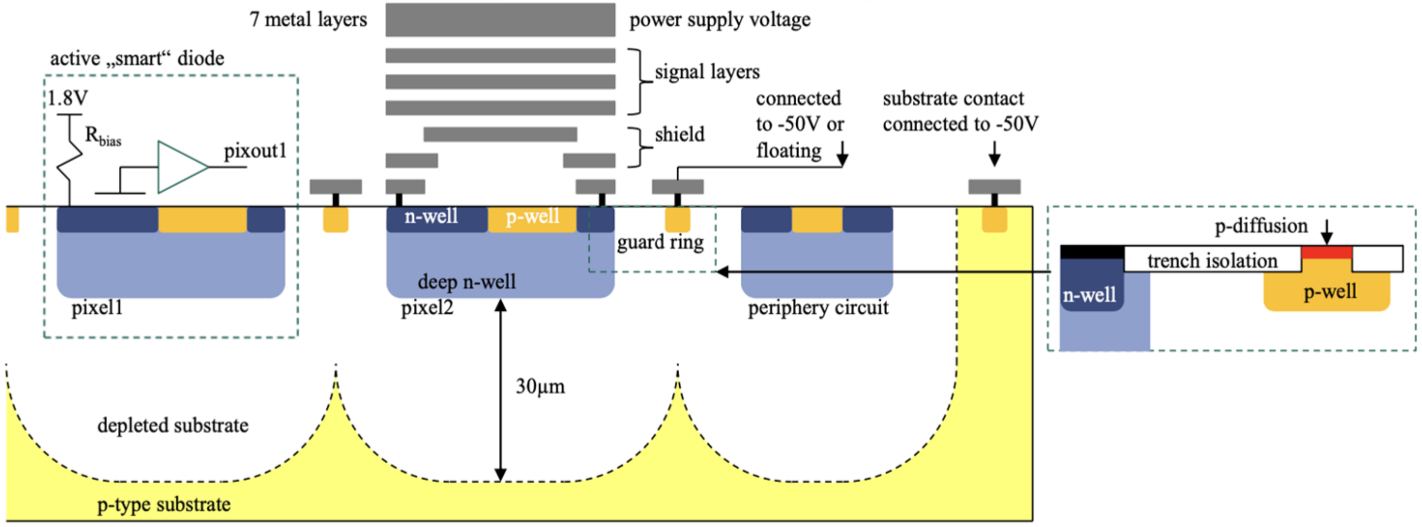
ATLASPIX3 Detector

- **ATLASPIX3 general features**
  - **TSI 180 nm HVCMOS** technology
  - full-reticle size **20×21 mm²** monolithic pixel sensor
  - 200 Ωcm substrate (other substrates up to 2 kΩcm also possible)
  - **132 columns of 372 pixels**
  - **pixel size 50×150 μm²** (25×150 μm² on recent prototypes)
  - **breakdown voltage ～-60 V**
  - up to **1.28 Gbps downlink**
  - **25 ns timestamping**
  - analog pixel matrix, digital processing in periphery
- Both **triggerless** and **triggered** readout modes:
  - two End of Column buffers
  - 372 hit buffers for triggerless readout
  - 80 trigger buffers for triggered readout



Detailed presentation by R. Zanzottera



Serial Powering Chain

Distribution of power and data signals along the local supports

- **serial powering** to reduce dissipation on the distribution lines
- **minimize** the number of connections

Read-out units are:

- **multi-chip modules** (example 2x2 quad modules)
- (or large stitched detectors)

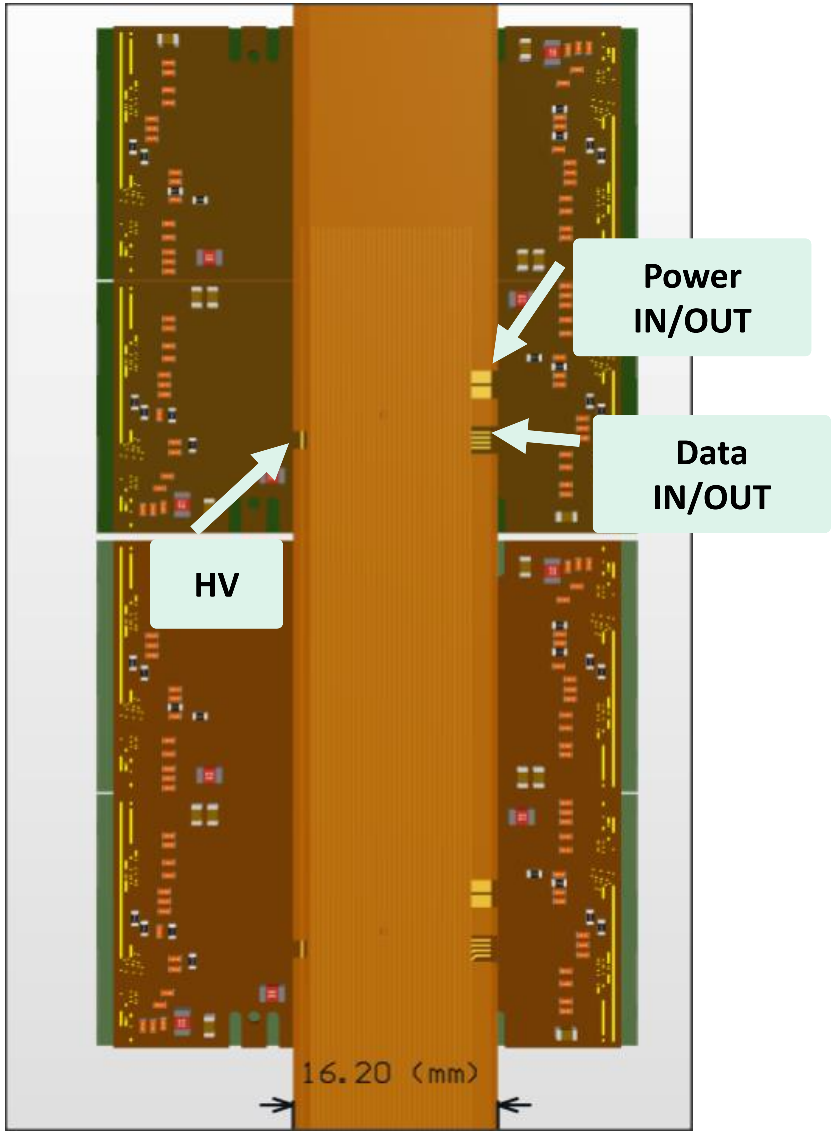
Minimal I/O connection on chip requires:

- Serial powering chain: all biases generated internally by shunt-LDO regulators
- chip-to-chip data transmissions: local data aggregation on module
- clock data recovery

not available on ATLASPIX3 modules

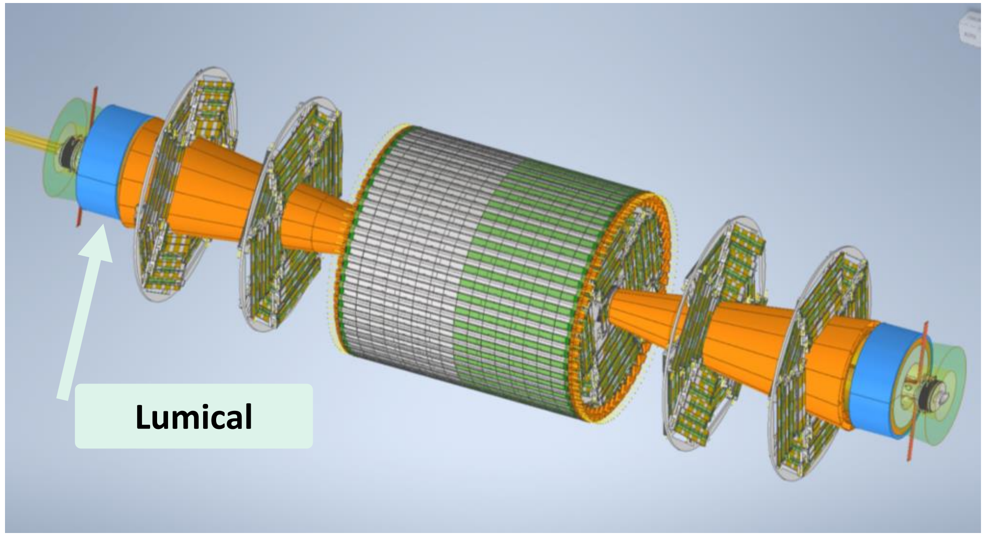
Reducing material by developing PCB with Al as conductor

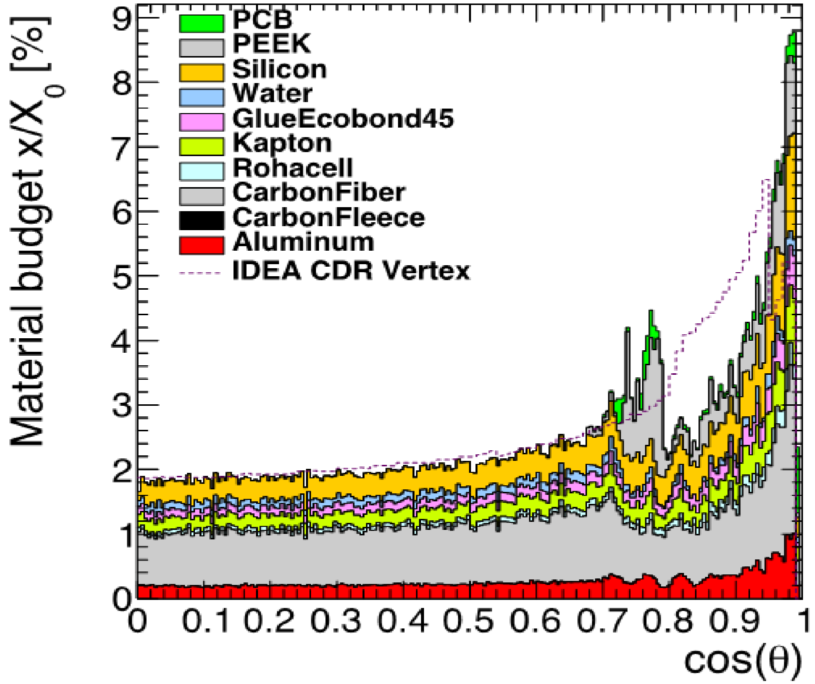
- on going design of PCBs to prototype a serial power chain

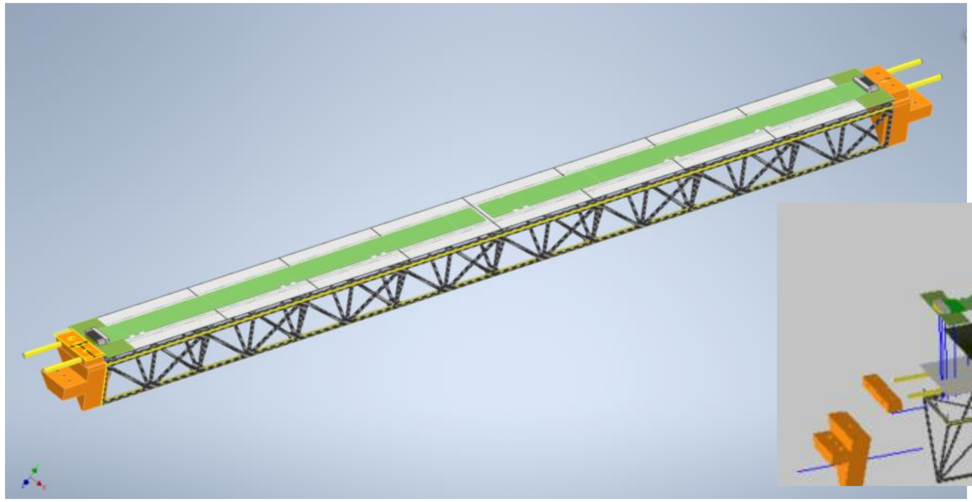


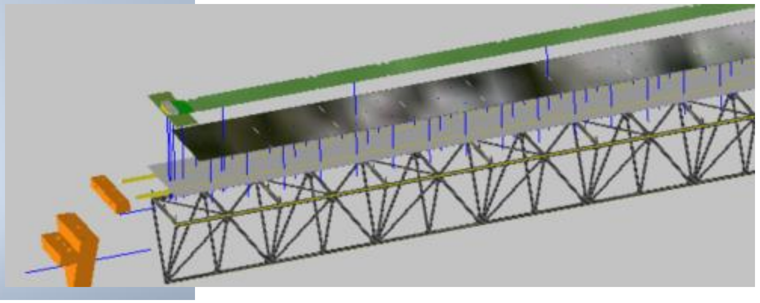
Outer Vertex Layout

- 2 barrel layers
  - 13 cm and 31.5 cm radii
  - covering $|\cos\theta| < 0.77$
- 2x3 Disks
  - $0.77 < |\cos\theta| < 0.99$
- Light stave truss
- Assuming 100 mW/cm^2, total power consumption 1742 W
- Thermal plate with light Kapton pipes for liquid cooling
- Module PCB provides important contribution to material





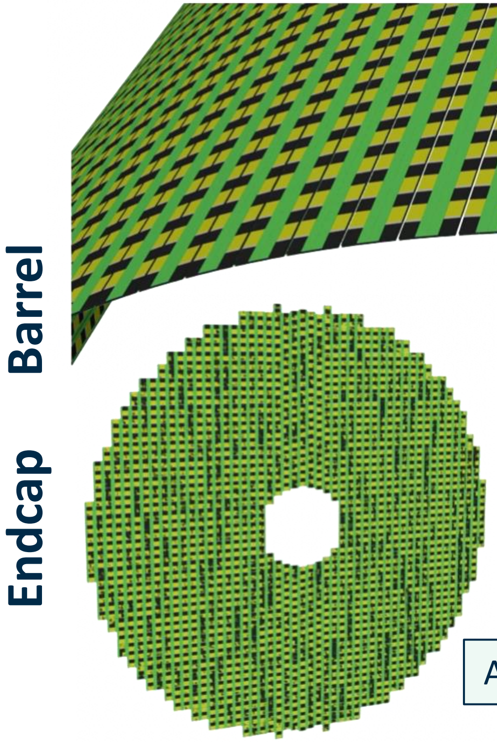




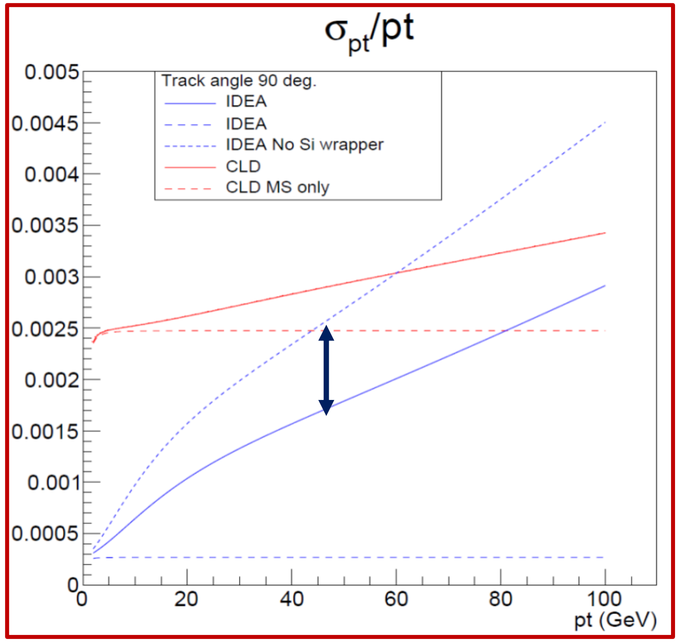
SILICON WRAPPER

The IDEA Concept: Si Wrapper

- **Precision silicon layer around the central tracker**
  - **improve momentum resolution**
  - **extend tracking coverage in the forward/backward region** by providing an additional point to particles with few measurements in the drift chamber
  - precise and stable ruler for acceptance definition
  - *it may provide TOF measurement*

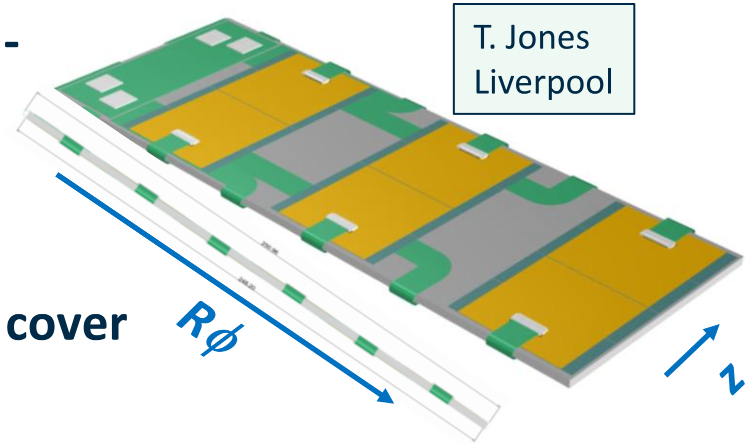


A. Ilg's talk



- Covered area ~100 m^2
  - important impact on services
  - technology suitable for large size production

- **Re-use the ATLASPIX3 quad-module concept**
- No detailed layout of the mechanical structure yet
- **Using multi-module tiles to cover the whole acceptance area**

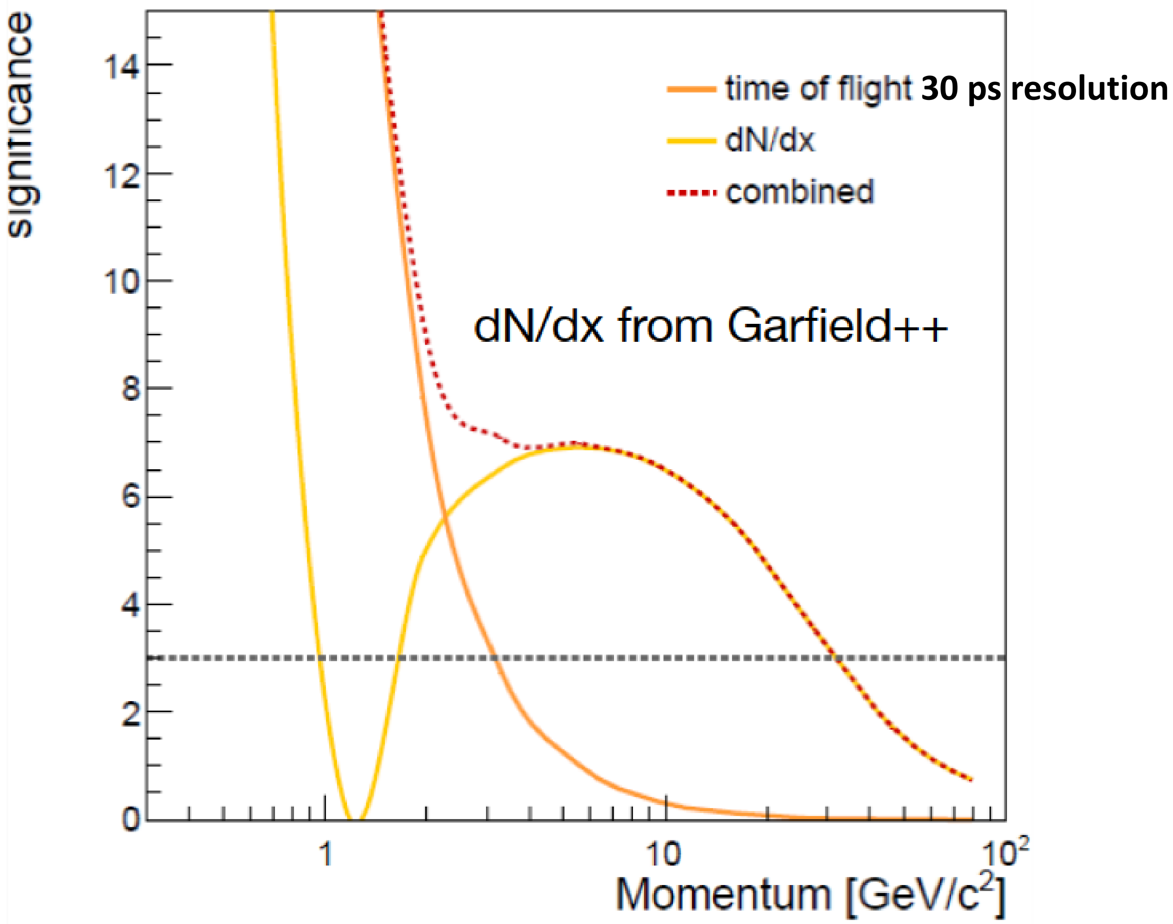


T. Jones Liverpool

TOF measurement in Si Wrapper

- Particle Identification is essential for many physics measurements
- Needed on a wide momentum range
  - $B_s^0 \rightarrow D_s K$ has K up to 30 GeV/c
  - K for flavour tagging in $b \rightarrow c \rightarrow s$ decay chains are pretty soft
  - useful in tau physics for Vus measurements in $\tau \rightarrow K\nu$

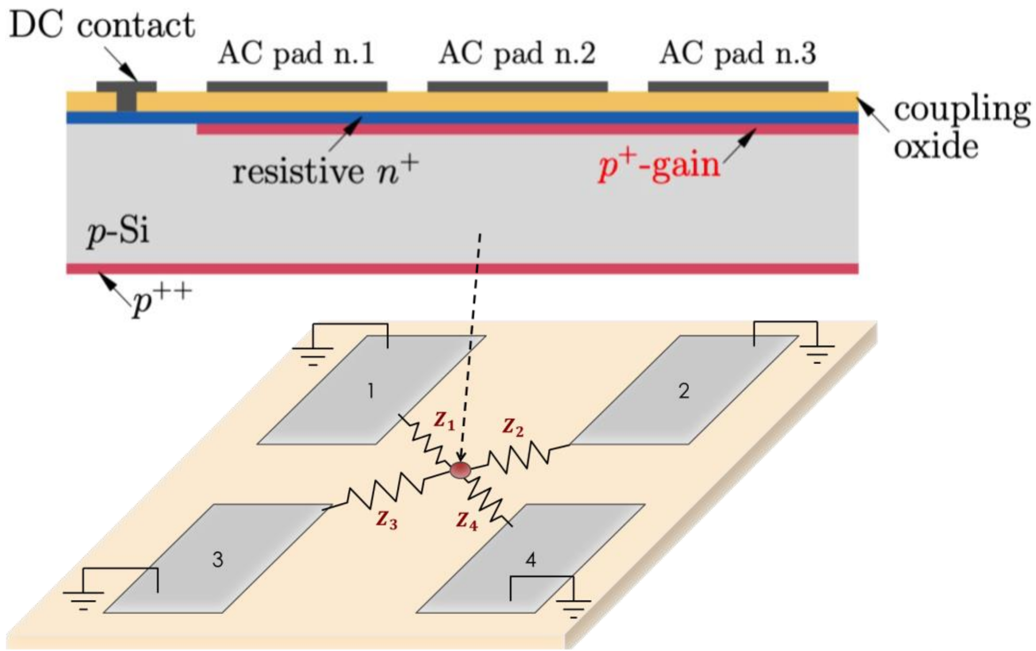
- **dN/dx** measurements in Drift Chamber provides 3σ separation up to 30 GeV/c
- Confusion region about 1 GeV/c can be covered by **TOF** measurement with resolution **<100 ps**

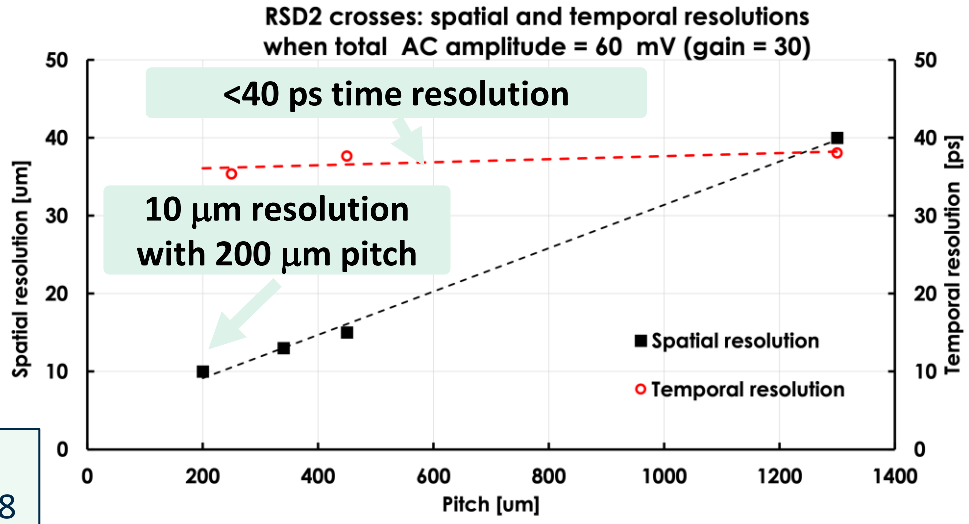


Can it be implemented in the Si Wrapper without compromising the spatial resolution?

Si-Wrapper: alternative RSD option

- LGAD detector with **continuous gain layer**
- Charge collection through **resistive n-layer**
- Readout by induction on **AC coupled pads**
- Fully active detector
  - avoids inefficient regions due to the insulation between pixels needed in LGAD sensors
- Charge sharing defined by the relative impedance of the path between the charge deposition and readout electrodes
  - Sharing is deterministic (in low pitch pixel detectors sharing is dominated by Landau fluctutations)
  - Timing resolution approximatively independent from pixel pitch
  - Position resolution ~5% of the readout pitch: more space in readout pixel cell to implement precision TDC





N. Cartiglia et al. arXiv:2301.02968

Summary and outlook

- The IDEA tracker layout poses different challenges for the different silicon trackers:
  - Extremely high resolution and low-mass are needed for the vertex detectors
  - System issues are the focus topics for the large area detectors
  - Depleted Monolithic CMOS pixel detectors are a cost-effective and high-performance solution
- **ARCADIA** (LF 110 nm) provides a global platform for fully-depleted CMOS sensors
  - The sensitive area has been developed and detector performance appears very promising
  - Fine granularity and low power make it suitable for the vertex trackers
  - Periphery needs to implement features for system integration: command decoder, 1.28 Gbps serializers...
- **ATLASPIX3** (AMS/TSI 180 nm) is a well-developed full-size sensor:
  - Already a possible solution for the bulk of the detector silicon area
  - It is used to investigate integration and system issues
- **Resistive Silicon Detectors** are an extremely interesting option for the Silicon Wrapper:
  - Micrometric spatial resolution even with coarse granularity: reduced number of channels
  - Provide a TOF layer supplementing the drift chamber particle ID
- Plenty of **fascinating electronic design and sensor development** will be needed to arrive to build a state-of-art detector within the time scale of future e^+e^- factories
- At the same time, it is possible to **address system aspects with already existing detectors**

BACKUP

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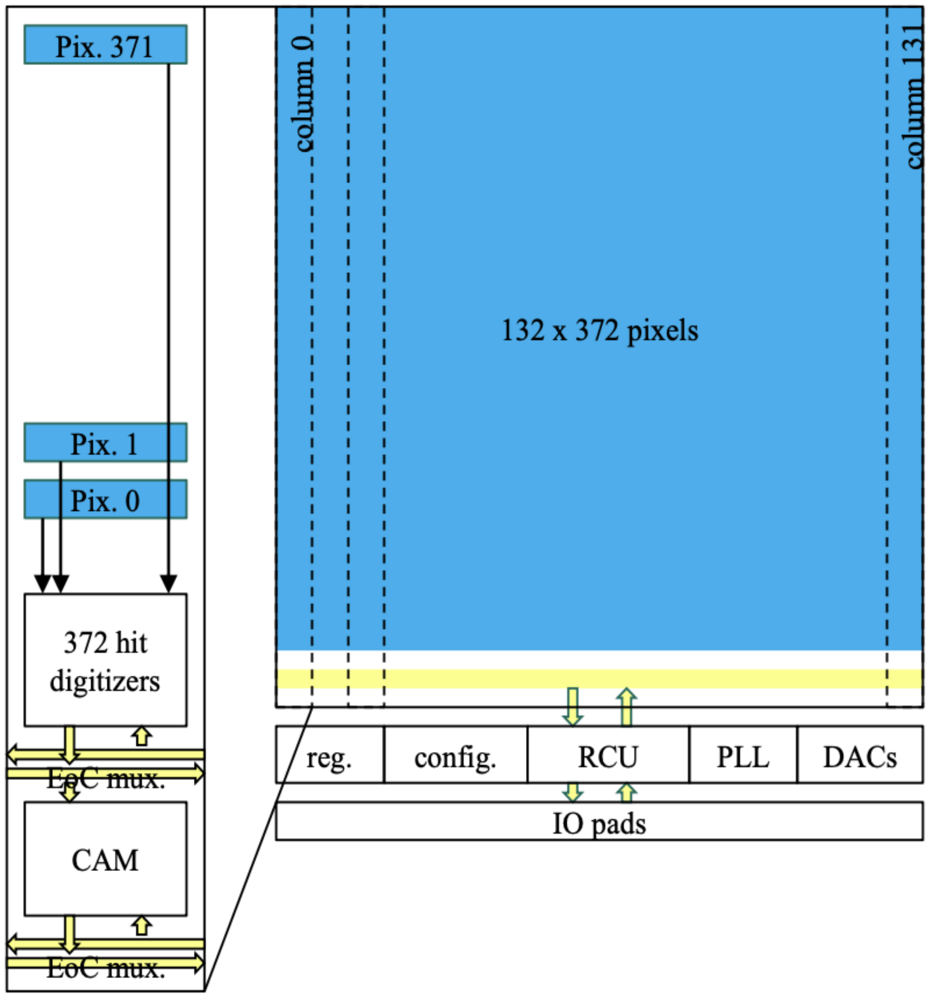
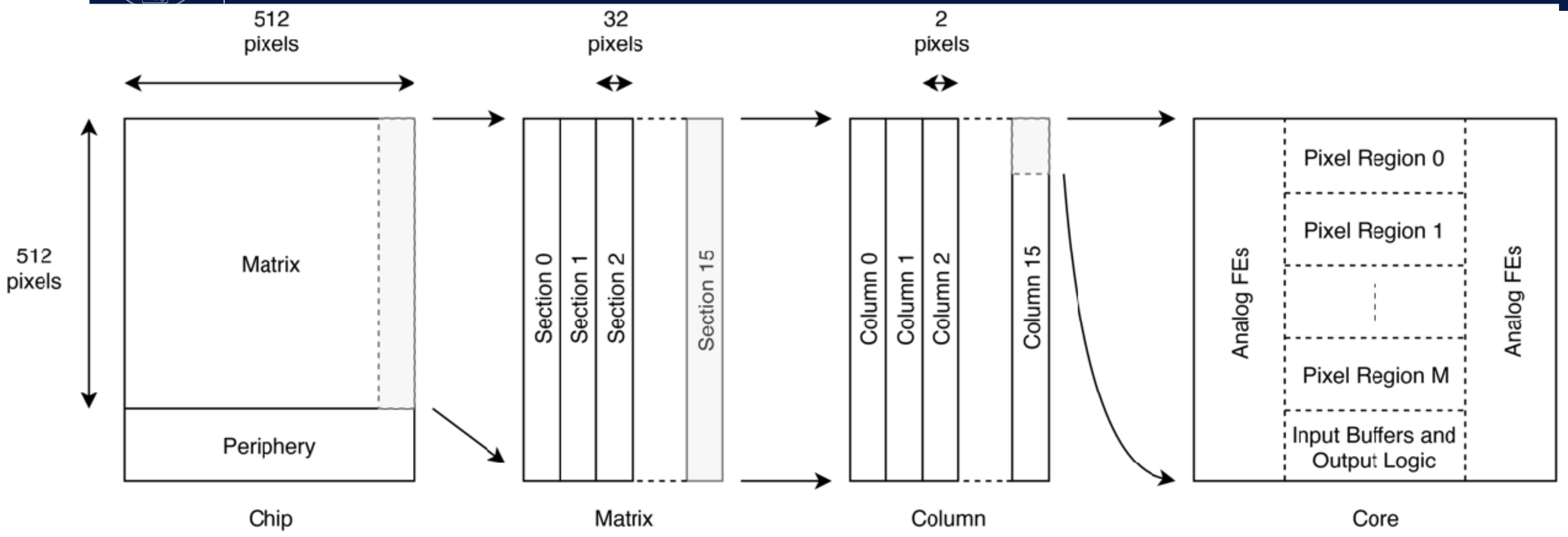
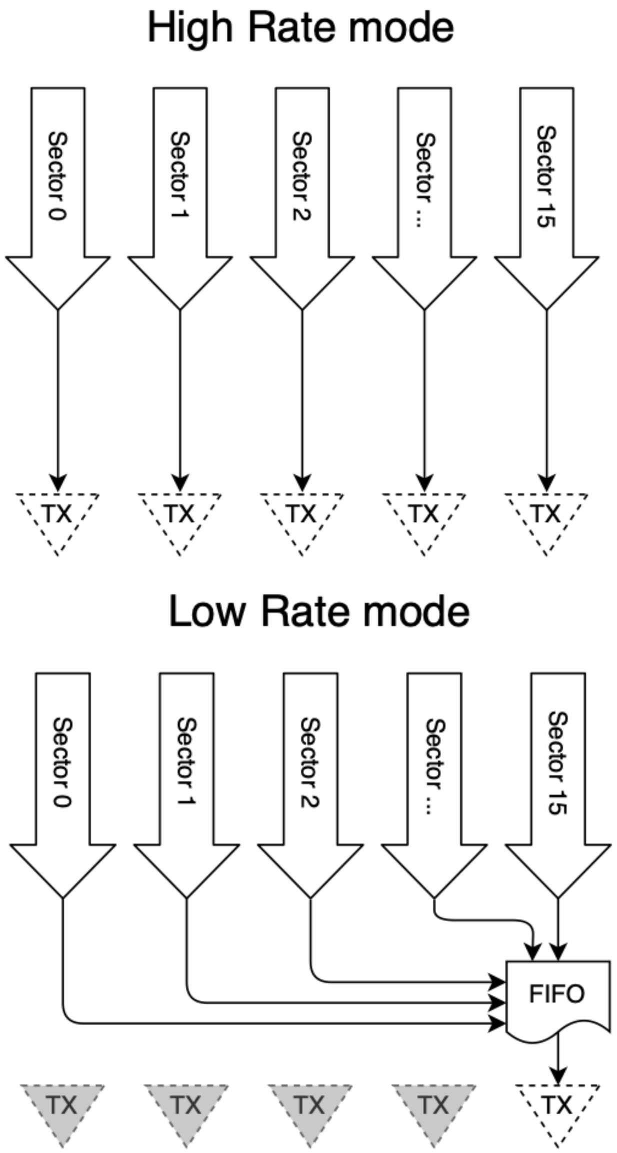
ATLASPIX3 Readout Architecture

- **Chip architecture**
  - organized in 132 columns, each with:
    - 372 pixels
    - **372 hit digitizers** (HDs)
    - **80 content addressable memory cells** (CAM)
    - **two end-of-column multiplexers** (EoC mux)
  - **digital part** (HDs, CAM, EoCs) in **chip periphery**, separated from analog pixels electronic (CSA and comparator)
  - chip periphery also contains the readout control unit (RCU), the clock generator, configuration registers, DACs, linear regulators and IO pads
  - **triggerless** and **triggered** readout
    - two EoCs
    - 372 hit buffers for triggerless RO
    - 80 trigger buffers for triggered RO



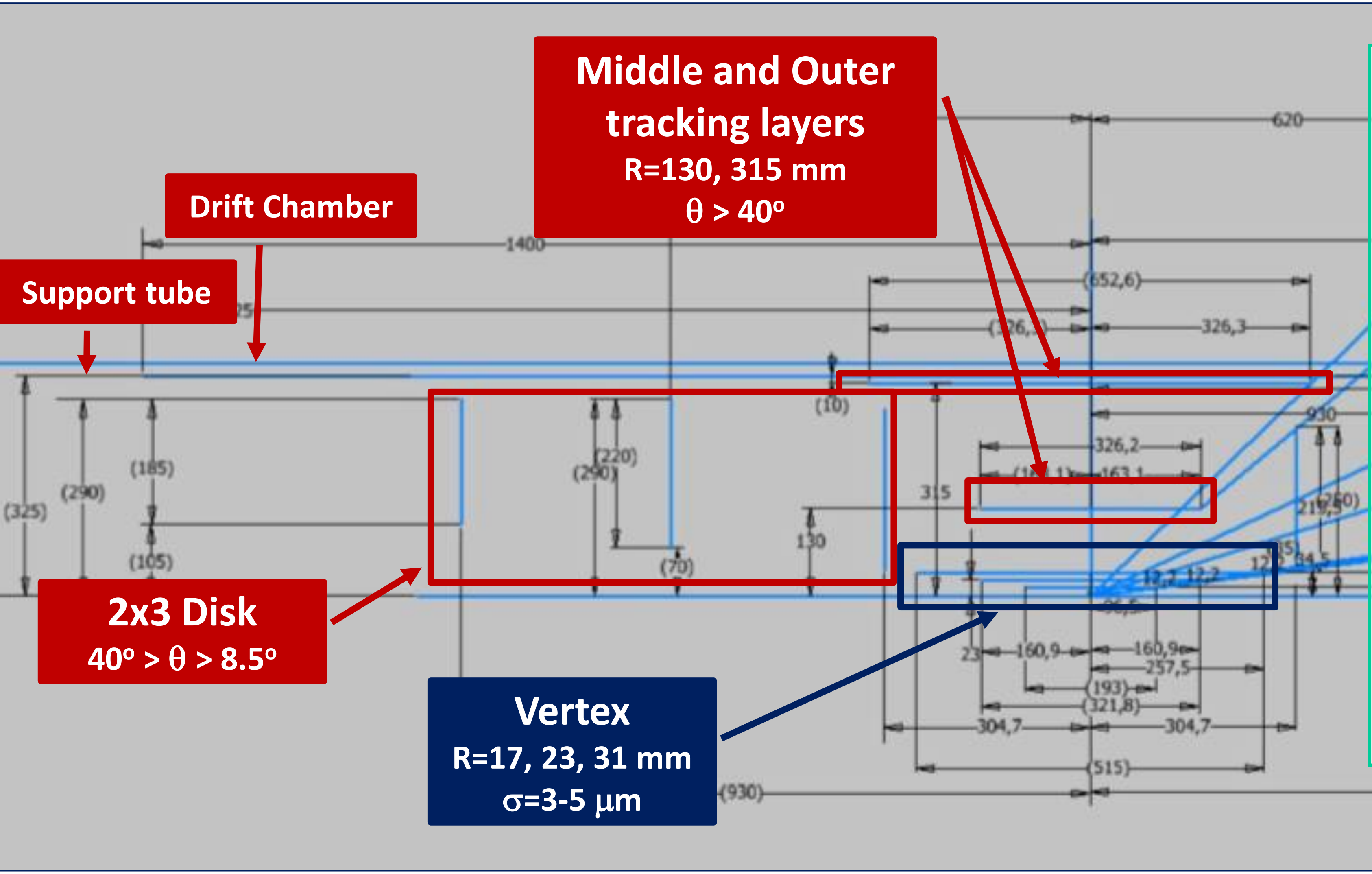
ARCADIA: MD3 Architecture





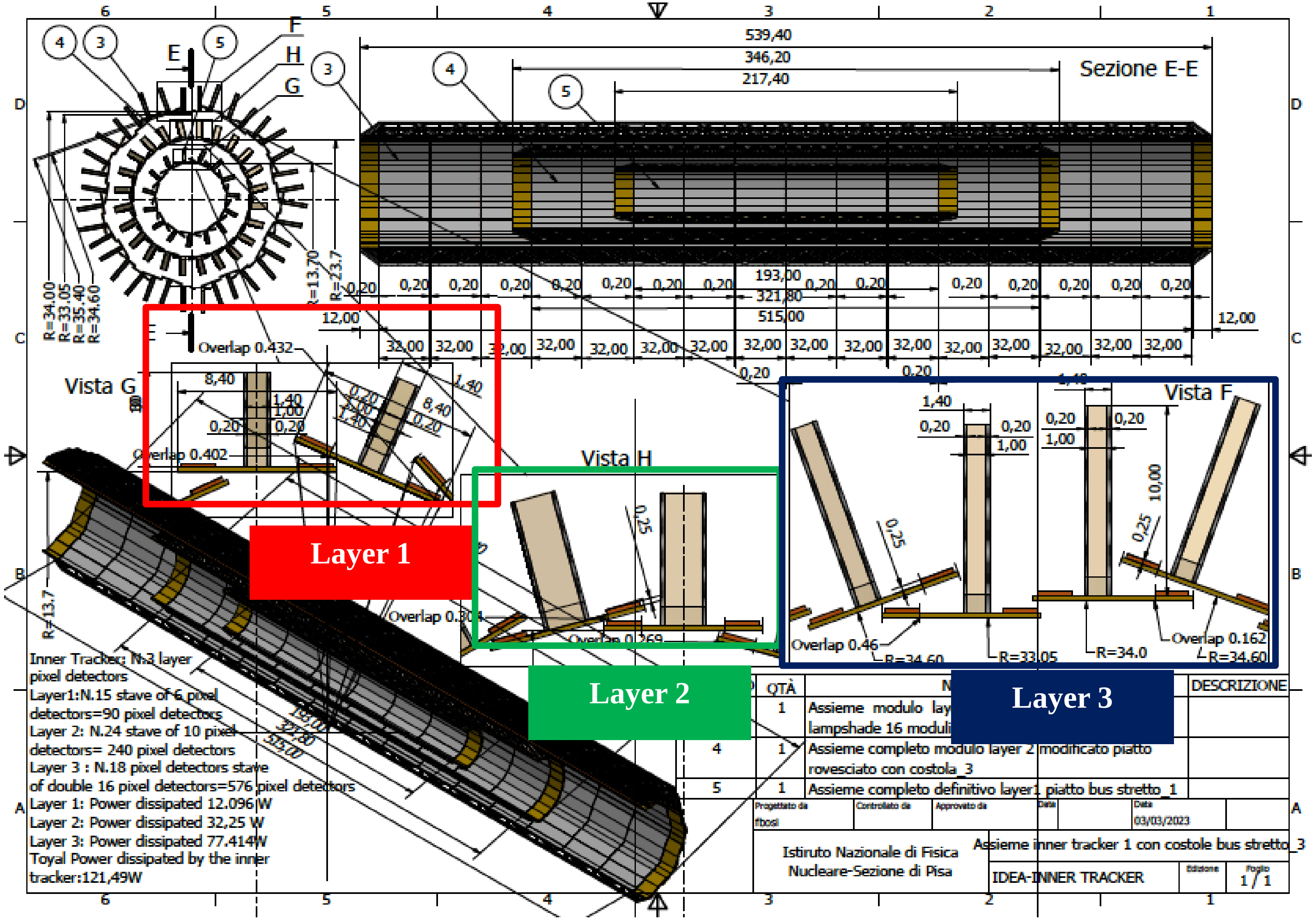
- Pixel size 25 µm x 25 µm, Matrix core 512 x 512, 1.28 x 1.28 cm silicon active area, “side-abuttable”
- Triggerless data-driven readout and low-power asynchronous architecture with clockless pixel matrix
- Event rate up to 100 MHz/cm^2 (post-layout simulations, to be demonstrated: test-beam in late 2023)
- Each sector has an independent readout and output link when operating in High Rate Mode
- Sector data is sent out (8b10b encoded) via dedicated 320MHz DDR Serialisers
- In Low Rate Mode, the first serialiser processes data from all the sections. The other serialisers and C-LVDS TXs(*) are powered off in order to reduce power consumption.

The IDEA Concept: Vertex Detector



- **Vertex detector:**
  - target high granularity
  - low power consumption (air cooling)
  - may compromise between time-resolution vs. power
- **Silicon internal tracker**
  - precision points connecting vertex with drift chambers
  - low p_t tracking
  - bunch crossing identification

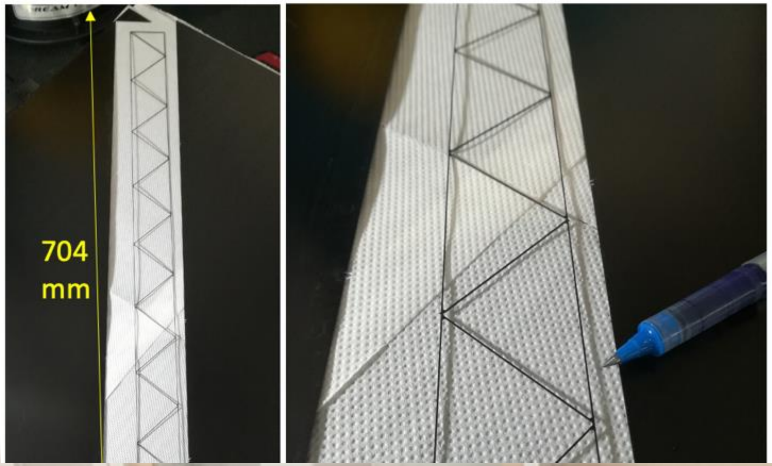
Inner vertex layout

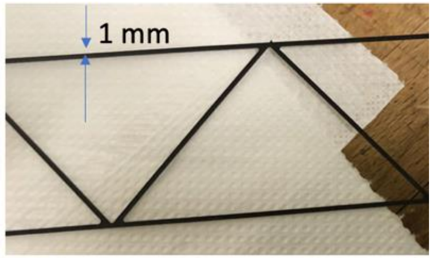


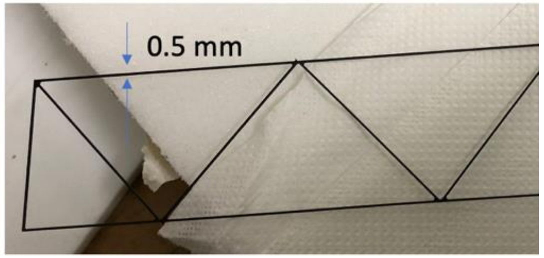
Outer Vertex Stave prototyping

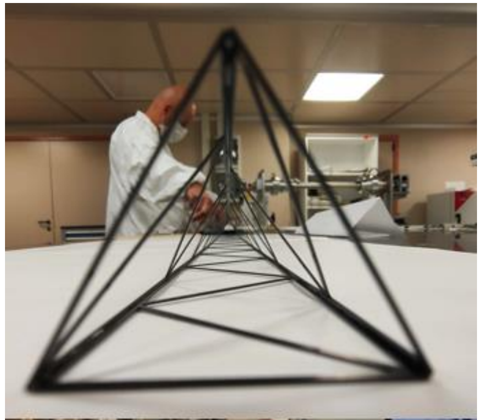
Prototypes built for Belle II upgrade in Pisa

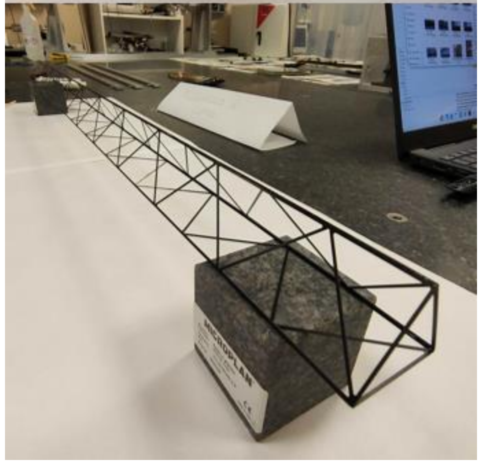
CF water-jet cut (by WatAJet Company)





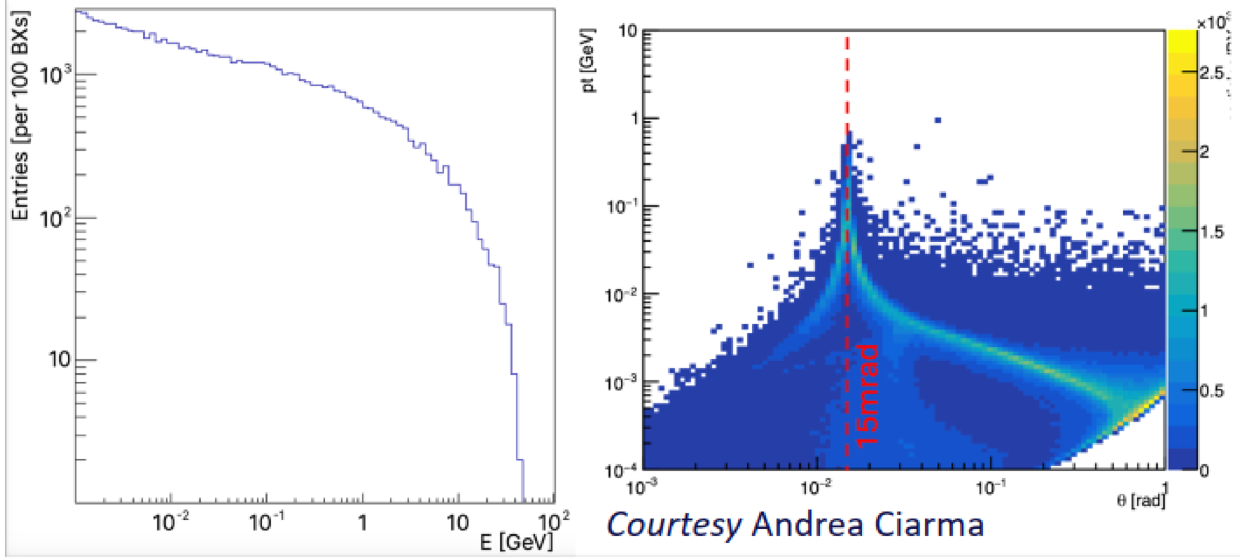






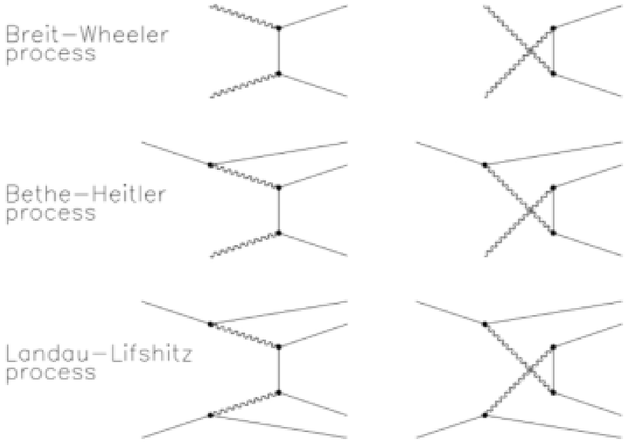
Incoherent Pairs Creation (IPC)

Z pole, V23 optics, GuineaPig++



Courtesy Andrea Ciarma

Secondary e+e- pairs produced during bunch crossing via the interaction of beamstrahlung photons with real or virtual photons.



see talk by A. Ilg

- Cluster size of 5, safety factor of 3, 25 μm pitch pixels
- Cut at 1.8 keV of deposited energy (500 e-)

M. Boscolo @ MAPS detector for FCCee Workshop

First occupancy and hit rates calculations in the vertex detector

	FCC-ee	ALICE ITS3
Occupancy	$\sim 20\times10^{-6}$	$\sim 30\times10^{-6}$
Hit rate	170 MHz/cm^2	250 MHz/cm^2