Trigger Primitive Generation using FELIX FPGA system: A case study for DUNE

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Introduction

The Prototype Deep Underground Neutrino Experiment (ProtoDUNE)[1] Data Acquisition (DAQ) system required the ability to generate Trigger Primitives (TPs) from the ADC waveforms that represented particle detection signals from the Anode Plane Array (APA) wires. A Field Programmable Gate Array (FPGA) PCIe card was used for ADC data ingest to a readout server and it was demonstrated that TP generation could be performed in the same FPGA device.

Firmware Design

The Firmware (FW) Trigger Primitive Generation (TPG) design consisted of multiple modular FW blocks to handle various aspects of data processing to extract TP information from raw ADC data. This included the reorganising and routing of a monolithic Warm Interface Board (WIB) packet into four separate streams of ADC samples for processing along with appending each stream with header information such as channel ID, detector IDs and timestamps. From there the stream processors perform a pedestal subtraction on the data using a known pedestal value for each channel in the system, pass the data through a Finite Impulse Response (FIR) filter and finally perform hitfinding on the current ADC values to check they have not exceeded a programmable threshold limit. If the limit is exceeded, a TP packet is produced.

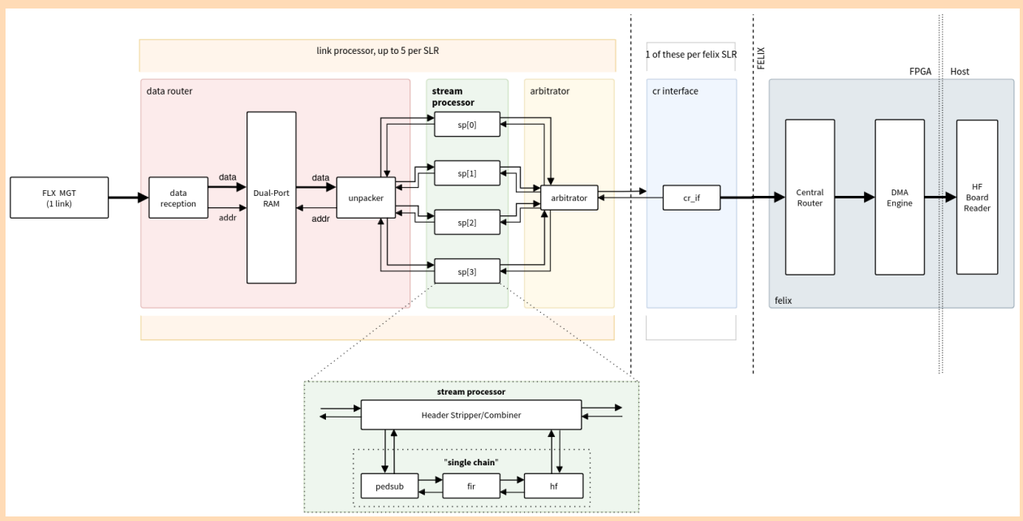


Diagram illustrates the top level functionality of the FW TPG system. The system itself was scalable via the use of generic statements in the code, such that the number of stream processors or link processors could be scaled up if FPGA logic resources are available to do so.

Hardware Implementation

The FPGA card selected for the ProtoDUNE readout solution was a variant of the Front End LInk eXchange (FELIX)[2] system, namely the FLX-712. This card features an AMD® Kintex Ultrascale (XKCU115) FPGA. Along with the physical circuit board design, the FLX-712 is provided with a build scripting infrastructure and various firmware blocks. These build scripts were modified to allow the ProtoDUNE FW TPG design to be embedded inside a functioning FLX-712 FW design.

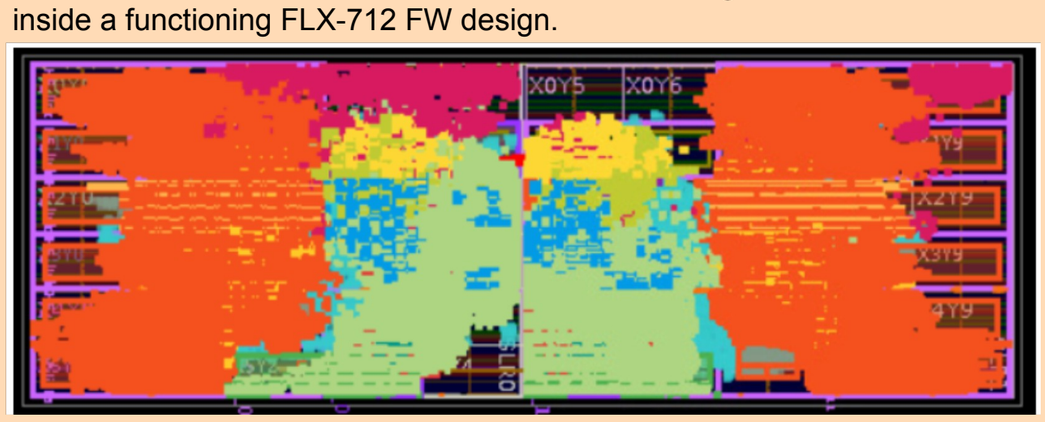


Diagram shows the device view of the FELIX FPGA with the firmware implementation completed. The logic blocks have been coloured to better highlight and separate logic functions. Orange blocks are DUNE specific TPG firmware. This specific example processes 12 ADC links.

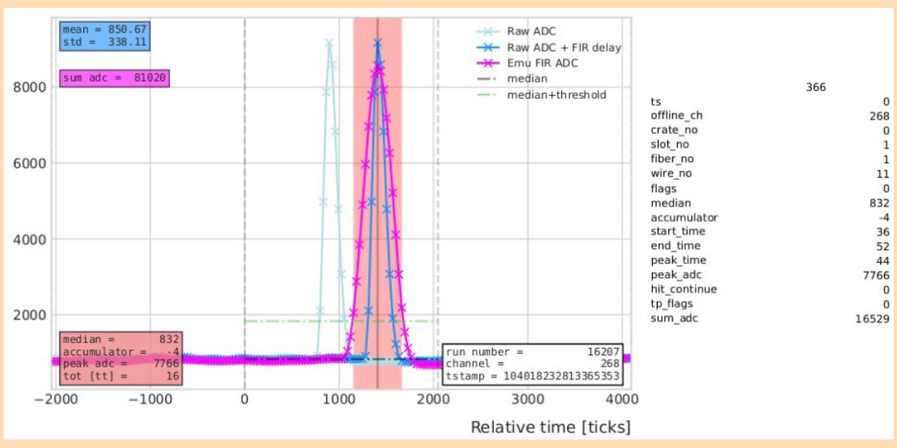
Software Implementation

Software development for the FW TPG required implementation of a control interface to directly communicate to FW modules to configure various options and running states of the system. This was achieved with the IPBus[3] software suite which when used in conjunction with compatible FW modules, allow for control data packets to be sent to the device.

A readout software interface was developed to facilitate the movement of data out of the Direct Memory Access (DMA) buffers of the FELIX card and onto the host system for further processing. This involves unpacking TP frames from larger superchunk packets which collate multiple TP frames together for more efficient memory transfer operations. After this, TPs frames where the hit crosses their representative time boundaries are stitched together. There is then another software layer to allow the TP data to be interfaced to the rest of the DUNE-DAQ system.

Validation Tools

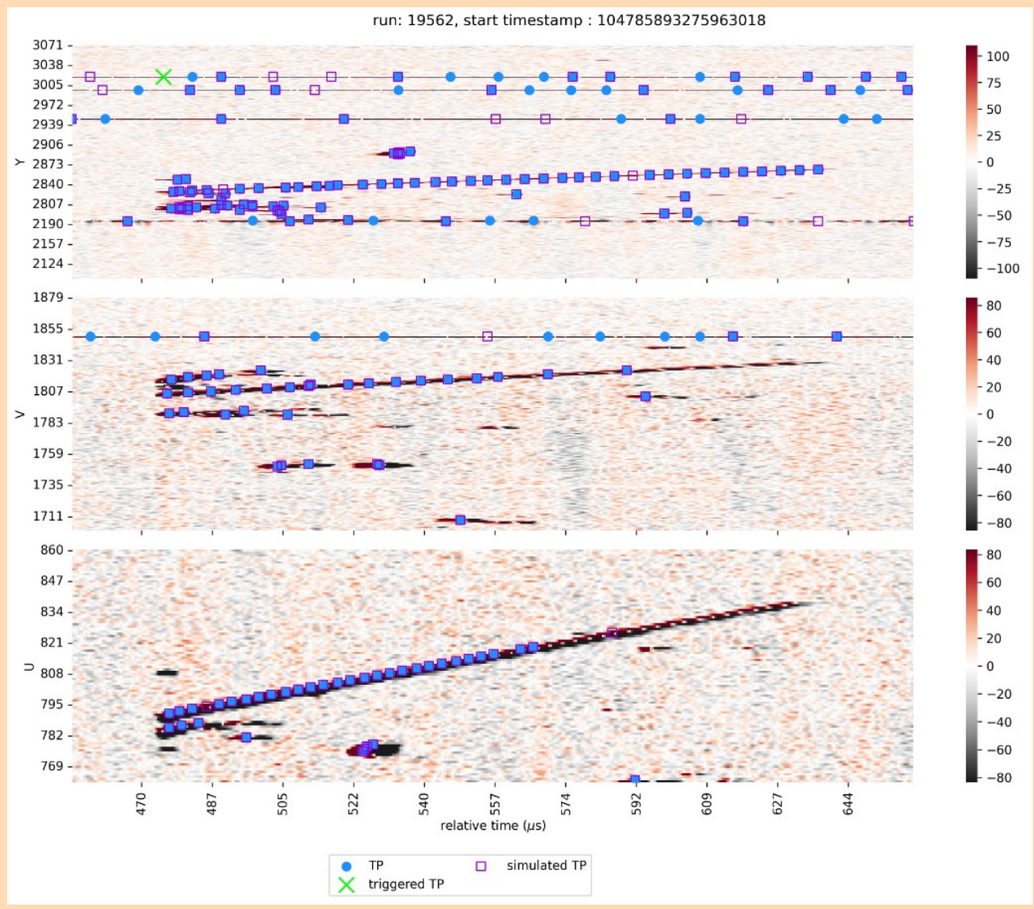
A suite of simulation, plotting and analysis tools where also developed to allow for testing, performance benchmarking and validation of the FW TPG.



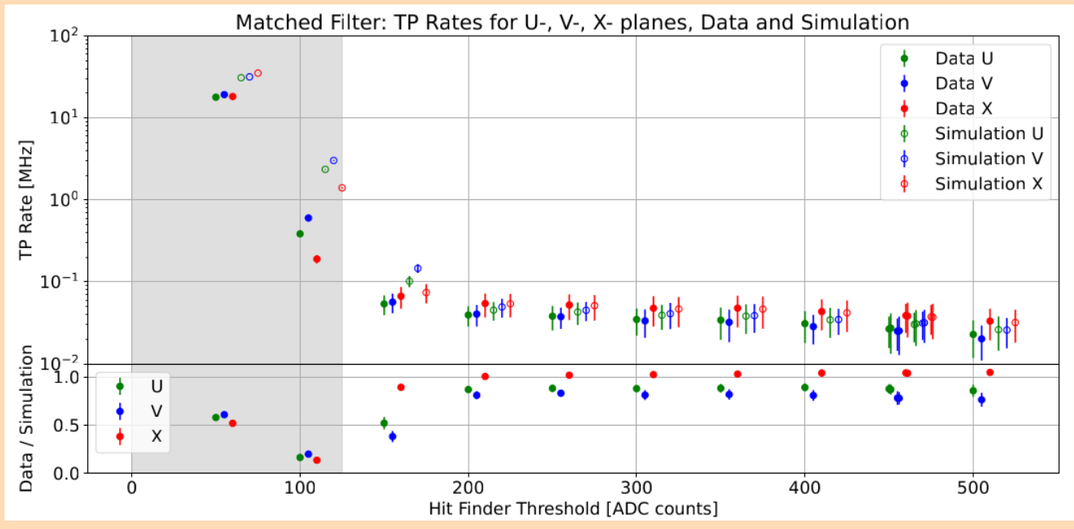
Plot shows a hit event from ADC data with overlaid information from the FW TP produced highlighted by the red band and a software emulation of the ADC data in magenta showing good agreement.

Performance Evaluation

The FW TPG system was deployed during ProtoDUNE-I operation and various test stands in the lead up to ProtoDUNE-II operations. The largest variant of the design performed TPG on 12 links of data from the Vertical Drift, (VD), variant of the coldbox test platform. This involves analysing 3072 channels across the Charge Readout Plane, (CRP).



The plot is an event display of 3 ADC links of recorded VD data. This data was recorded with the use of a cosmic ray trigger algorithm, with the trigger being supplied TPs from the FW TPG.



Plot is a comparison of TP rates between data and simulation, with data being FW TPG binary captures and simulation being playback of the same period of captured ADC data.

Summary

The FW TPG successfully demonstrated operation during ProtoDUNE-I and was further developed to support various coldbox operations with a view to targeting and supporting ProtoDUNE-II operations. The FW TPG was discontinued in favour of a software based TPG solution for ProtoDUNE-II and the full scale DUNE detector, however the work demonstrated as part of the FW TPG development proved it a viable option for TPG in large scale detectors such as ProtoDUNE.

References
[1] ProtoDUNE: FERMILAB-PUB-20-024-ND
[2] FELIX: arXiv:1806.09194
[3] IPBus: http://dx.doi.org/10.1088/1748-0221/10/02/C02019