

Quantum machine learning classifiers implemented on FPGA for ultra-low latency applications.

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Tree Tensor Networks (TTNs) are hierarchical tensor structures commonly used for representing many-body quantum systems, but can also be applied to ML tasks such as classification or optimization. We study the implementation of TTNs in high-frequency real-time applications such as the online trigger systems of HEP experiments. The algorithmic nature of TTNs makes them easily deployable on FPGAs, which are naturally suitable for concurrent tasks like matrix multiplications. Moreover, the limited hardware resources can be optimally exploited by measuring quantum correlation and entanglement entropy, that can be used for the optimal pruning of the TTN models. We show different TTN classifiers implementations on FPGA, performing inference on synthetic ML datasets for benchmarking. A projection of the needed resources for the HW implementation of a classifier for HEP application will also be provided by comparing how different degrees of parallelism affect physical resources and latency.

Alternate track

I read the instructions above

Yes

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