

Nanosecond AI for anomaly detection with decision trees on FPGA

Friday, 19 July 2024 20:45 (15 minutes)

We present an interpretable implementation of the autoencoding algorithm, used as an anomaly detector, built with a forest of deep decision trees on FPGA, field programmable gate arrays. Scenarios at the Large Hadron Collider are considered for which the autoencoder is trained using the Standard Model. The design is then deployed for anomaly detection of unknown processes. The inference is made with a latency value of 30 ns at percent-level resource usage using the Xilinx Virtex UltraScale+ VU9P FPGA. The work is documented at <https://arxiv.org/abs/2304.03836><https://nam12.safelinks.protection.outlook.com/?url=https%3A%2F%2Farxiv.org%2Fabs%2F2304.03836&>

Alternate track

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Yes

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