# Development of Cold Electronics for "Giant LAr TPCs"

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for
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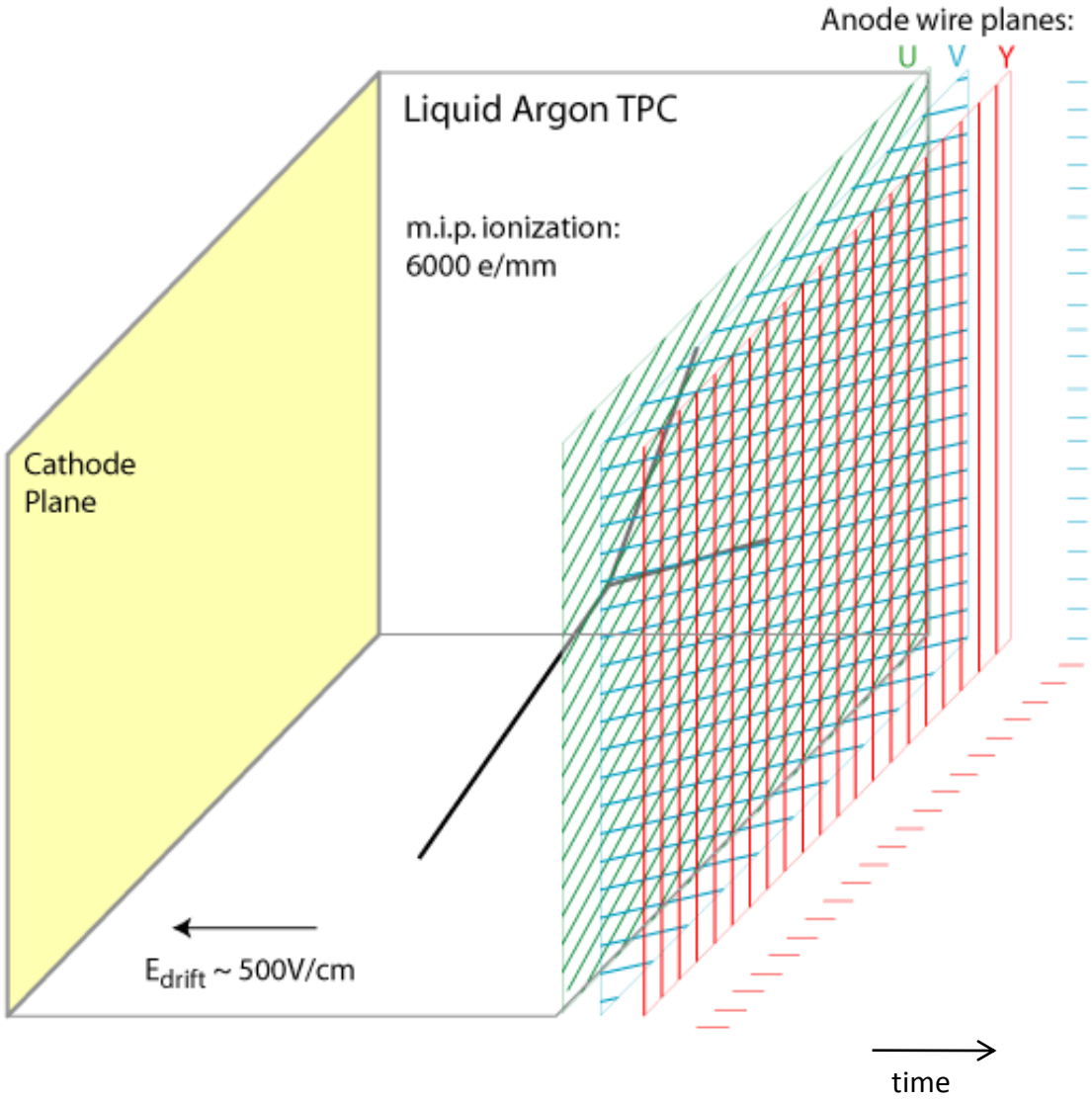
*Acknowledgements: Bo Yu, Alessio D'Andragora (BNL), John Cressler (Georgia Tech; CMOS at low temperatures), Craig Thorn (BNL), Bruce Baller, Grzegorz Deptuch, Ray Yarema (FNAL)*

*GLA2011, Jyvaskyla, June 5-10, 2011*

BROOKHAVEN NATIONAL LABORATORY

Office of Science U.S. DEPARTMENT OF ENERGY

# LAr TPCs



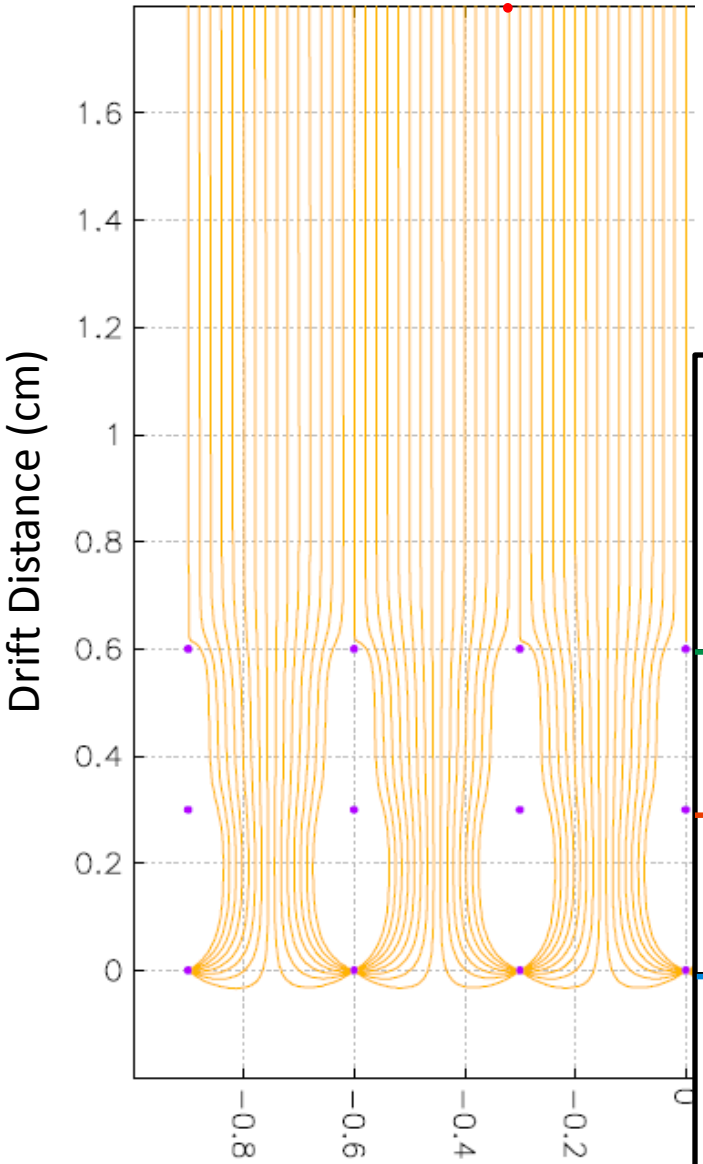

- Sense (anode) wires (up to ~ 10m long):
  - **~31 kwires/kton**, or
  - **~12 kwires/kton**
    - up to **200 pF/wire**
    - collecting (Y)
    - non-collecting (U,V)
- charge sensitivity
  - range ~300 fC
  - ENC < 1,000 $e^-$
- sample/buffer events
  - ADC 12-bit, 2 MS/s
  - **3,000 deep buffer**
- **digital multiplexing**
  - **128:1** to1024:1 two-three stages
  - **power constraint**
  - **~ 10 mW** /wire
- operation in LAr
  - **> 30 years**

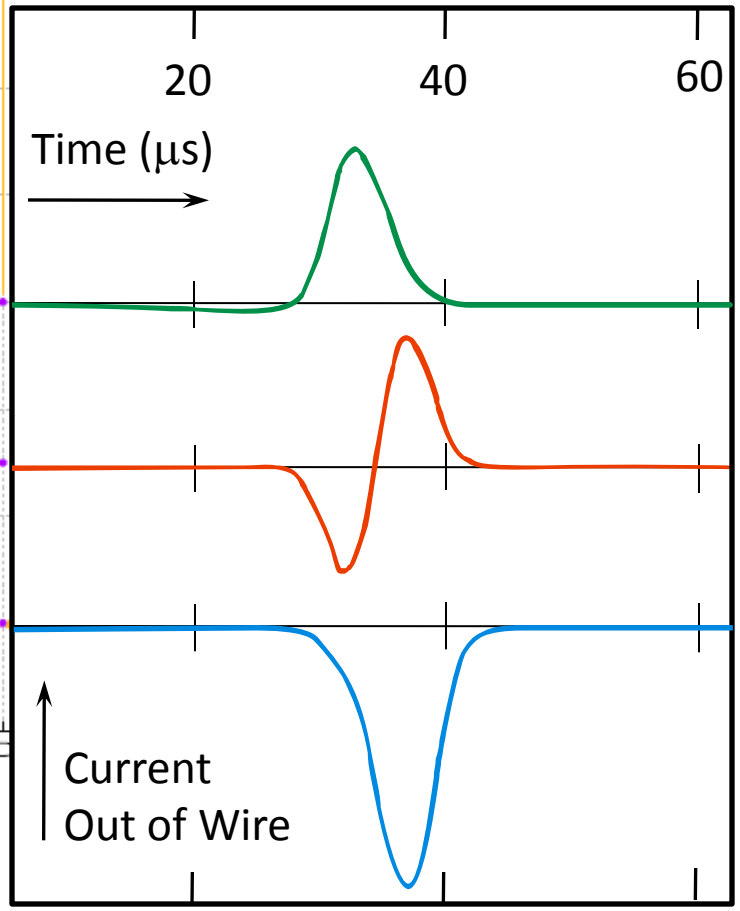
*Outline*:

1. TPC and signal formation
2. Giant TPCs  readout challenge and essential block diagram
3. CMOS properties vs temperature
4. CMOS lifetime and electronics reliability
5. ASIC design
6. ASIC results
7. Summary and future developments

# Charge Signal Formation

Induction by and Collection of electrons on wires (by a track at 0 degrees and perpendicular to the wire planes)




U Induction (small, bipolar)

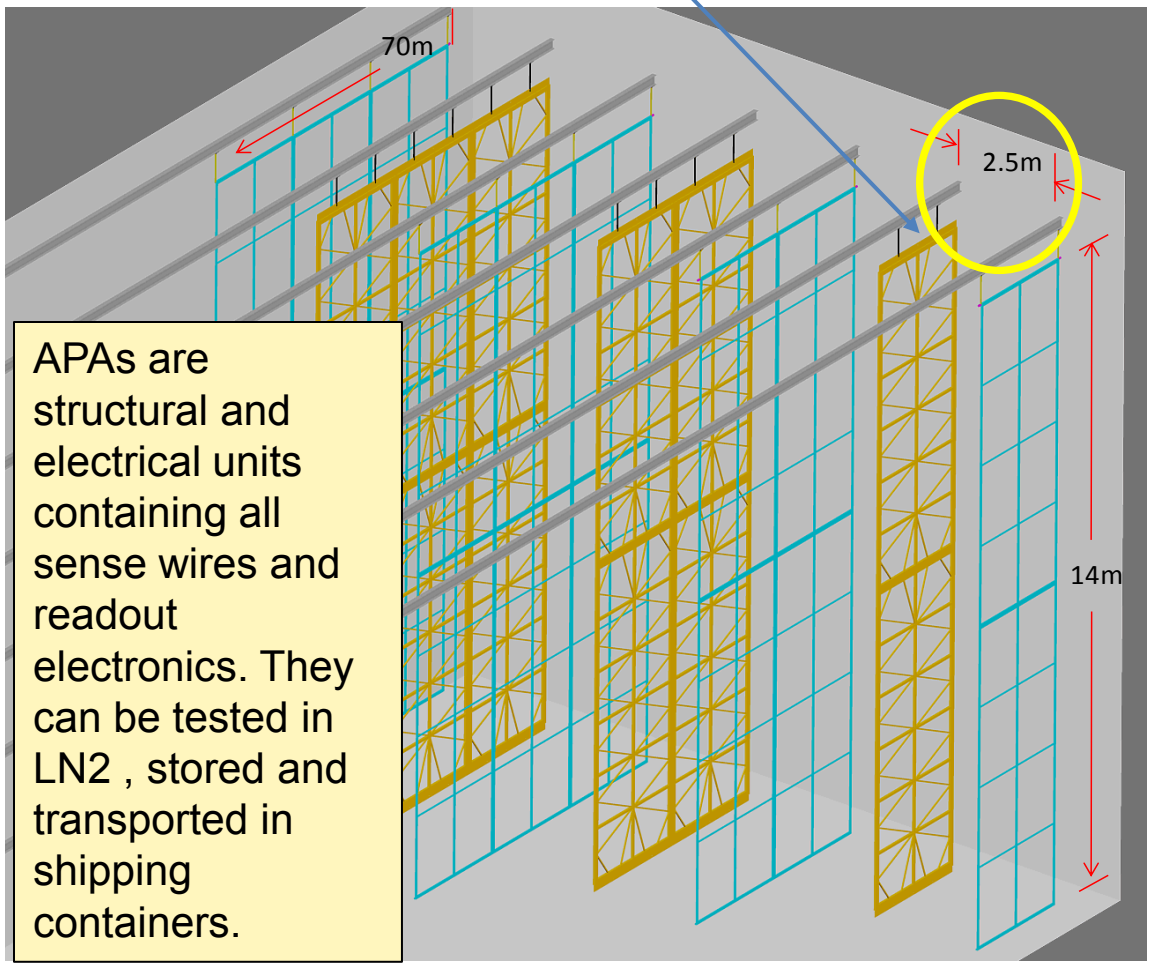
V Induction (small, bipolar)

Y Collection (large, unipolar)

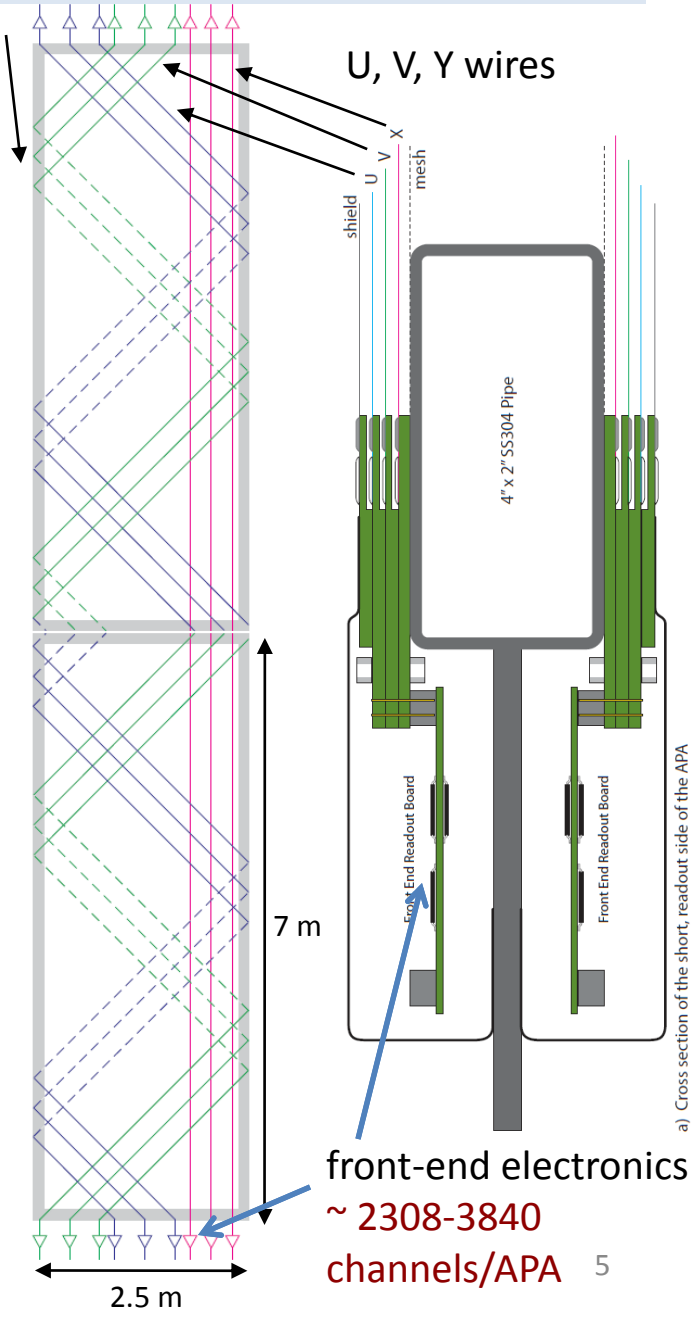
# Anode Plane Assembly (APA) → modular TPC in a large cryostat

~7APAs/kton, 3mm wire pitch, 2.5m drift, 3840 wires)/APA

~5 APAs/kton, 5mm wire pitch, 3.8m drift , 2304 wires/APA




APAs are structural and electrical units containing all sense wires and readout electronics. They can be tested in LN2 , stored and transported in shipping containers.




front-end electronics ~ 2308-3840 channels/APA

# APA + CPA Assemblies form TPC modules in a large cryostat

Field Cage Bars

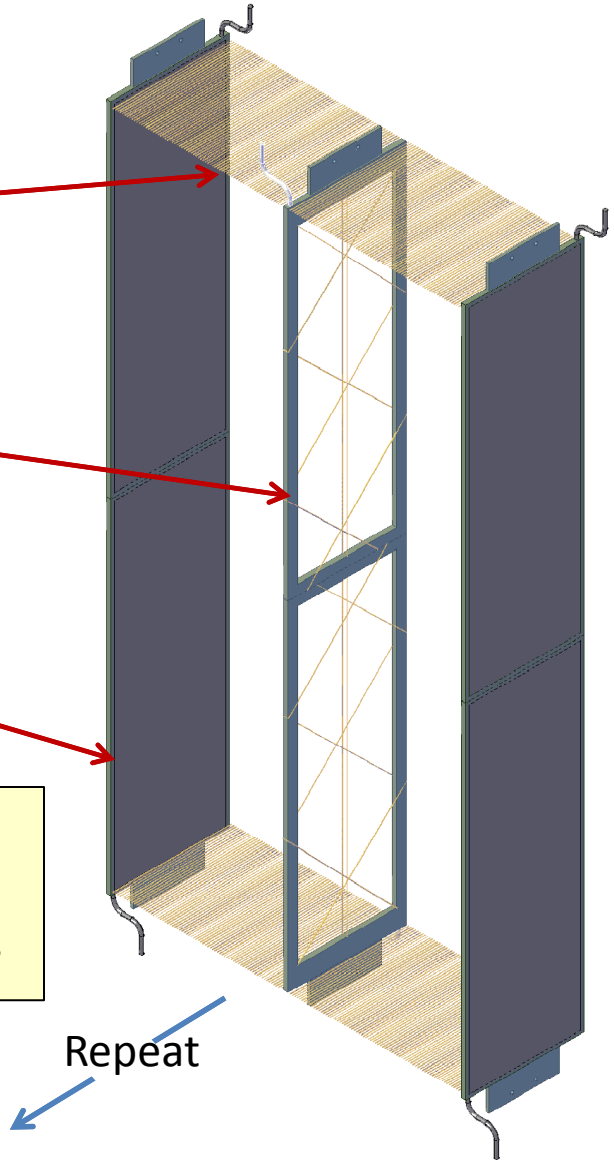
APA = Anode Plane Assembly

CPA = Cathode Plane Assembly

**Active volume/APA**

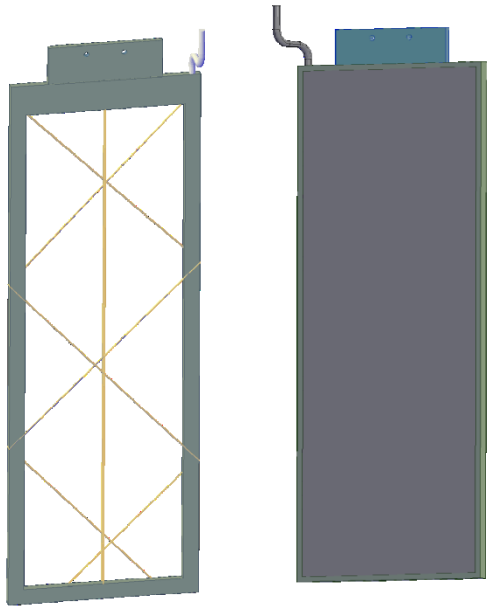
2x2.5mx7mx2.5m=87.5 $m^3$

2x2.5mx7mx3.8m=132.5 $m^3$




**Unit Cell**

TPM = TPC Module = 1 APA + 1 CPA (+1 "terminal" CPA)



APA CPA

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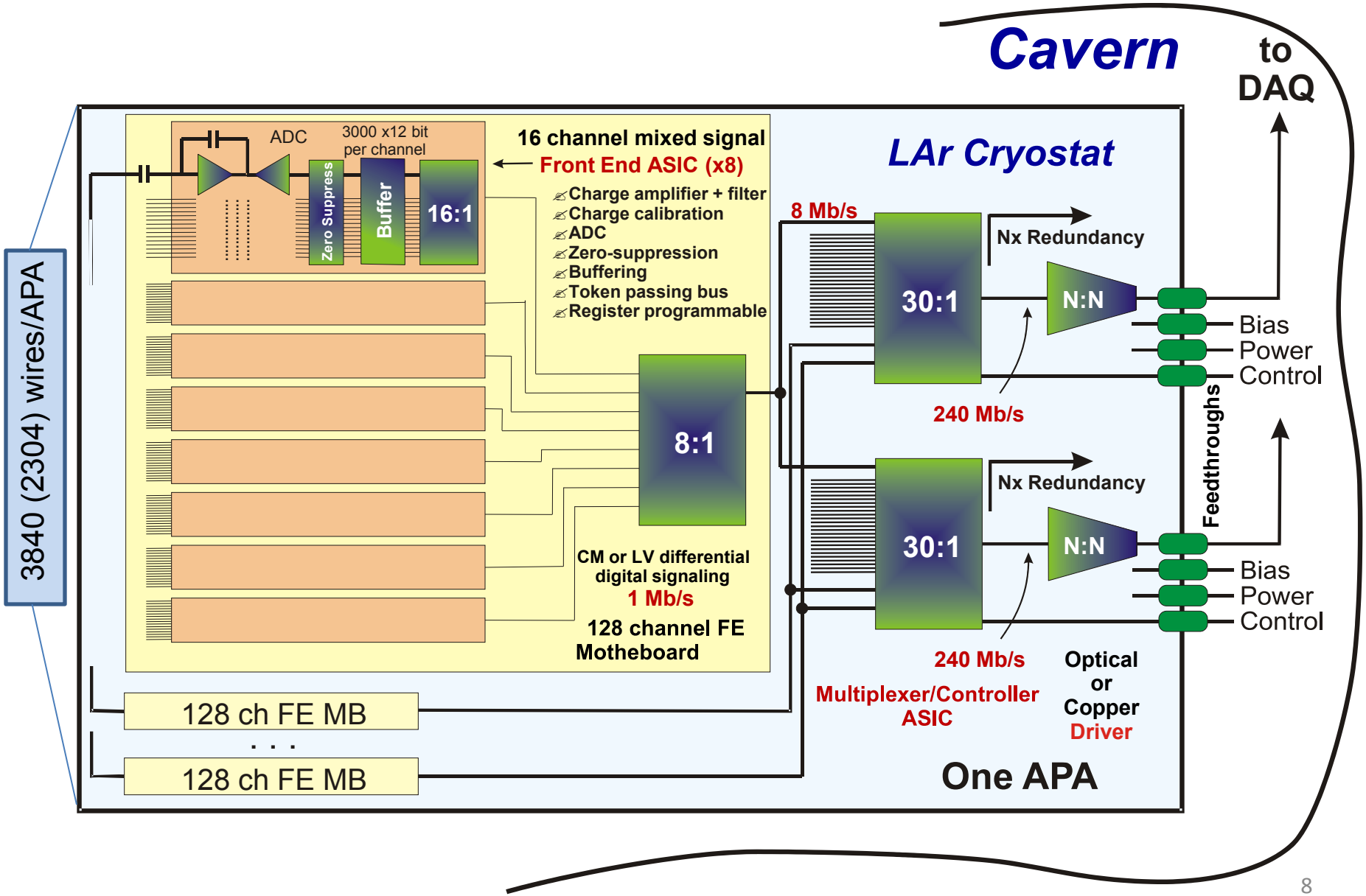
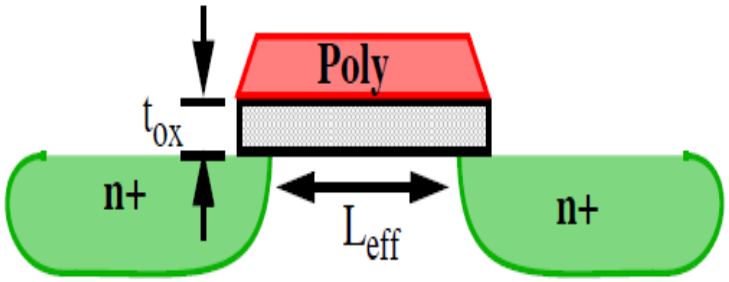
# TPC Readout Electronics Outline



*Outline*:




MOS transistor ~1927

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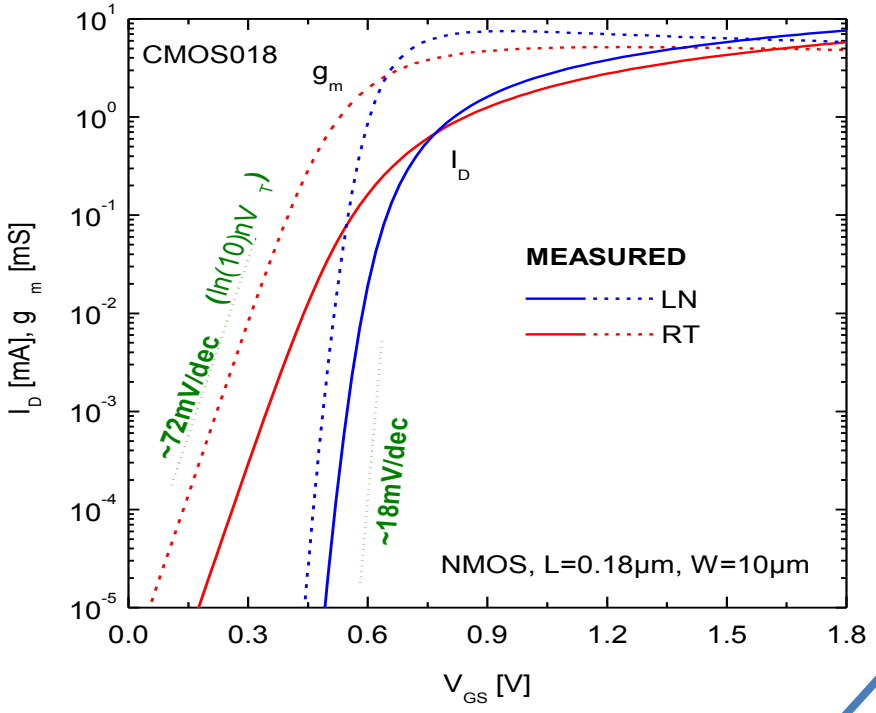
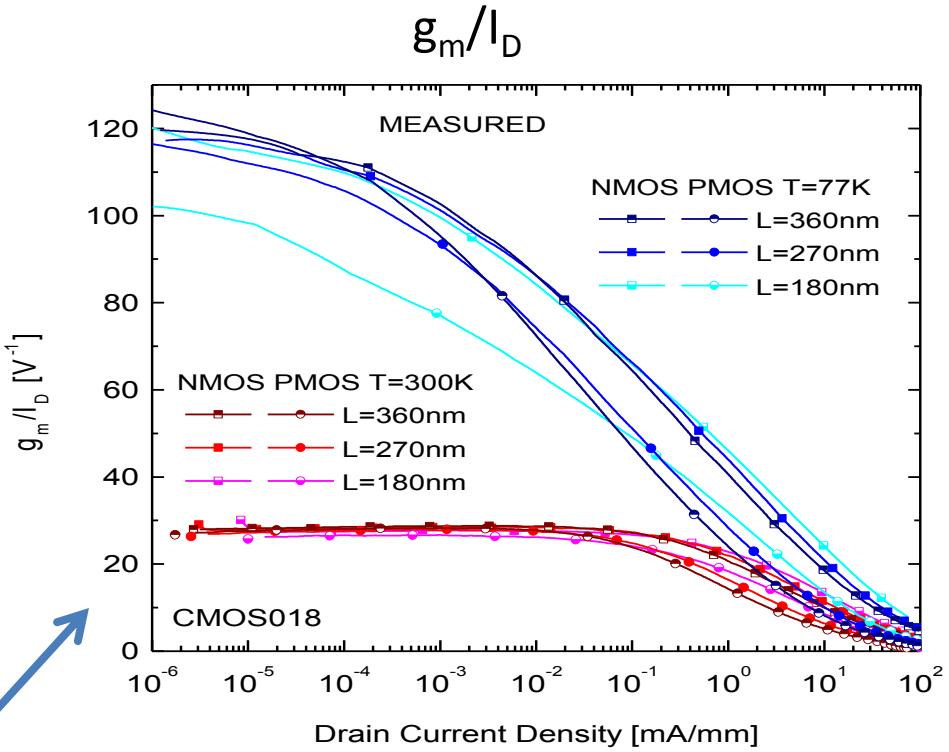
# Did God(s) create CMOS to work in LAr?!




*Transconductance/ /drain current*

$$\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \ \ at \ \ T = 300K \\ \sim 116 \ \ at \ \ T = 77K \end{cases}$$

At 77-89K, charge carrier ***mobility*** in silicon *increases*, ***thermal fluctuations*** *decrease* with ***kT/e***, resulting in a ***higher gain***, ***higher*** $g_m/I$, ***higher speed*** and ***lower noise***.

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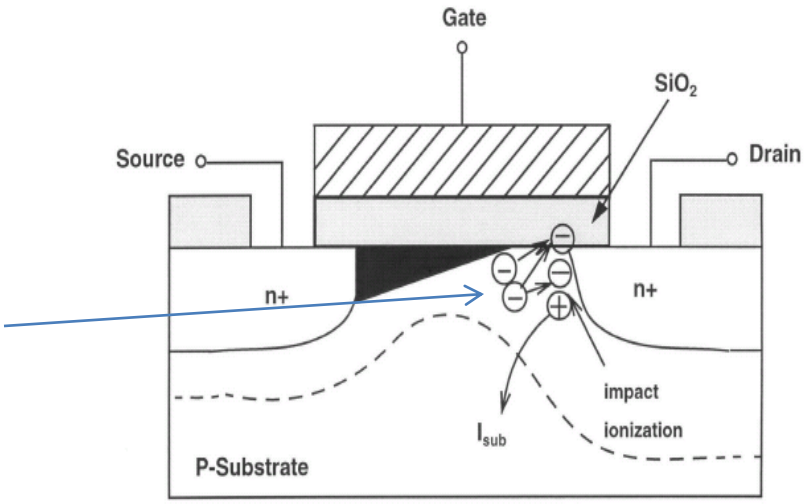
# Impact Ionization and CMOS *Lifetime*

***Chemistry slows down at 89K.***

***What is left?***

•***Impact ionization*** occurs at a lower drain-source voltage at 89K than at 300K. The charge trapped in the gate oxide causes a decrease in transconductance (gain) of the transistor and a threshold shift.

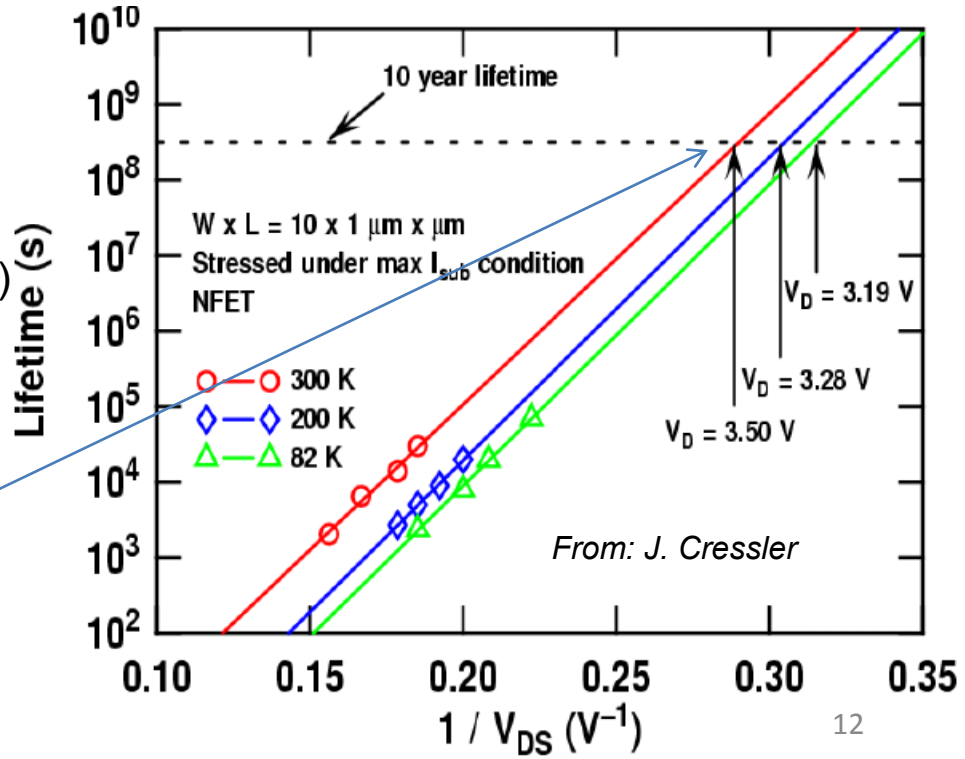



• This limits the effective ***lifetime*** of the device at any temperature (defined in industry as *10% decrease in transconductance* $g_m$).

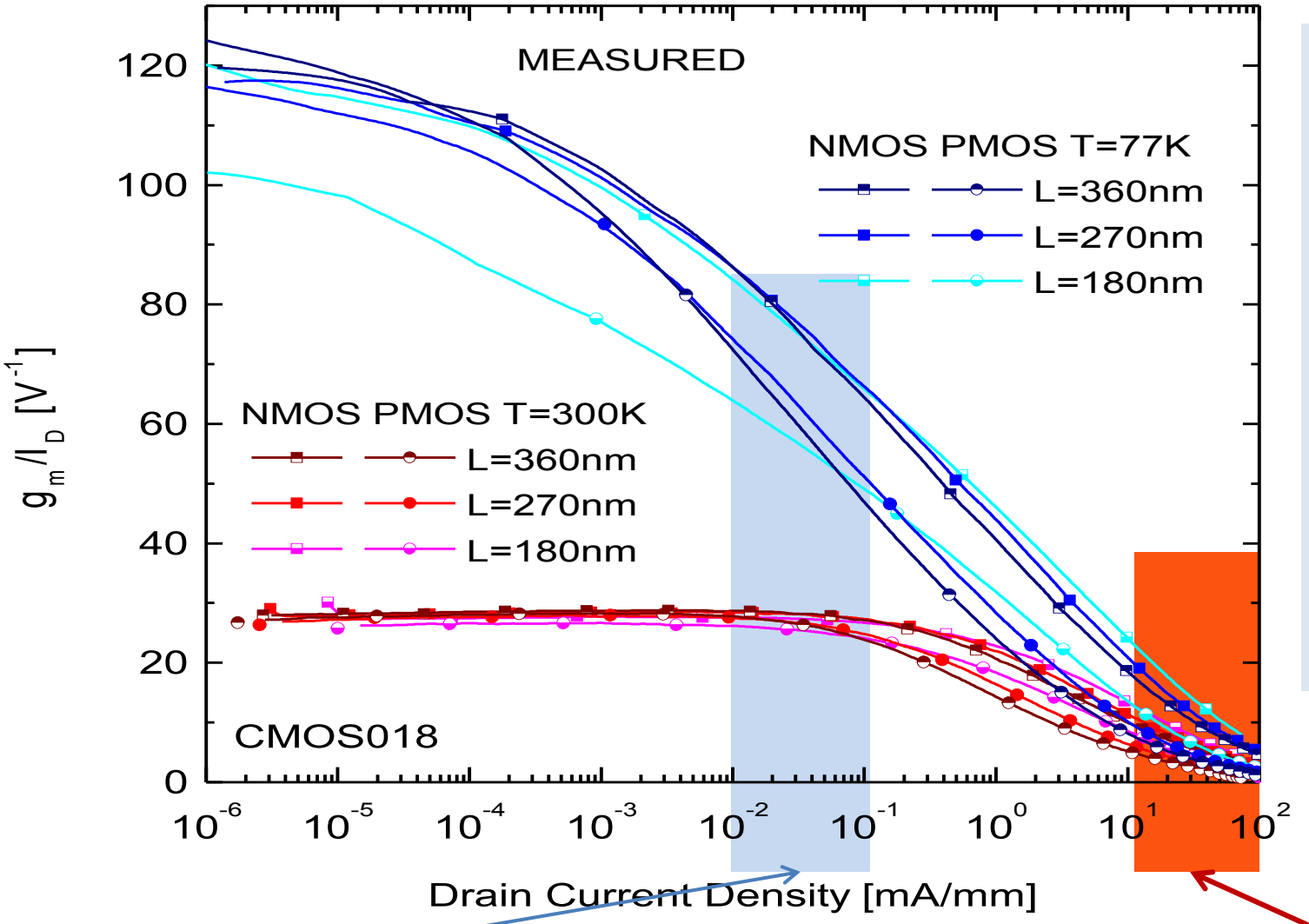
•***Accelerated lifetime testing*** is performed at increased drain-source voltages by measuring the substrate current (*a very sensitive indicator*)

•*Bottom Line: An MOS transistor has* ***equal lifetime*** *due to impact ionization at* ***89K*** *and at* ***300K*** *at different drain-source voltages.*

•***ASICs developed for LAr TPCs conform to design guidelines for a lifetime > 30 years.***



# Designing CMOS for low power = long lifetime




- *Lifetime* ≈ 1/(current density)
- Additional conservative guidelines: **$V_{DD}$-10%, L>1.5 $L_{min}$**
- *Digital*: **+** clock frequency **<<** ring oscillator frequency

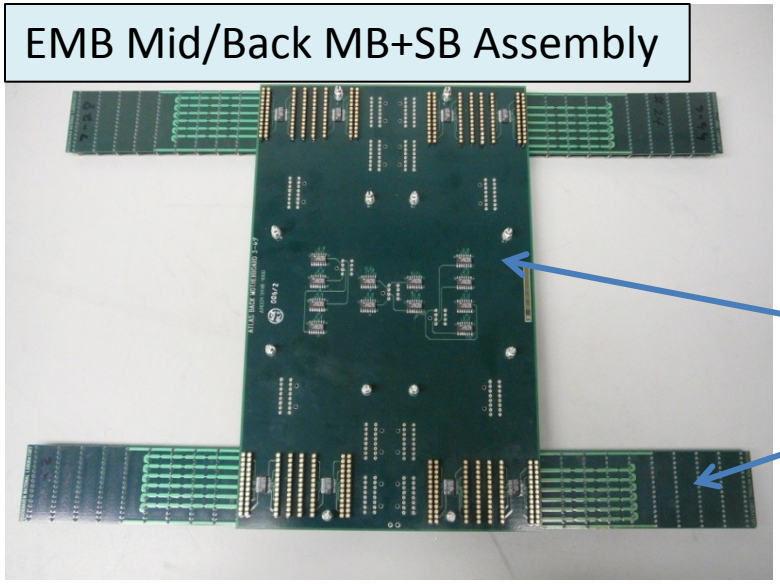
**Design region for low power and long lifetime (moderate inversion)**

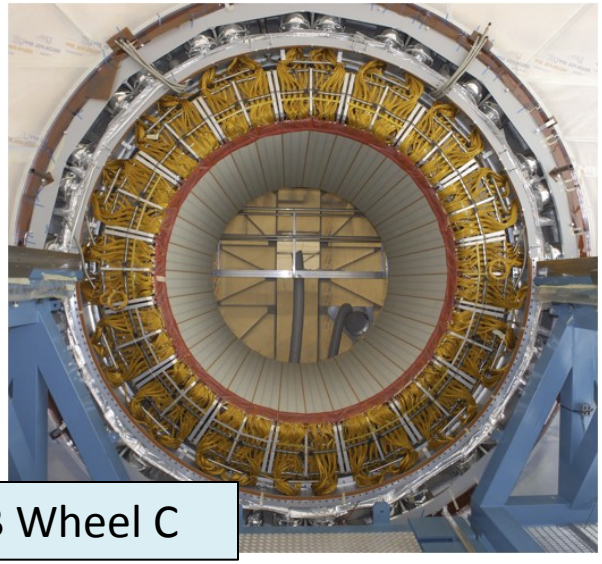
**Strong inversion region**

# Reliability of Cold Electronics (1)

## PCB and Cold Electronics in **ATLAS:** *thermal contraction-expansion*

EMB Mid/Back MB+SB Assembly





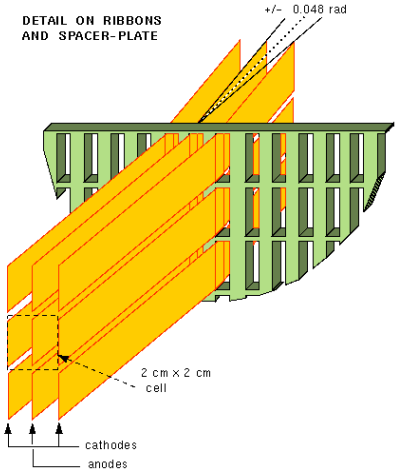
EMB Wheel C

- ATLAS LAr Calorimeter
  - **182,468** readout channels
- EM Barrel Mother Board and Summing Board
  - EMB has **~110,000** detector channels read out by 896x128-ch FEBs
  - **960** Mother Boards (MB)
  - **7,168** Summing Boards (SB)
  - **20,480** resistor network chips, **0.1%**
  - **~110,000** protection diodes on MBs/SBs
- EM Barrel Calorimeter has been cold since 2004
  - Operation: **7 years** so far
  - MB/SB will remain in operation without upgrade for super LHC

- **'Inoperative' channels <0.5%,** as of 05/10/2011
- **Dead channels in the cryostat ~0.02% since 2008**

# Reliability of Cold Electronics (2)

## Cryogenic front-end based on JFETs –**NA48-NA62**




- Liquid Krypton calorimeter
- JFET preamplifiers in LKr: **13,212** channels
- Operated at very high voltage
  - Tested up to 7kV, operated in 3kV
- Failures
  - ~50 because of an HV accident in 1998
  - **~25** cold electronics failures after 1998, **< 0.2%**
  - The last failure recorded was more than 3 years ago
- Always kept at LKr temperature since 1998
- Operation
  - **13 years** so far
  - Plan to run until 2015, expected to be in operation for **17 years**

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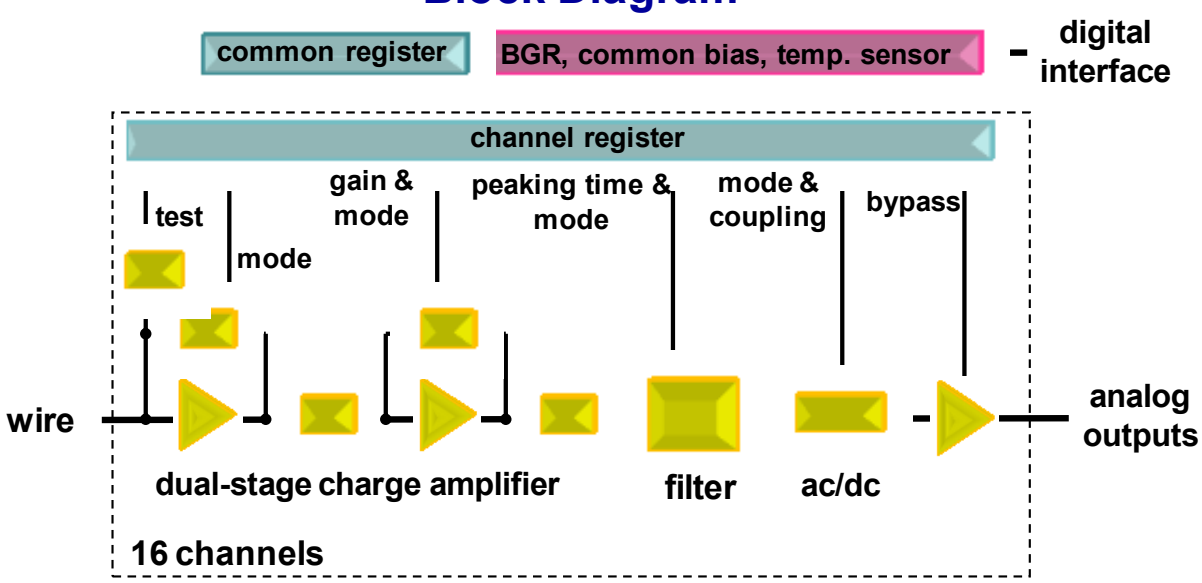
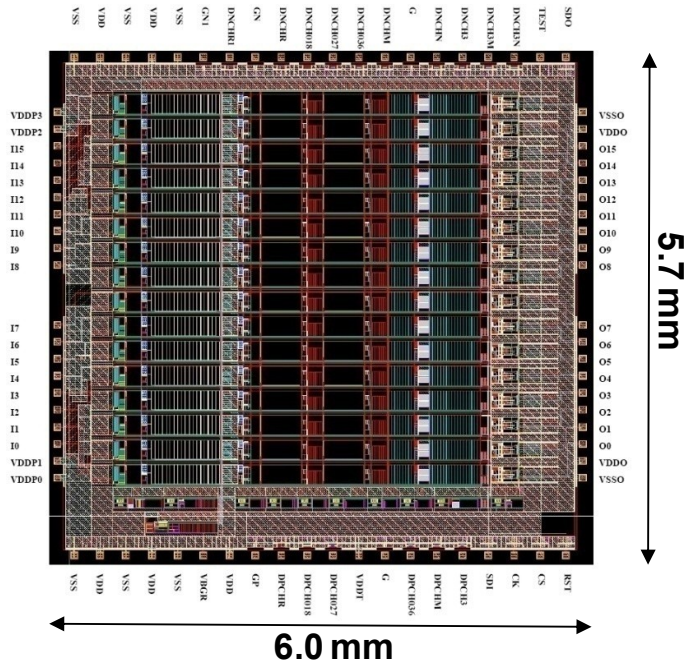
# Analog ASIC

## Block Diagram

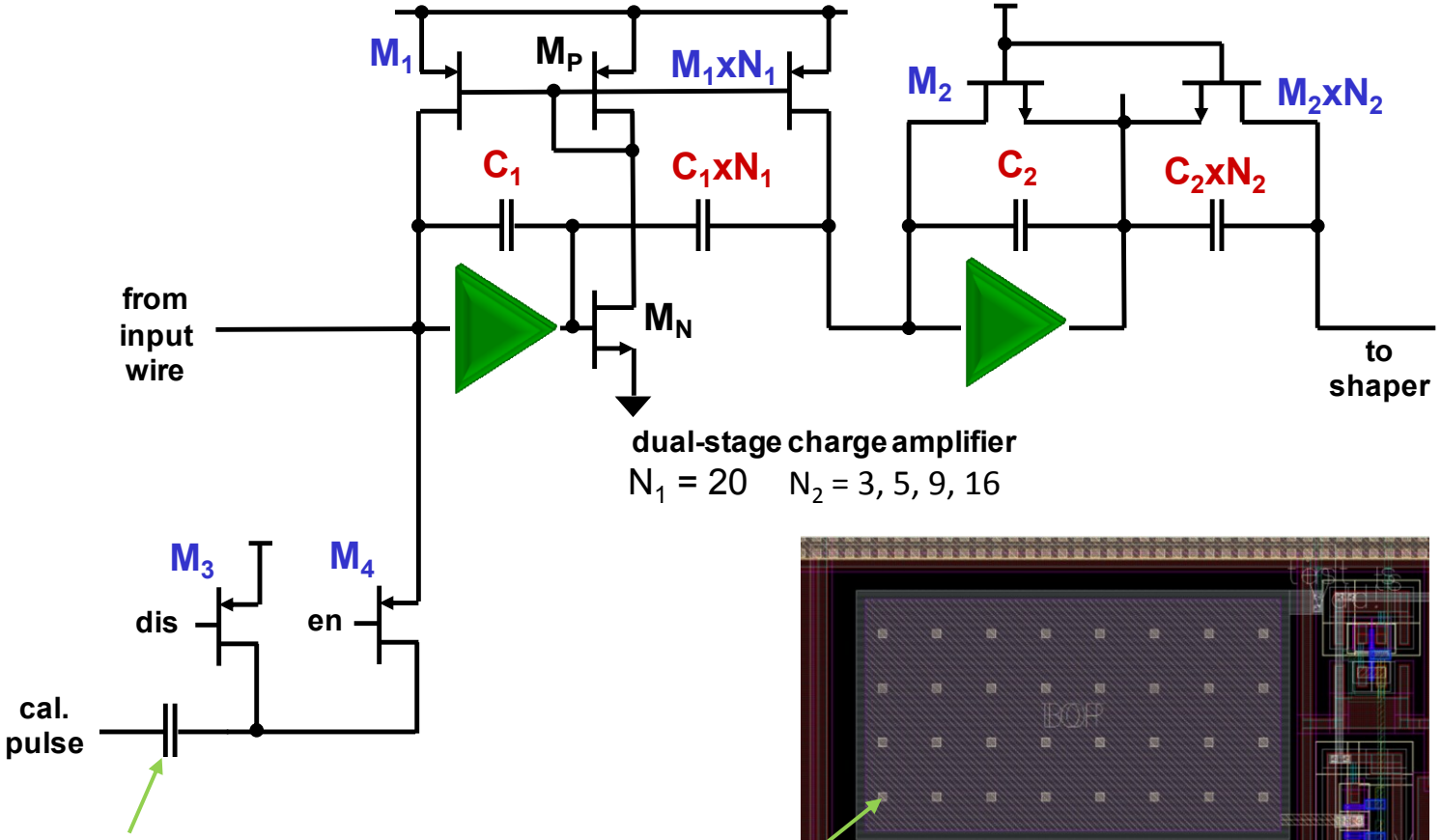



- 16 channels
- charge amplifier, high-order anti-aliasing filter
- programmable gain: 4.7, 7.8, 14, 25 mV/fC
  (charge 55, 100, 180, 300 fC)
  programmable filter
  (peaking time 0.5, 1, 2, 3 μs)
- programmable collection/non-collection mode (baseline 200, 800 mV)
- programmable dc/ac coupling (100μs)

- band-gap referenced biasing
- temperature sensor (~ 3mV/°C)
- 136 registers with digital interface
- 5.5 mW/channel (input MOSFET 3.9 mW)
- single MOSFET test structures
- ~ 15,000 MOSFETs
- **designed for room and cryogenic operation**
- technology CMOS 0.18 μm, 1.8 V

# Cold Electronics ASIC - Front-End Detail and Calibration Scheme






$C_{INJ} \approx 180$ fF

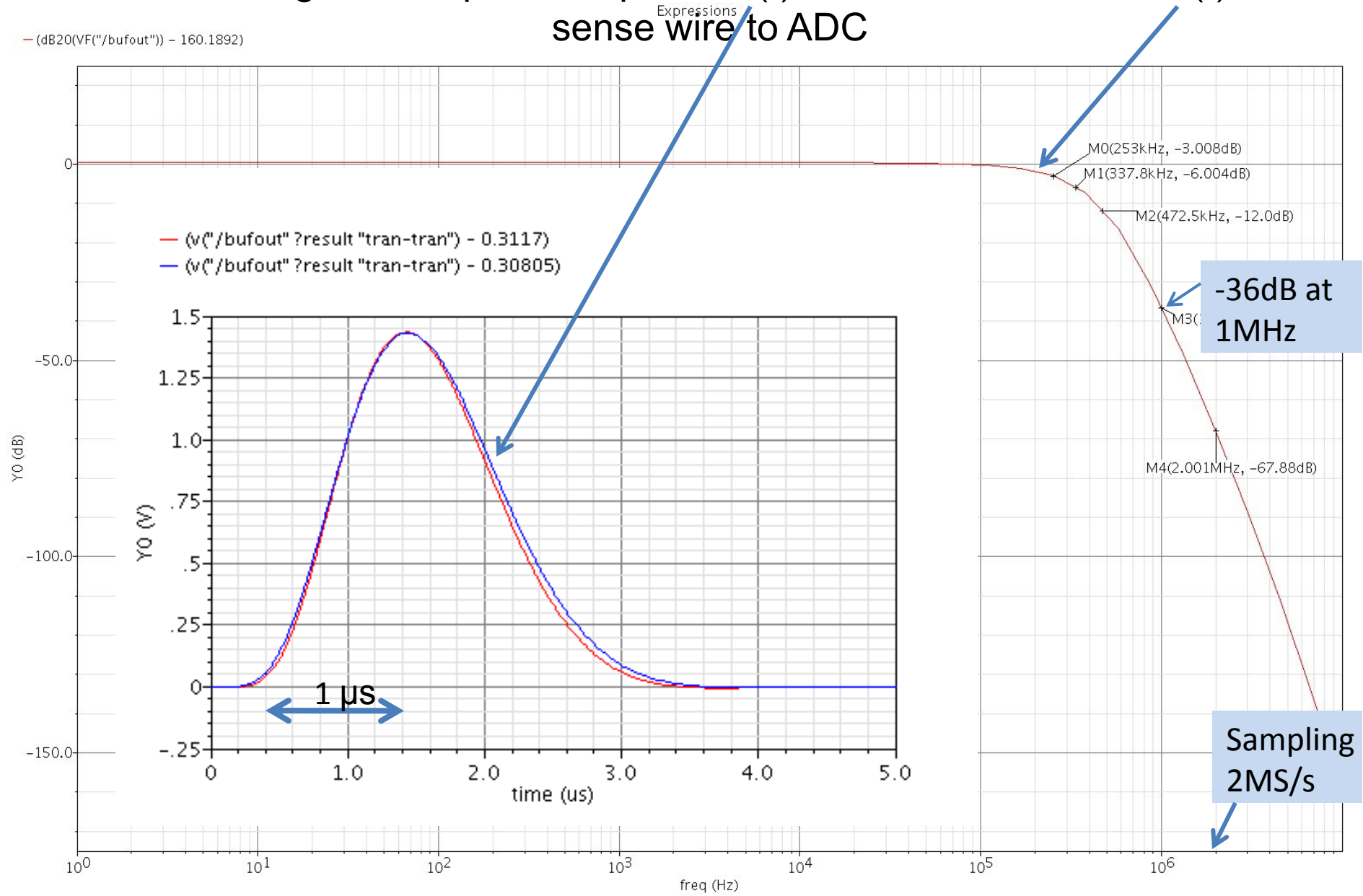
Integrated injection capacitance (10 x 18 μm²)

Measured with high-precision external capacitance

$$C_{INJ} \approx \begin{cases} 184\ fF\ \ at\ \ 300\,K \\ 183\ fF\ \ at\ \ 77\,K \end{cases}$$

Integrated pulse generators on ASICs ⇒ ***Charge sensitivity calibration of entire TPC during assembly, cooling and operation***

# Anti-aliasing filter: Impulse response h(t) and transfer function H(f) from sense wire to ADC



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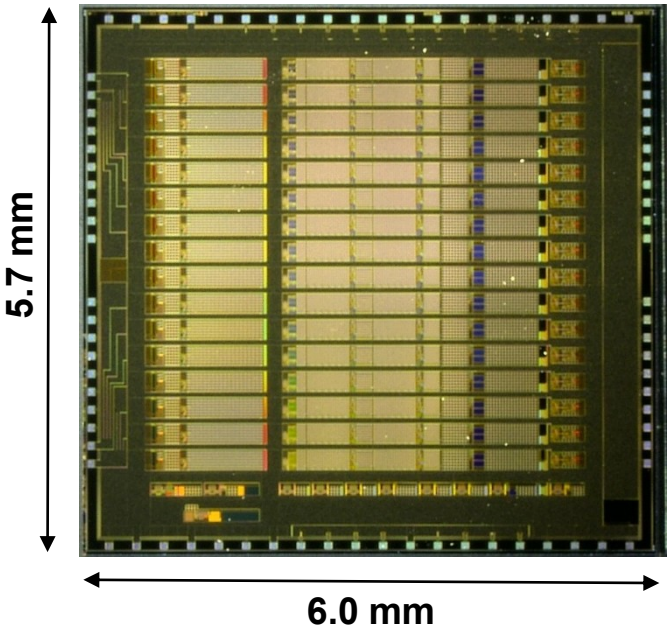
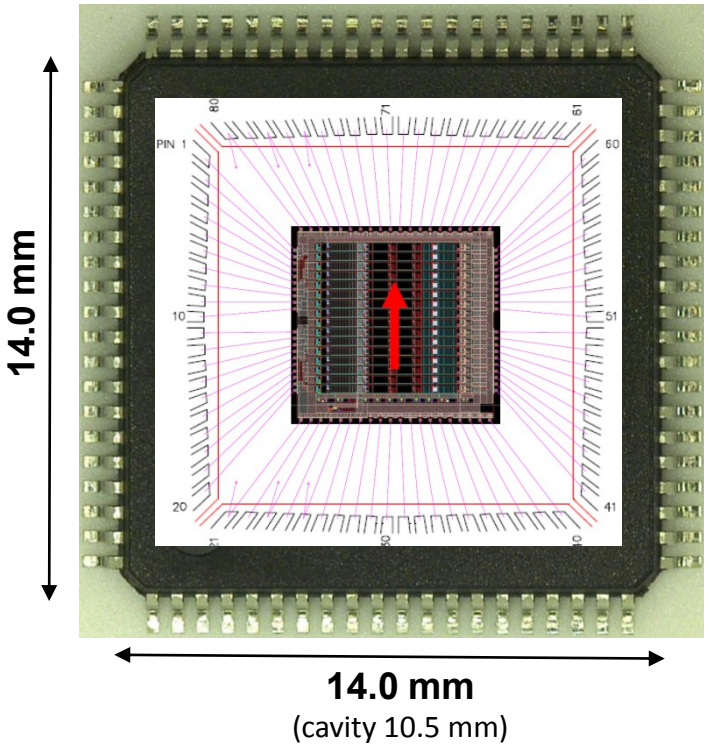
# Analog ASIC: Die and Packaging, Temperature Cycling

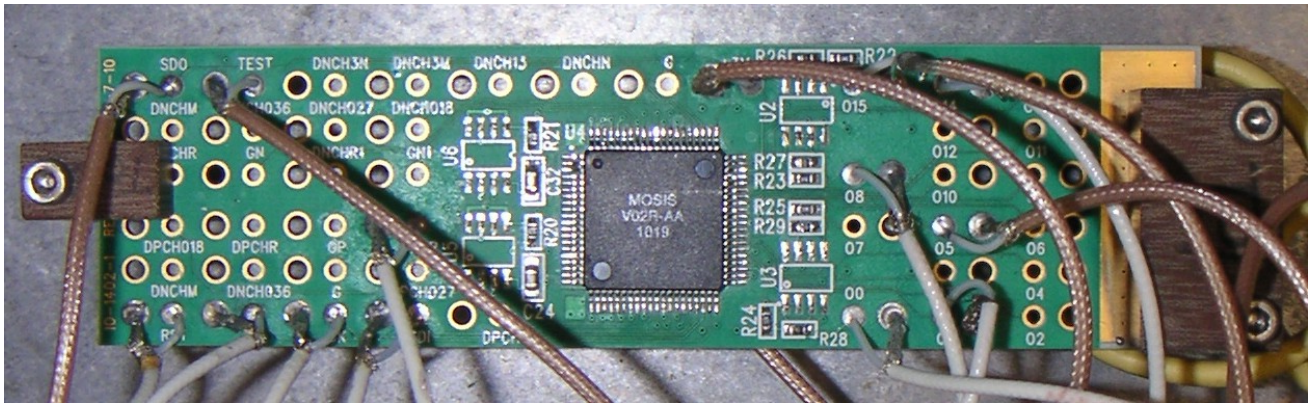
Die Photo




Package Photo




Test Fixture

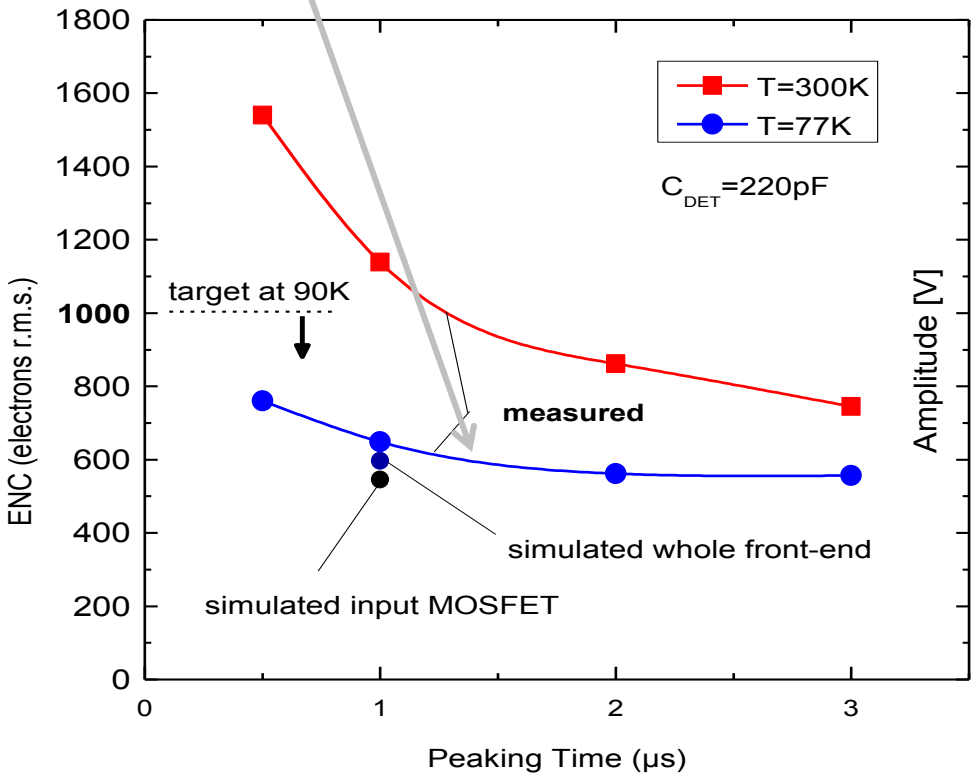



Cycled (abruptly, by pouring LN over the fixture in a dewar) from 300K to 77K more than 30 times

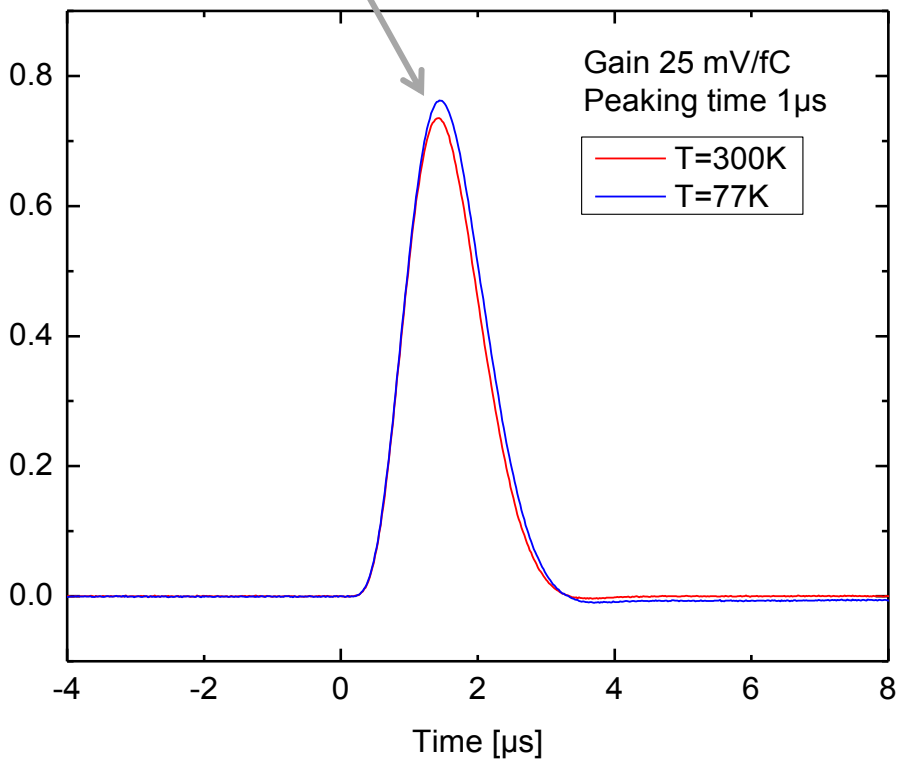
No failure occurred

# Cold CMOS: Results from New FE ASIC (1st prototype cycle)

***Noise*** gets better at 77K
(220pF det. Capacitance):




***Signal*** after preamp+shaper
changes little with temperature:

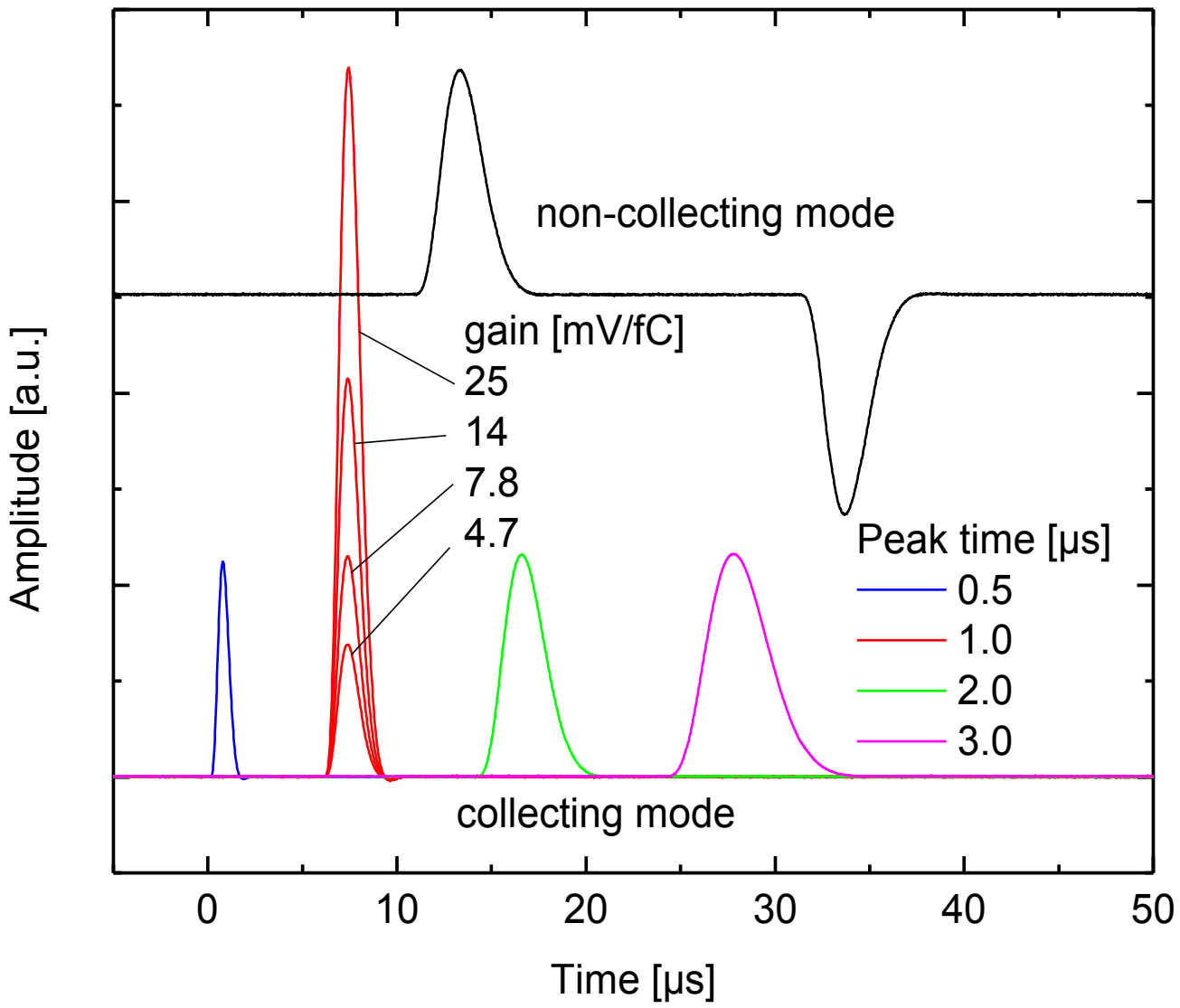



Integrated ***charge calibration*** capacitance
- <u>little change with temperature</u>

Measured with high-precision external capacitance

$$C_{INJ} \approx \begin{cases} 184 \text{ fF at } 300 \text{ K} \\ 183 \text{ fF at } 77 \text{ K} \end{cases}$$

# Signal Measurements: programmable gain, peak time and baseline




**Bandgap Reference:**

$$V_{BGR} \approx \begin{cases} 1.185\ V \text{ at } 300\ ^\circ K \\ 1.164\ V \text{ at } 77\ ^\circ K \end{cases}$$

variation ≈ 1.8 %

**Temperature Sensor:**

$$V_{TMP} \approx \begin{cases} 867.0\ mV \text{ at } 300\ ^\circ K \\ 259.3\ mV \text{ at } 77\ ^\circ K \end{cases}$$

~ 2.86 mV / °K

Programmable gain, peaking time and baseline

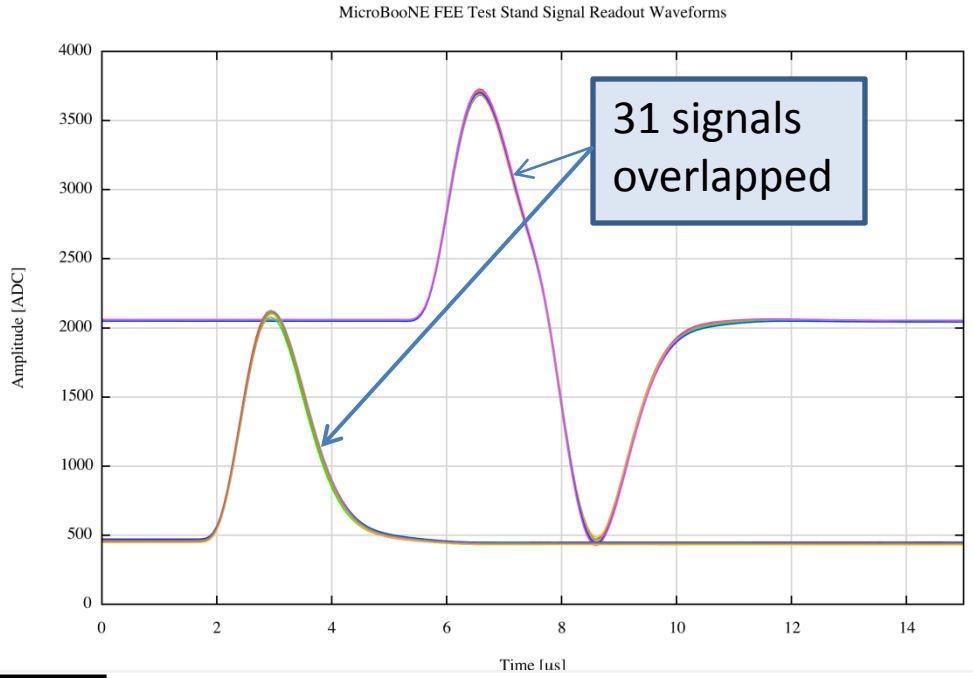
Maximum charge 55, 100, 180, 300 fC

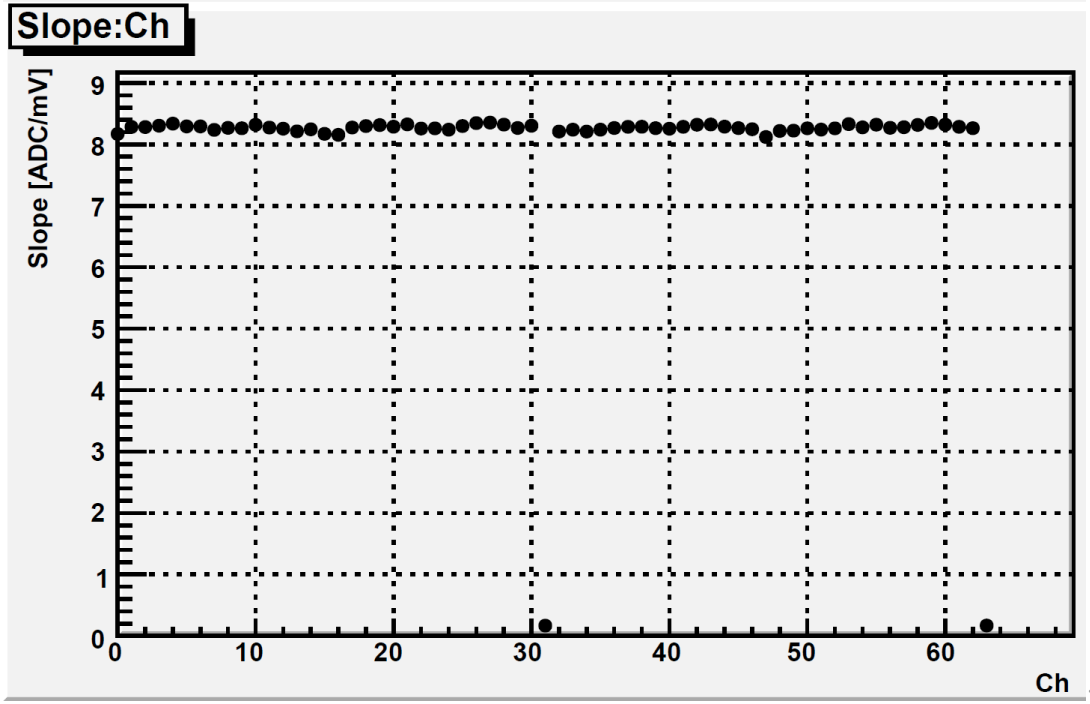
# Analog ASIC: *gain and waveform uniformity*

Four ASICs, **4x16** channels (one lead of the 32-channel cable not connected)

Residuals from a linear fit < 0.3%
Crosstalk < 0.3%

*These measurements performed with enireMicroBooNE signal chain*:
Analog ASIC+cold cable+
+intermediate amplifier+ADC



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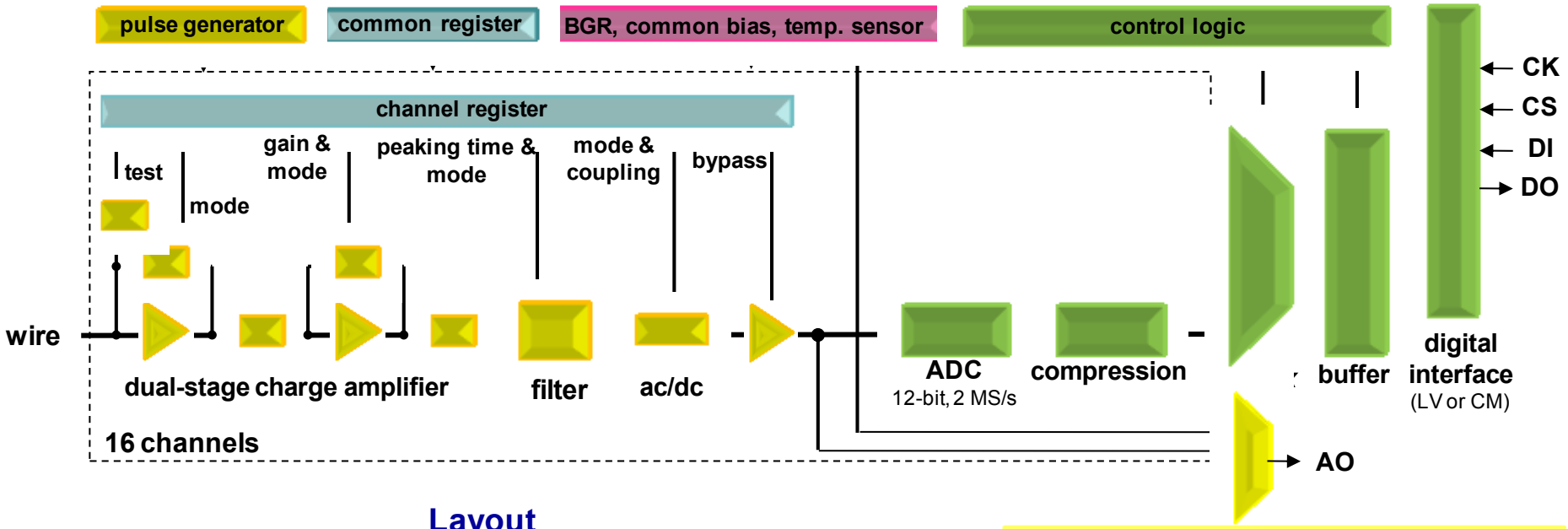
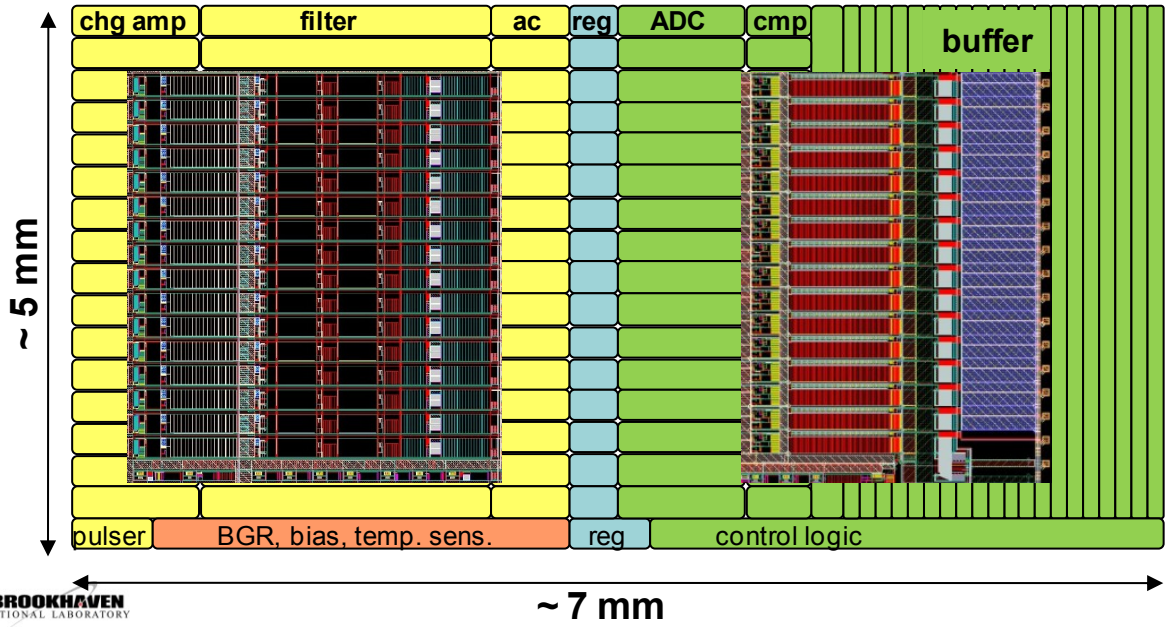
# Front-End ASIC with 16:1 digital multiplexing

## Block Diagram




## Layout




- 16 channels
- charge amplifier (progr. gain)
- high-order filter (progr. time constant)
- ac/dc, progr. baseline
- test capacitor, channel mask
- ADC (12-bit, 2 MS/s)
- compression, progr. discrimination
- multiplexing and digital buffering
- LV or CM digital interface
- pulse generator, analog monitor
- temperature sensor
- estimated size ~ 6 x 8 mm²
- estimated power ~ 10 mW/channel

# Summary and Future Work

- CMOS is "happier" in cryogenic environment (tested down to 40K)
- Low-noise demonstrated:
  - ENC~ 600$e^-$ rms at 200pF, ~5mW/ch. (analog part)
  - characterization and modeling of CMOS 180nm successful
- > 30 years lifetime using design guidelines consistent with low power design
- Critical building blocks (front-end, ADC) developed, fabricated and tested separately
- ***Entire TPC can have uniform calibrated (<1%) charge sensitivity***
- *Future work:*
  - Continue with the signal chain development, digital buffer, digital interface,
  - merge and finalize into a single chip, analog FE+ADC+buffer with 128:1 multiplexing (8:1 separately)

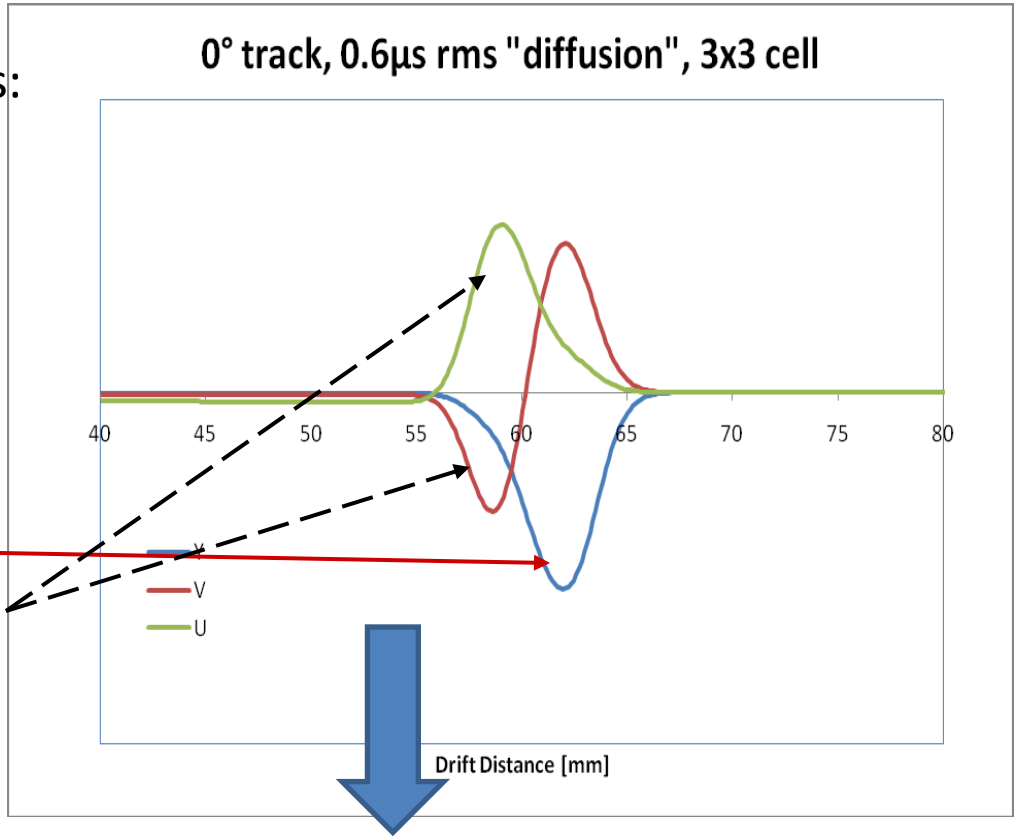
# Backup slides

# Signals in LAr TPC

*Charge signal:*

- A 3mm MIP track should create *210keV/mm x 3mm /23.6eV/e = 4.3fC.*
- After a 1/3 initial recombination loss: *~2.8fC*
- Assume the drift path to equal the charge life time, reducing the signal to 1/e≈0.368.
- The expected signal for *3mm* wire spacing is then ≈*1fC=6250 e*, … and for *5mm, ≈$10^4$ e*, for ***the "collection signal"***.
- The induction signals are smaller
- The ***time scale*** of TPC signals is determined by the ***wire plane spacing*** and ***electron drift velocity,*** *(~1.5 mm/μs at 500 V/cm).*

Induced Current Waveforms on 3 Sense Wire Planes:




Sampling rate ***≤ 2 Ms/s***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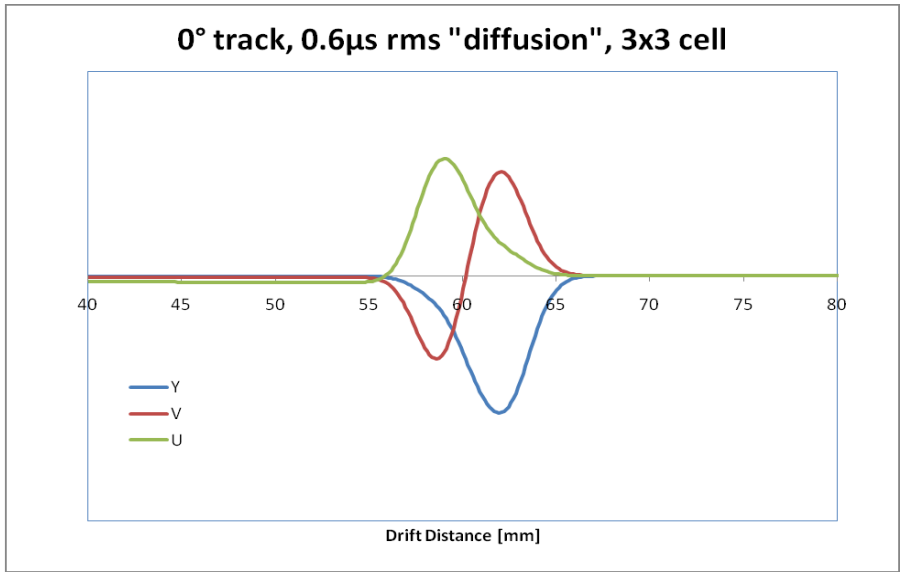
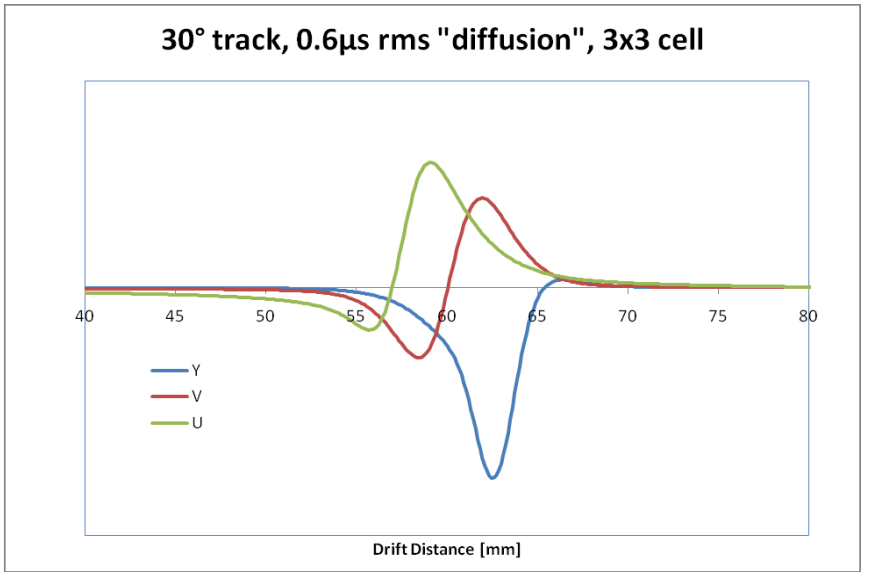
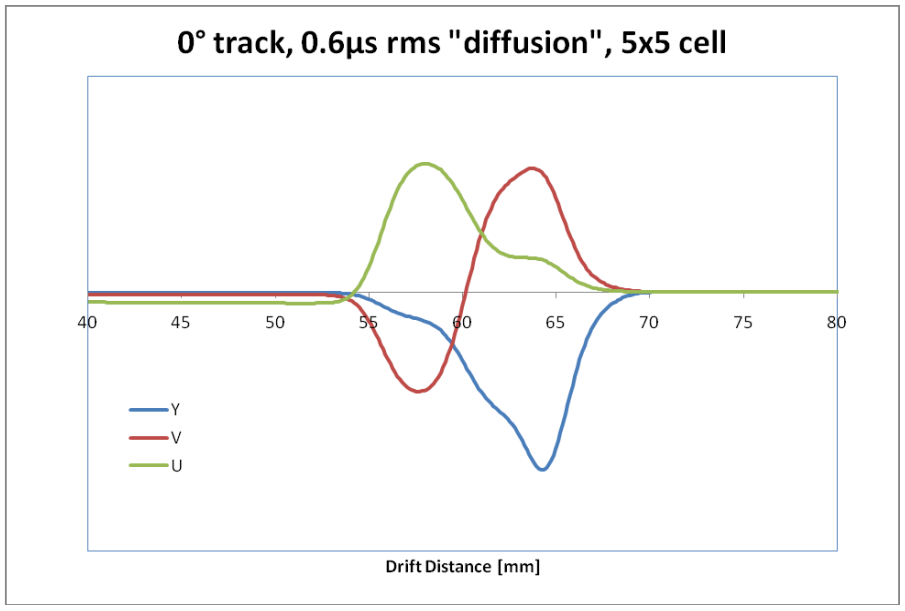
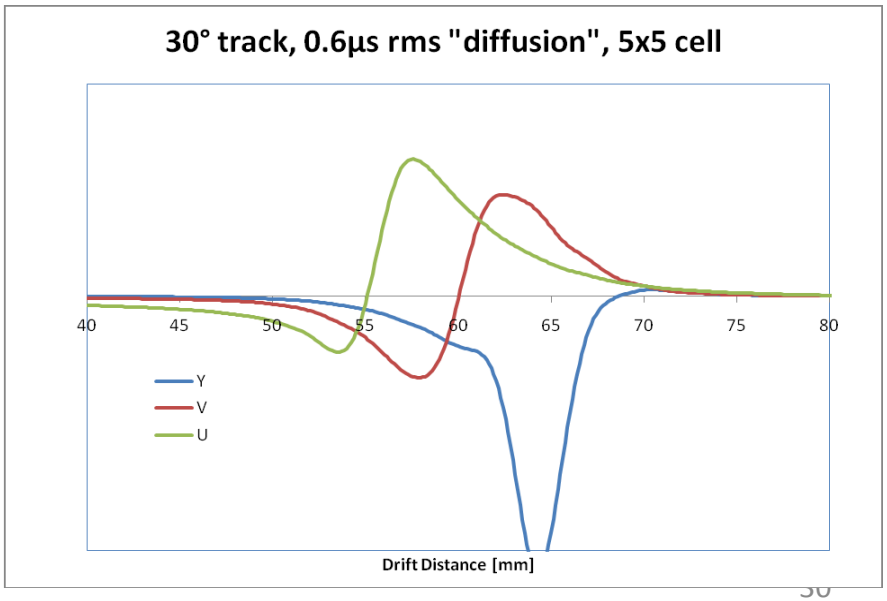
# Relative Induced Current Waveforms on 3 Sense Wire Planes *vs* Wire Spacing and MIP Angle



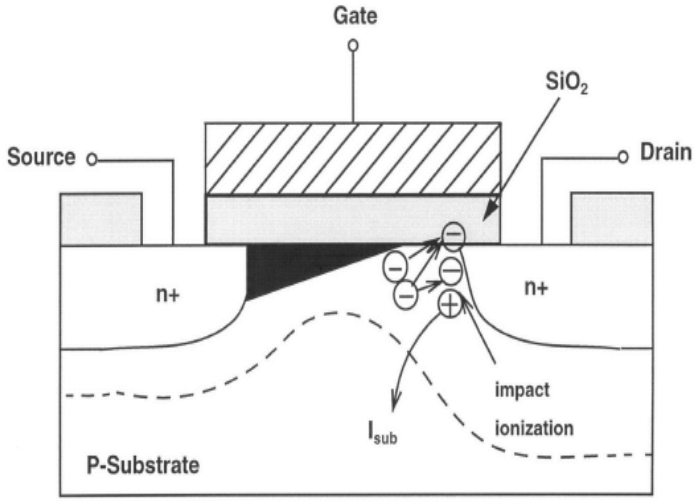
# Readout data rates/APA due to background at ~800ft

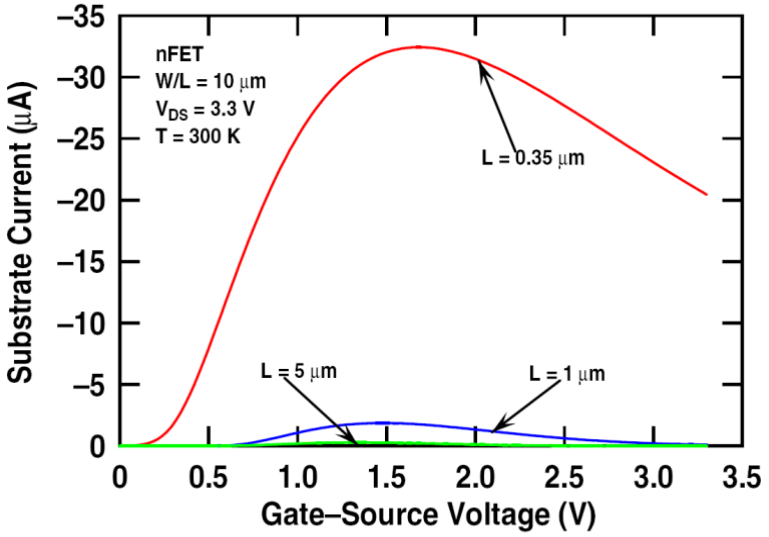
| Source | Event Rate | Data Rate |
|---|---|---|
| $Ar^{39}$ | 122 kHz | 9.8 Mb/s |
| $Kr^{85}$ | 28 kHz | 2.3 Mb/s |
| FE series noise | 21.5 kHz | 0.4 Mb/s |
| cosmic muons | 2.4 Hz | 0.2 Mb/s |
| $Co^{60}$ gammas | 2.5 kHz | 0.2 Mb/s |
| Total | | 12.9 Mb/s |

# CMOS Lifetime Overview (1)

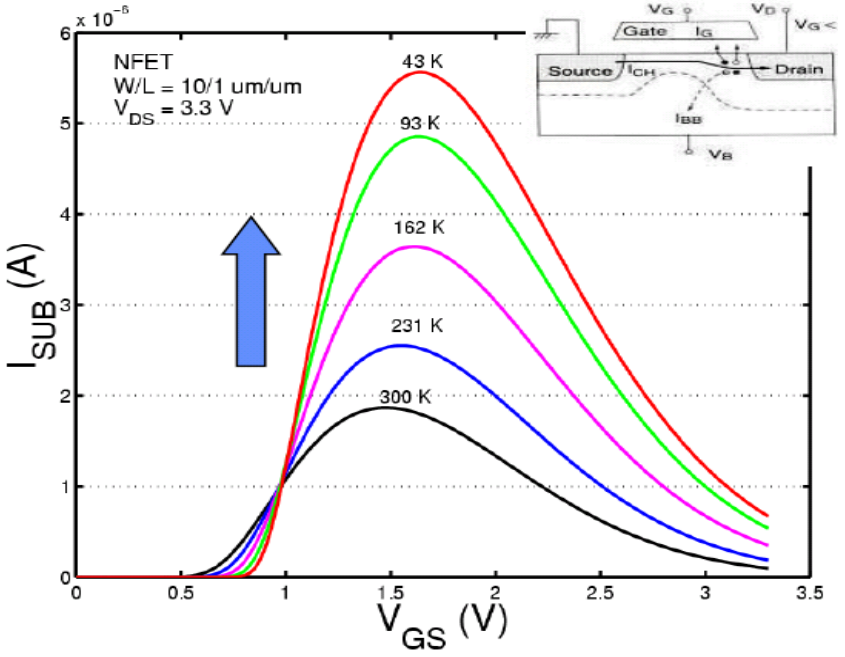
Lifetime of CMOS devices *at any temperature* is limited by Hot Carrier Degradation (HCD). During normal operation electron-hole pairs are generated in proximity of the drain from impact ionization by electrons. Holes contribute to the bulk (substrate) current without consequences (impact ionization affects much more n-channel transistors). *The principal life-limiting consequence of the electrons trapped in the gate oxide is to cause a gradual decrease (degradation) of the transconductance $g_m$.*

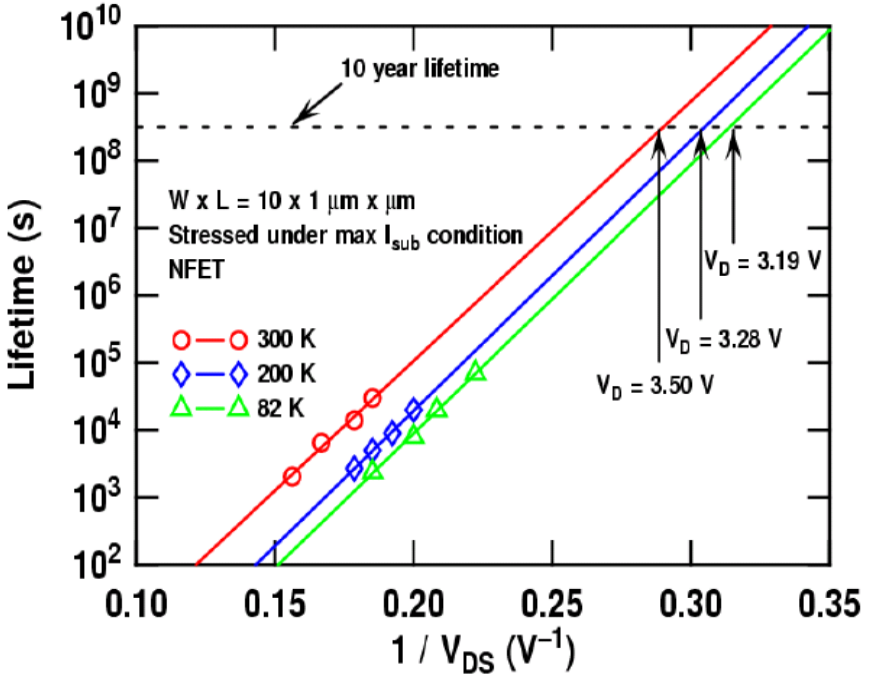
The amount of impact ionization depends on the device operating point (drain current density and drain-source voltage $V_{DS}$), channel length L, and temperature, and it can be monitored by measuring the device bulk (substrate) current $I_{sub}$ . The maximum ionization occurs for minimum-L devices operating at $V_{DS} = V_{DD}$ ($V_{DD}$ is the maximum recommended supply voltage) and $V_{GS} \approx V_{DD}/2$. It also increases as the temperature decreases.



# CMOS Lifetime (2)




Impact ionization increases with the drain current. Typically at 90 K the impact ionization is about twice that at – 50 C (220 K), and the lifetime consequently decreases . *Design guidelines to constrain the electric field and/or the current density to values somewhat lower than at 220K must be applied in order to guarantee >30 years lifetime.*

# CMOS Lifetime (3)

In ***digital operation*** lifetime can be increased to more than ***30 years*** by *two of the three* following steps:

- increasing the channel length L by about 50% (note: since the devices at cryogenic temperature are faster, the circuit speed is not compromised)
- decreasing the operating frequency: operating at 50% of the maximum frequency doubles the lifetime; *we will operate at clock frequencies more than one order of magnitude lower than the ring oscillator frequency*
- decreasing the supply voltage: a 10 % decrease in $V_{DD}$ increases the lifetime by about one order of magnitude

# CMOS Lifetime (4)

In ***analog operation*** lifetime can be increased to more than ***30 years*** by one or more of the following steps:

- operating the devices at low $V_{GS}$: in moderate inversion the lifetime is increased by several orders of magnitude (note: *in our low-power ASIC design almost all devices operate in moderate inversion*)
- using non-minimum channel length for those devices which approach strong inversion
- operating at $V_{DS}$ lower than $V_{DD}$ which is normally achieved in all analog circuits

***In the design of our front-end ASIC at least two of the above conditions have been satisfied for every single transistor (of ~ 15,000 transistors in the circuit).***

These guidelines, extracted from the data and models provided by the foundries and from the results reported in the literature, will be verified by performing accelerated tests. Dedicated test structures have been fabricated. These tests are being performed at BNL, Fermilab and Georgia Tech.

# MicroBooNE signal feedthrough (proven ATLAS design, 1920 pins, 960 channels)