Firmware Design for Particle Timing Measurements in the CMS ETL

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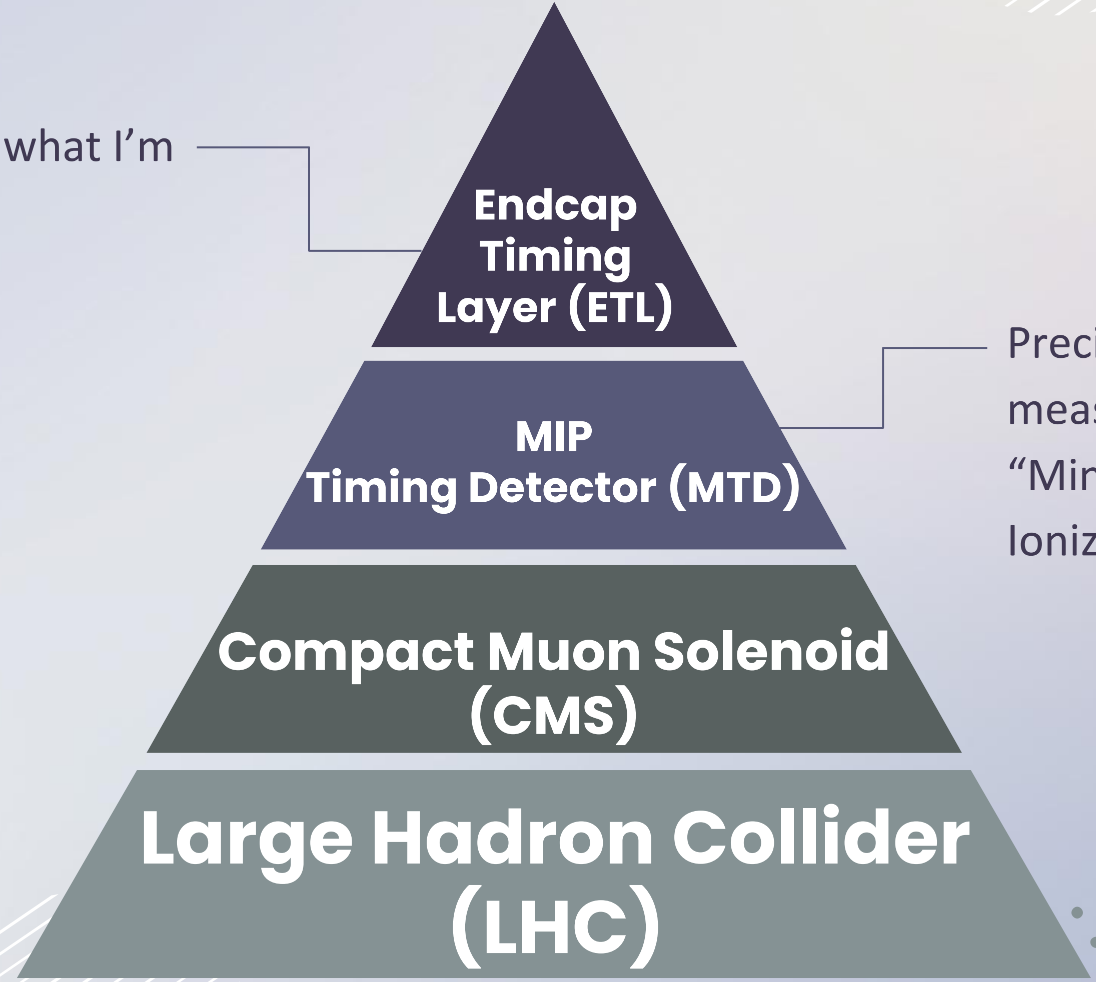
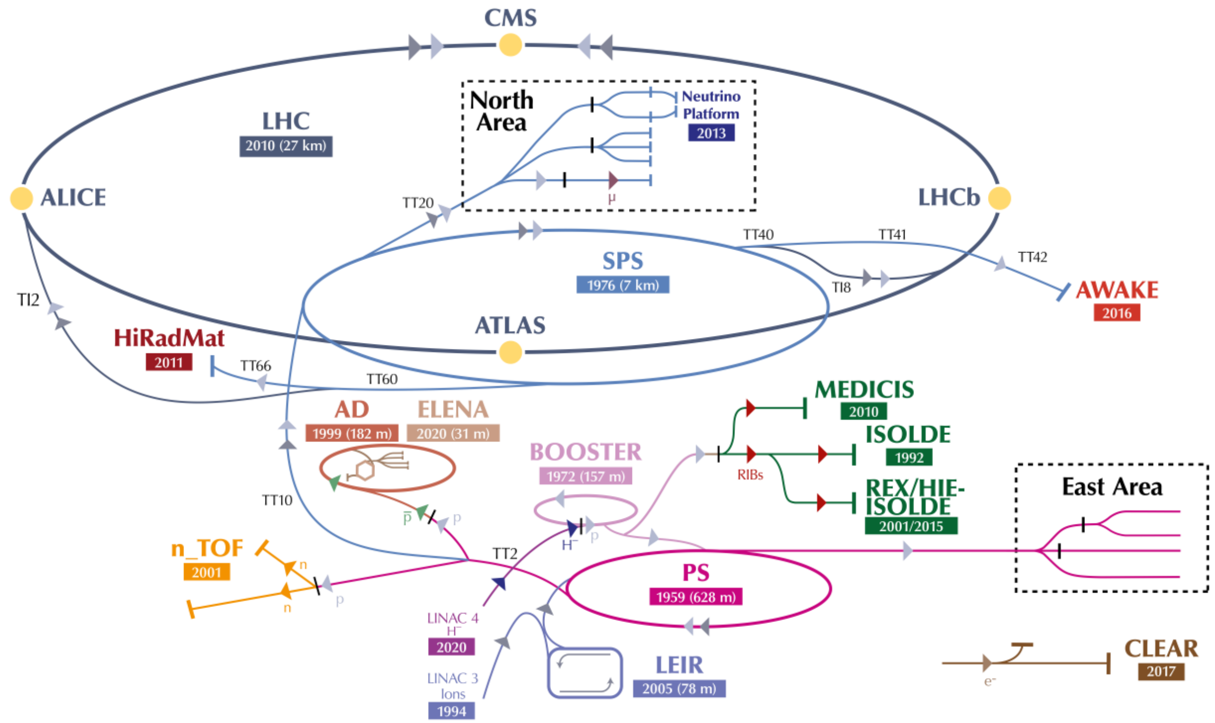
Part of MTD: what I’m working on.



Precision timing measurement of “Minimum Ionizing Particles”.

The CERN accelerator complex
Complexe des accélérateurs du CERN



The CERN accelerator complex
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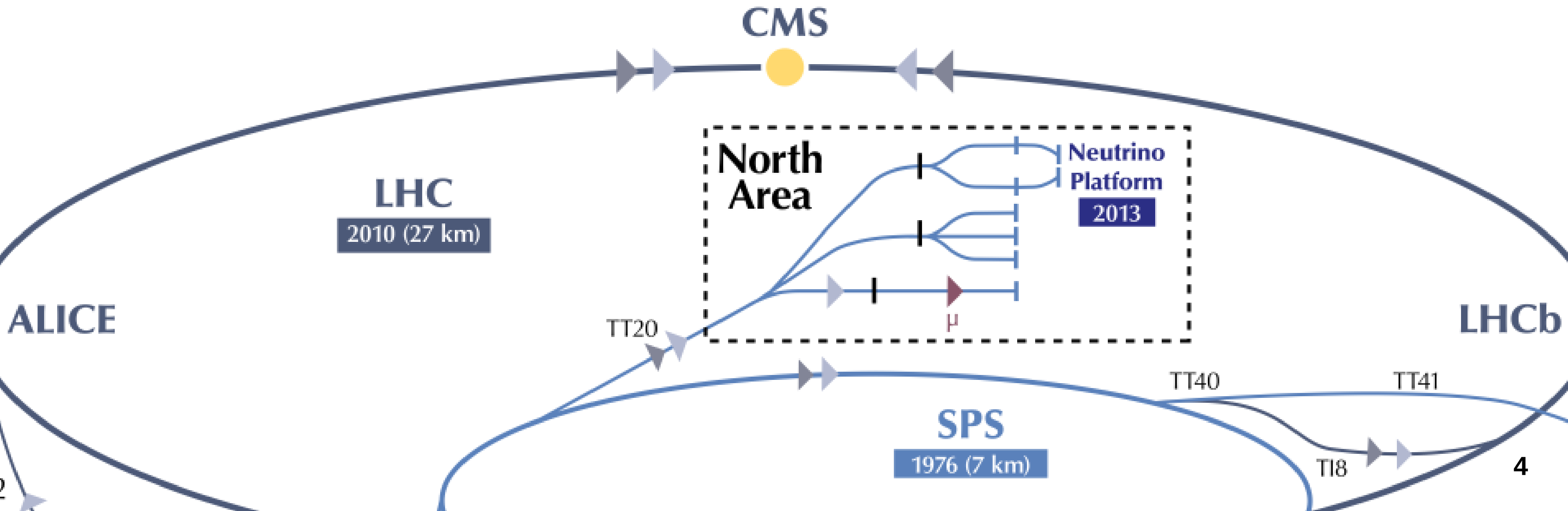
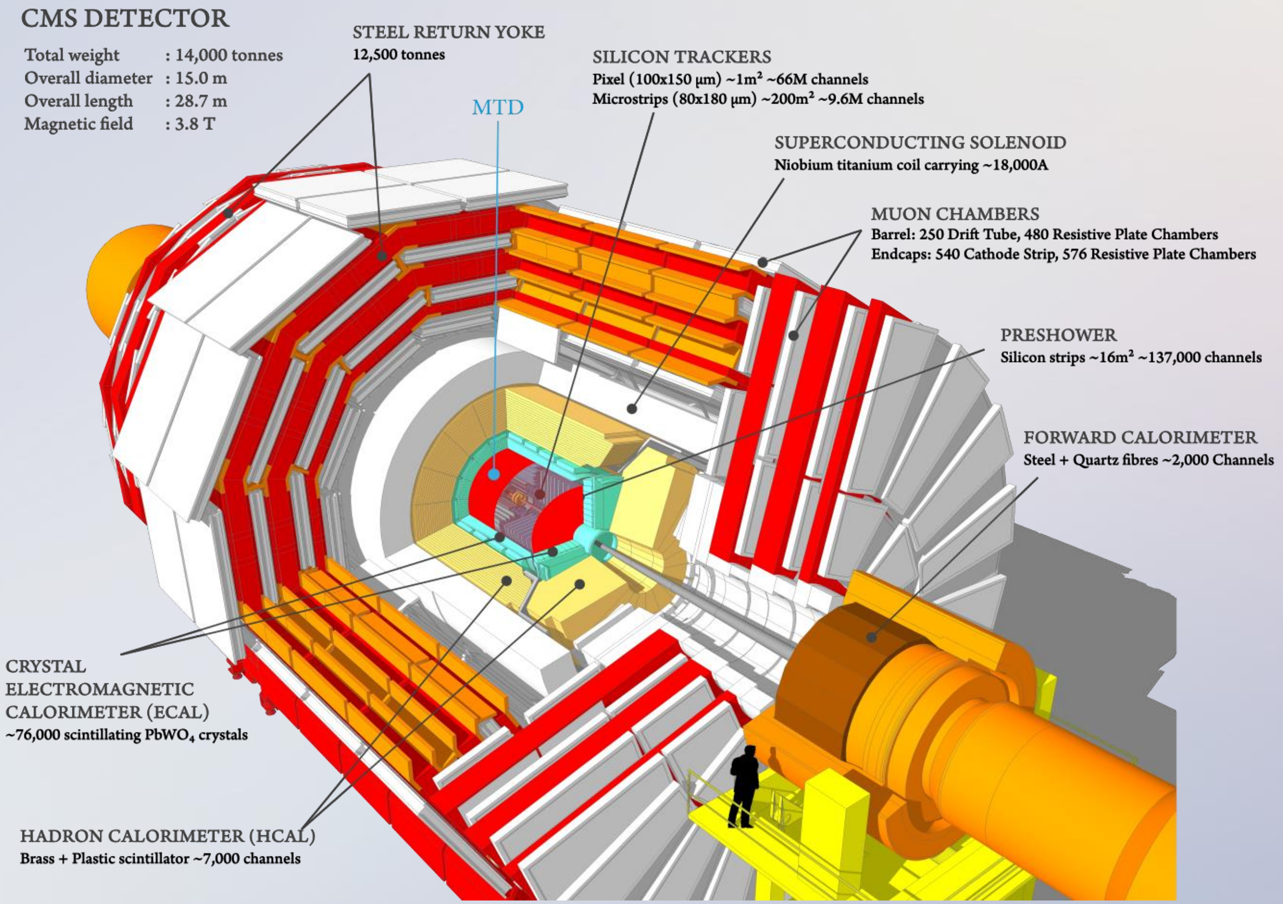
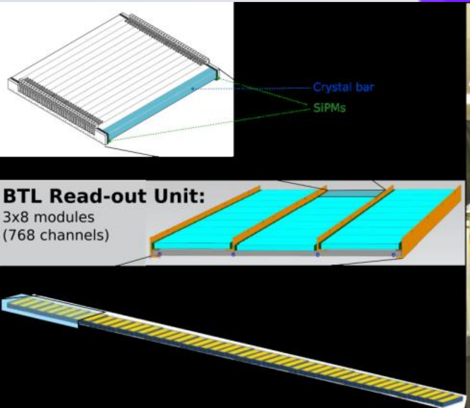
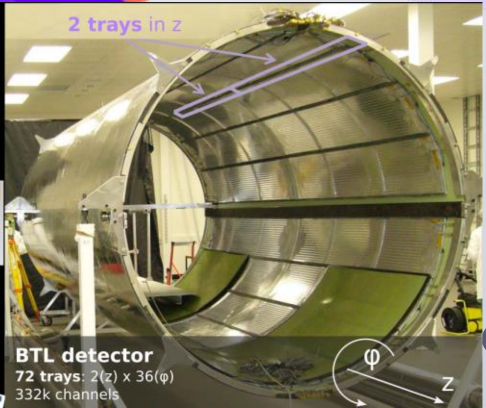
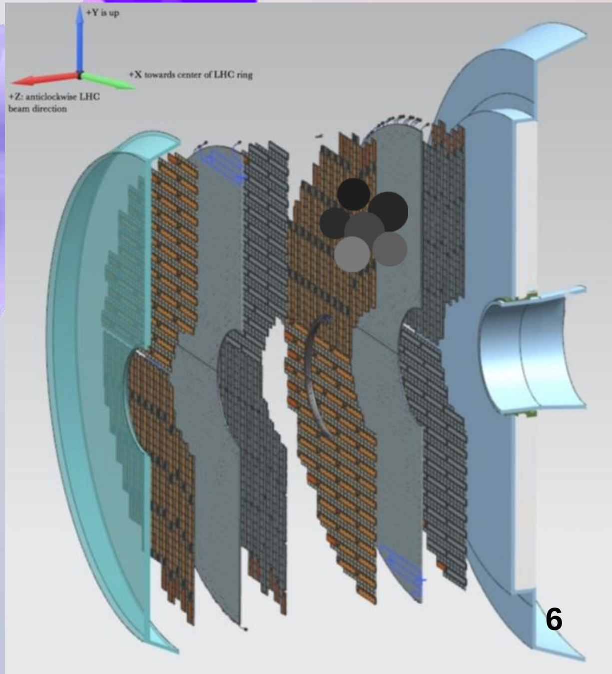



CMS DETECTOR
Total weight : 14,000 tonnes
Overall diameter : 15.0 m
Overall length : 28.7 m
Magnetic field : 3.8 T
STEEL RETURN YOKE
12,500 tonnes
MTD
SILICON TRACKERS
Pixel (100x150 μm) ~1m² ~66M channels
Microstrips (80x180 μm) ~200m² ~9.6M channels
SUPERCONDUCTING SOLENOID
Niobium titanium coil carrying ~18,000A
MUON CHAMBERS
Barrel: 250 Drift Tube, 480 Resistive Plate Chambers
Endcaps: 540 Cathode Strip, 576 Resistive Plate Chambers
PRESHOWER
Silicon strips ~16m² ~137,000 channels
FORWARD CALORIMETER
Steel + Quartz fibres ~2,000 Channels
CRYSTAL ELECTROMAGNETIC CALORIMETER (ECAL)
~76,000 scintillating $PbWO_4$ crystals
HADRON CALORIMETER (HCAL)
Brass + Plastic scintillator ~7,000 channels

MTD: MIP Timing Detector





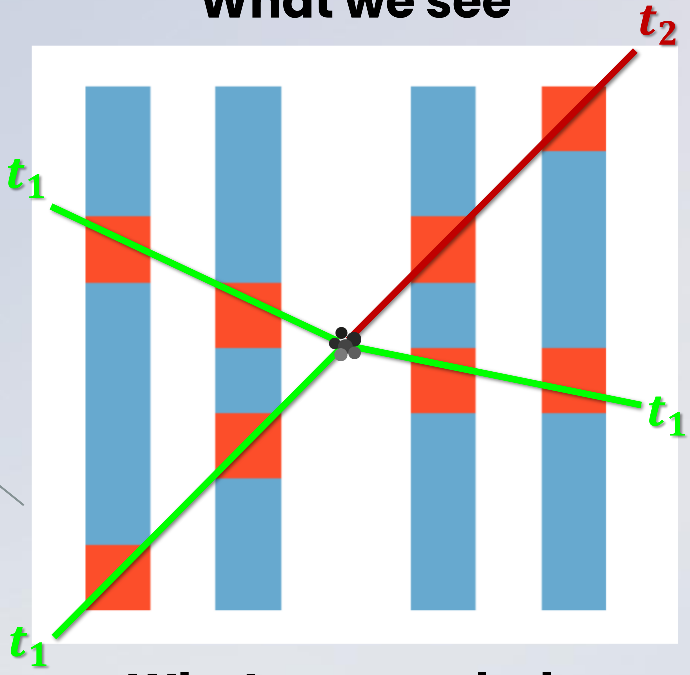


The Main Goal of MTD

Is to measure particles with 30 ps resolution at the beginning of its lifetime.

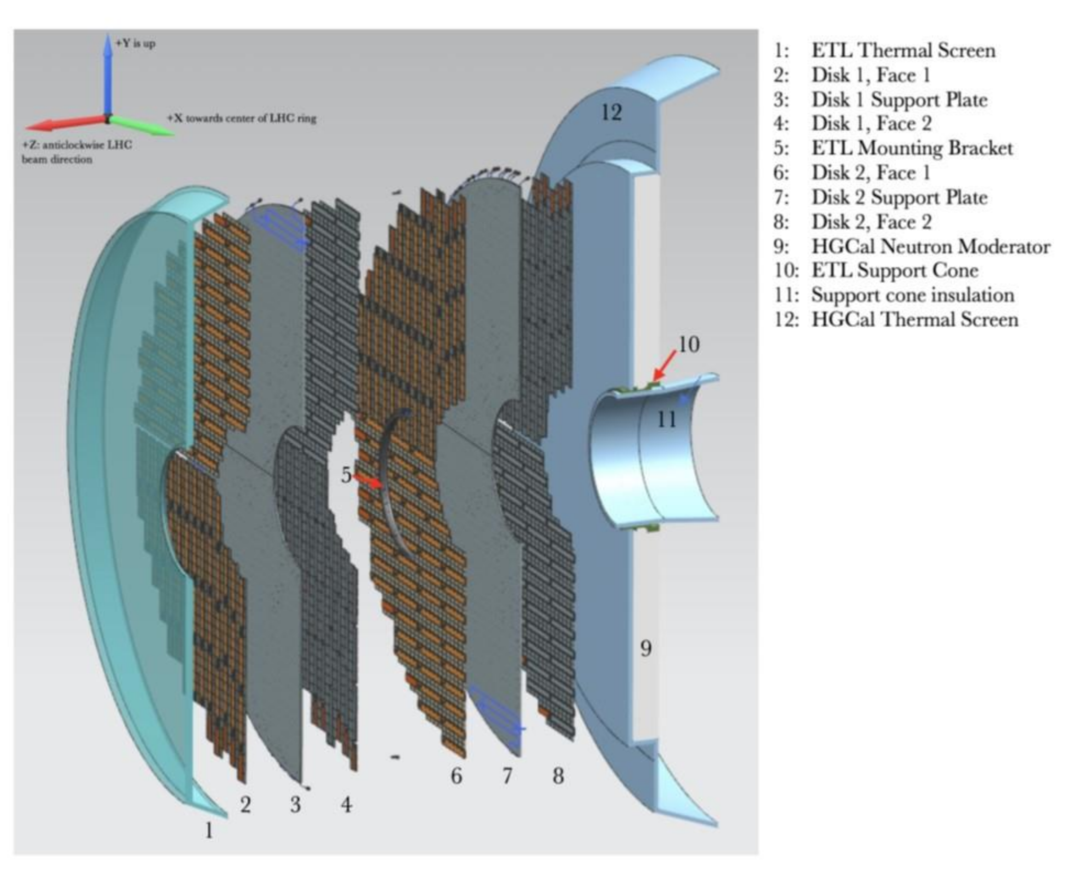
30 picoseconds = 0.000000000030 seconds

What we see



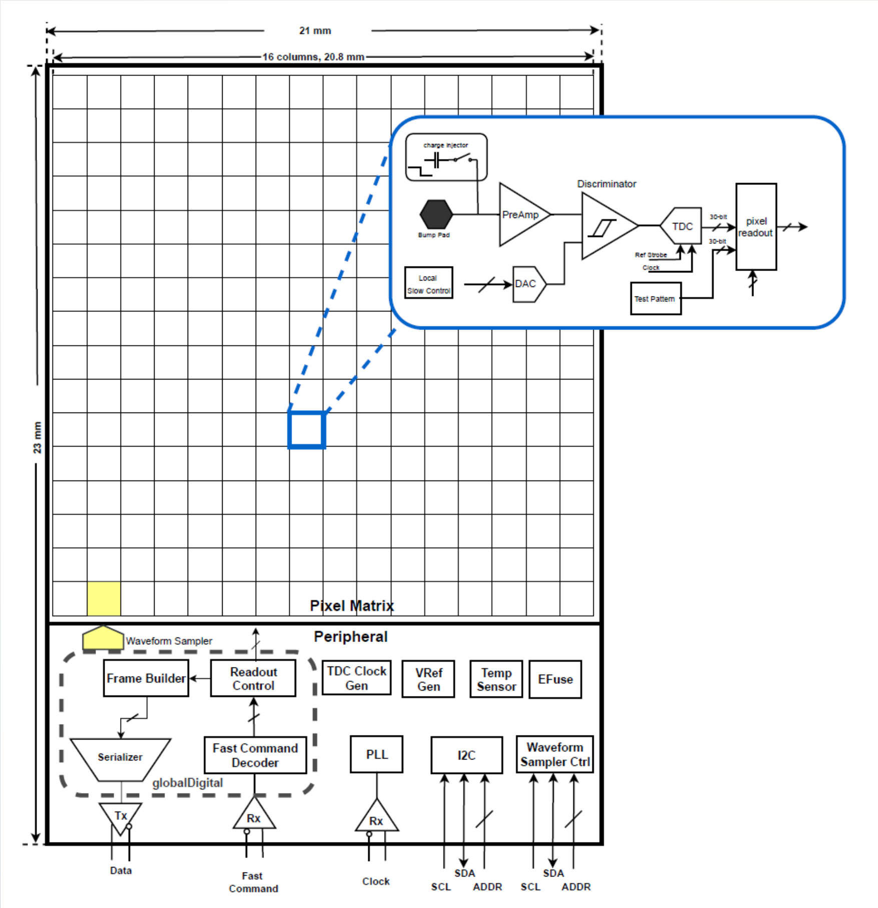
What we conclude

The detector separates the tracks coming from different simultaneous collisions.



Modified from Ziga Brencic, CERN Student Session 2018

ETROC is the **ASIC** designed for precision timing in **CMS ETL**. **ETROC2** is the first full-size fully-functionality prototype of **ETROC**, which aims to achieve **50 ps per hit** time resolution. An **ETROC2** includes a 16 × 16 pixel matrix and a chip peripheral.



Raw data frame

Frame Header	0	15'H3C5C	2'B00	L1Counter(8B)	TYPE (2B)	BCID (12B)
DATA Word	1	EA(2B)	Col_ID(4B)	Row_ID(4B)	TDC_DATA/TEST PATTERN(29B)	
Frame Trailer	0	CHIPID(17B)	STATUS(6B)	HITS(8B)	CRC (8B)	
Frame Filler	0	15'H3C5C	2'B10	RT_L1Counter(8B)	EBS (2B)	RT_BCID (12B)

Input Module	Reads 8 bits by 8 bits from an incoming bitstream.
Header Detection Module	Detects the "Header" data type in the incoming bitstream.
Data Word Storage Module	Stores the data when the "Header" is detected.
Hamming Coding Module	Checks for errors using **Hamming coding**.
FIFO Buffer Module	Puts the entire information (data word with error check result) into a FIFO buffer.

Example On Hamming (10,8) Code Error Correction

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity hamming_code is
  Port ( data_in : in  STD_LOGIC_VECTOR(7 downto 0);
      encoded_data : out  STD_LOGIC_VECTOR(9 downto 0));
end hamming_code;

architecture Behavioral of hamming_code is
  signal p1, p2 : STD_LOGIC;
begin
  -- Calculate parity bits
  p1 <= data_in(0) XOR data_in(1) XOR data_in(3) XOR data_in(4) XOR data_in(6) XOR data_in(7);
  p2 <= data_in(0) XOR data_in(2) XOR data_in(3) XOR data_in(5) XOR data_in(6) XOR data_in(7);

  -- Create encoded data
  encoded_data(0) <= data_in(0);
  encoded_data(1) <= data_in(1);
  encoded_data(2) <= p1;
  encoded_data(3) <= data_in(2);
  encoded_data(4) <= data_in(3);
  encoded_data(5) <= data_in(4);
  encoded_data(6) <= p2;
  encoded_data(7) <= data_in(5);
  encoded_data(8) <= data_in(6);
  encoded_data(9) <= data_in(7);

end Behavioral;
```

Conclusion

Including the **MIP Timing Detector** in the upgrade plan for the **HL-LHC era** will help to assign charged tracks to the correct interaction vertices in bunch crossing with an **average of 200 collisions** or more.

Thank You

Special thanks to:

My family
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