CMS HGCAL Train on Track for Particle Detection

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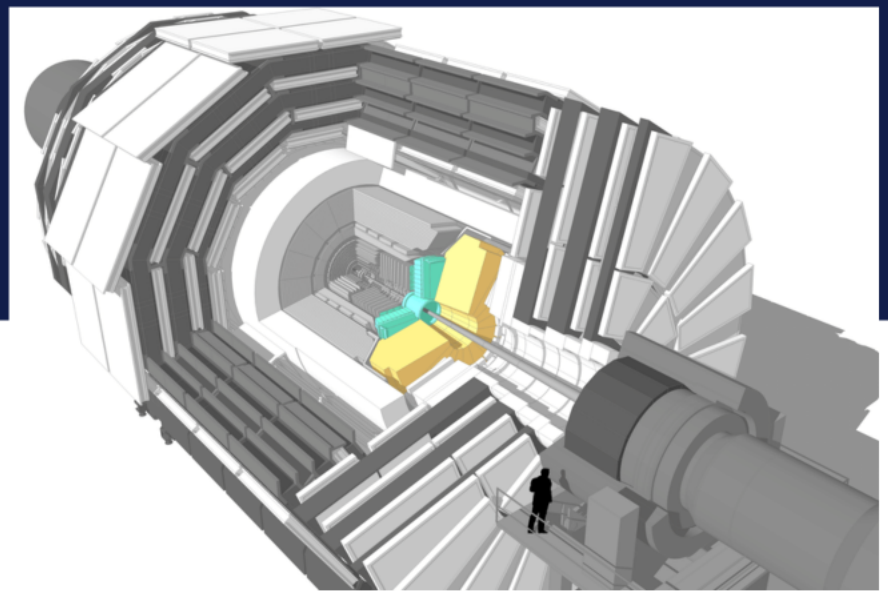
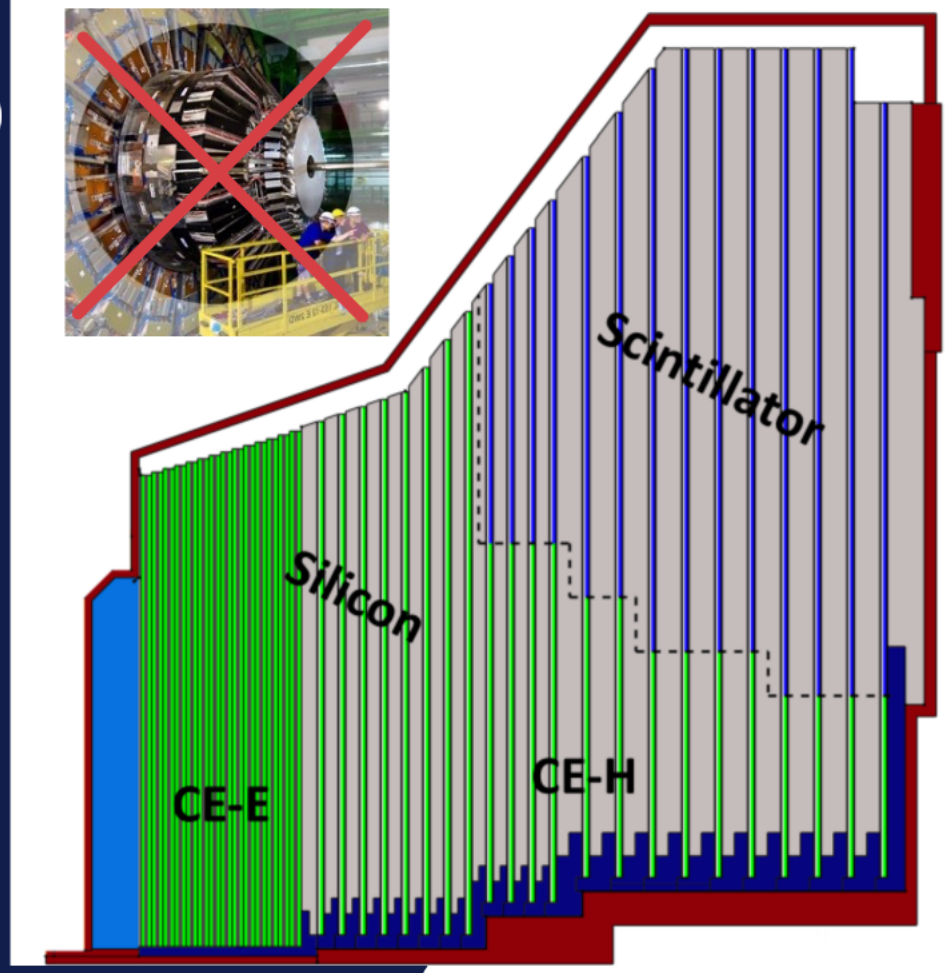


New endcap calorimeter: high granularity calorimeter

- Electromagnetic calorimeter (CE-E) - 47 layers
- Hardronic calorimeter (CE-H)
- Scintillator and SiPM modules

Requirements:

- Radiation tolerance;
- Calorimetric energy measurement;
- Fine imaging spatial **granularity**;
- Precise timing for showers.



First vertical slice detecting particles

Hexaboard testing

DAQ System

Building blocks

Layer 3 - 60 degree cassettes

Low density silicon **modules** :
300 µm or 200 µm thick
High density silicon **modules** :
120 µm thick

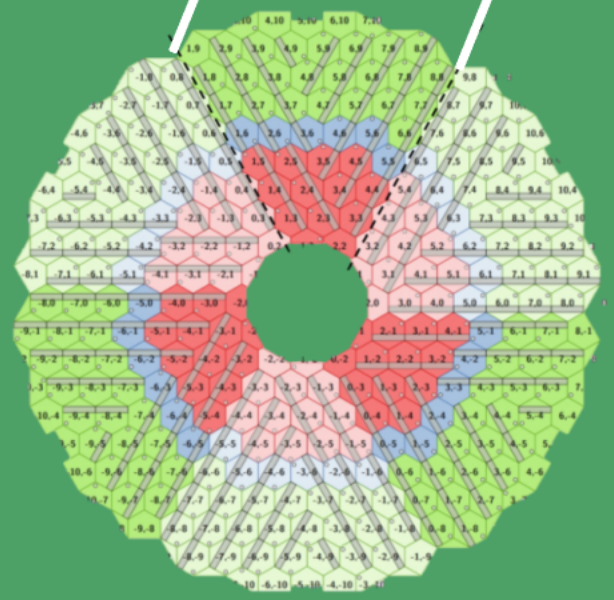
Sensor-PCB ('Hexaboard')
- Read-out (HGCROC*) of sensor cells + bias supply
- Connects to motherboard for data transfer

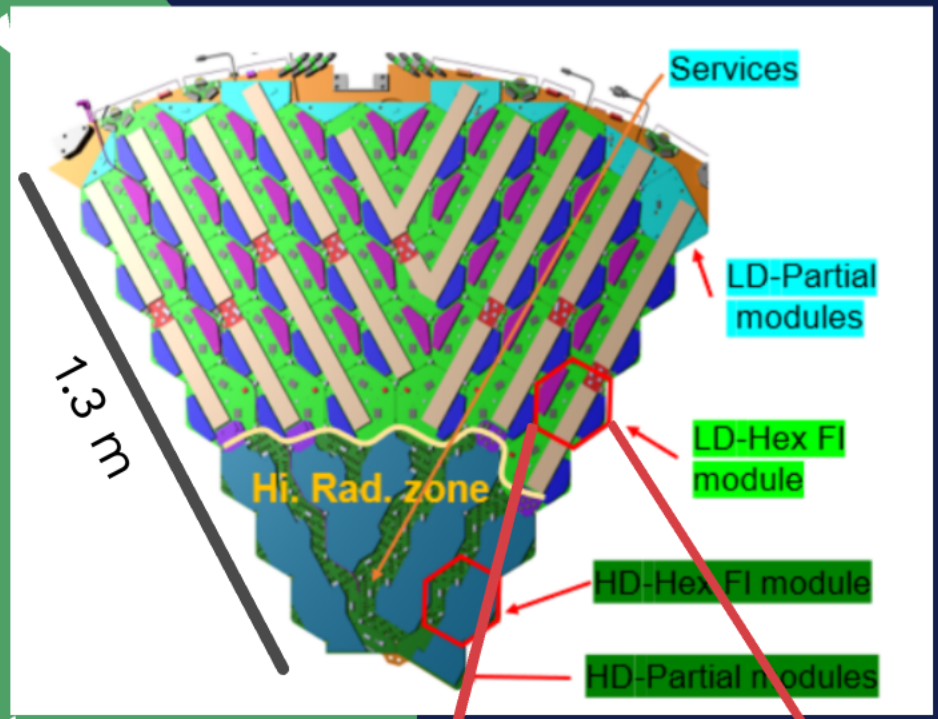
Silicon sensor

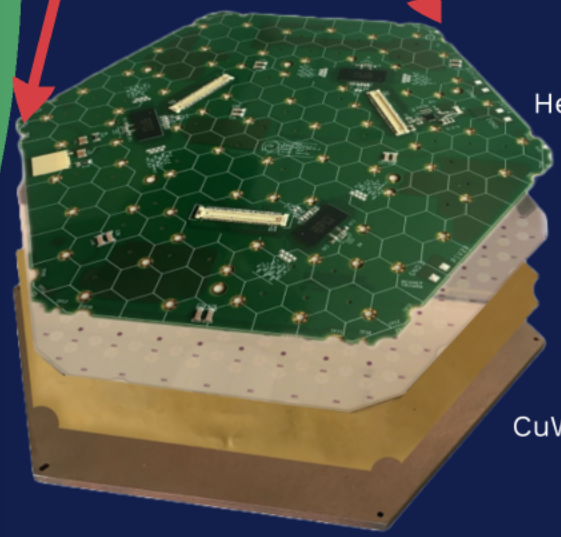
Kapton sheet
- Insulate from baseplate + bias supply to sensor back side

Baseplate
- Rigidity, contributes to showering material

*HGCROC: high granularity calorimeter read out chips

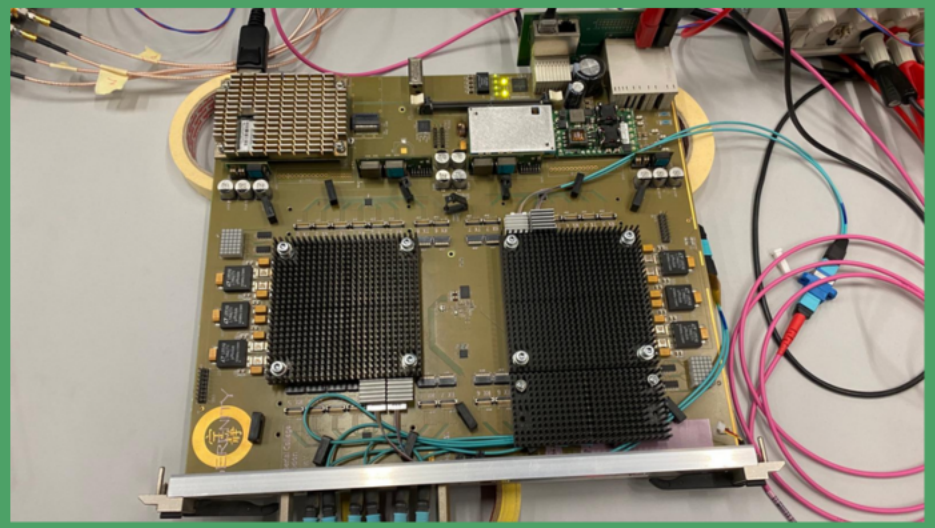






First vertical slice detecting particles

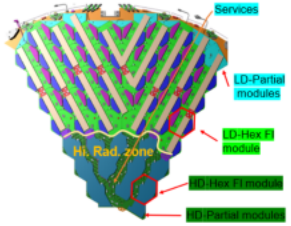
Backend: Serenity board

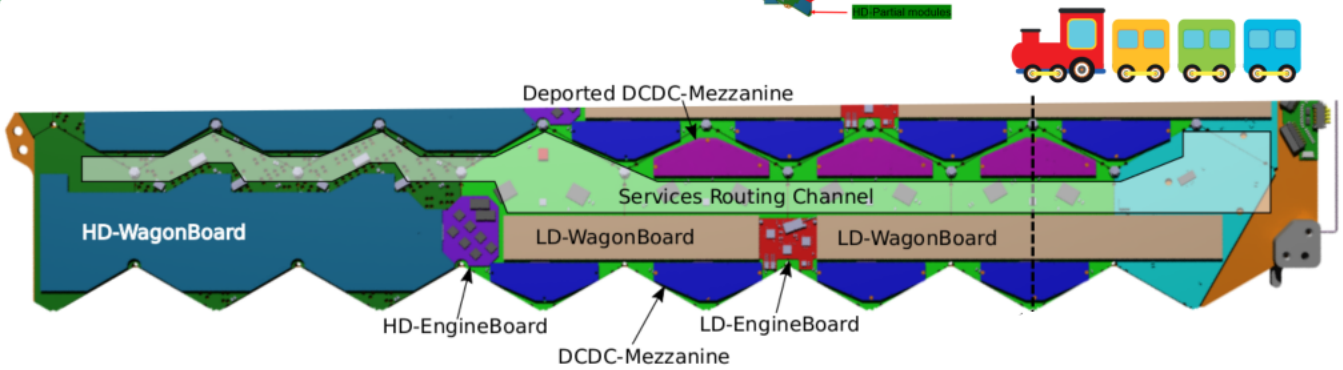


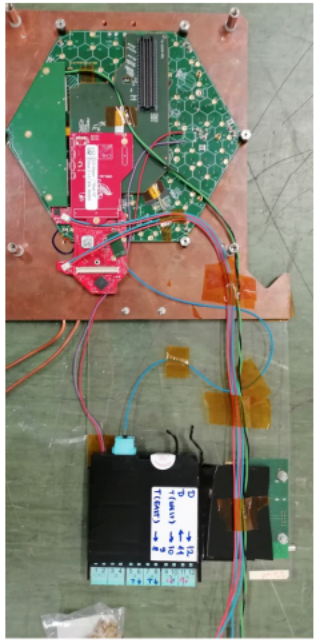
Frontend:

- Engines and wagons, which are connected to 5 hexaboards via an interposer.
- This interposer connects to an FPGA that emulates the ECON-D*

ROCs → Unicorn → ECON emulator ZCU → Unicorn Hexaboard → Wagon → Engine → Serenity

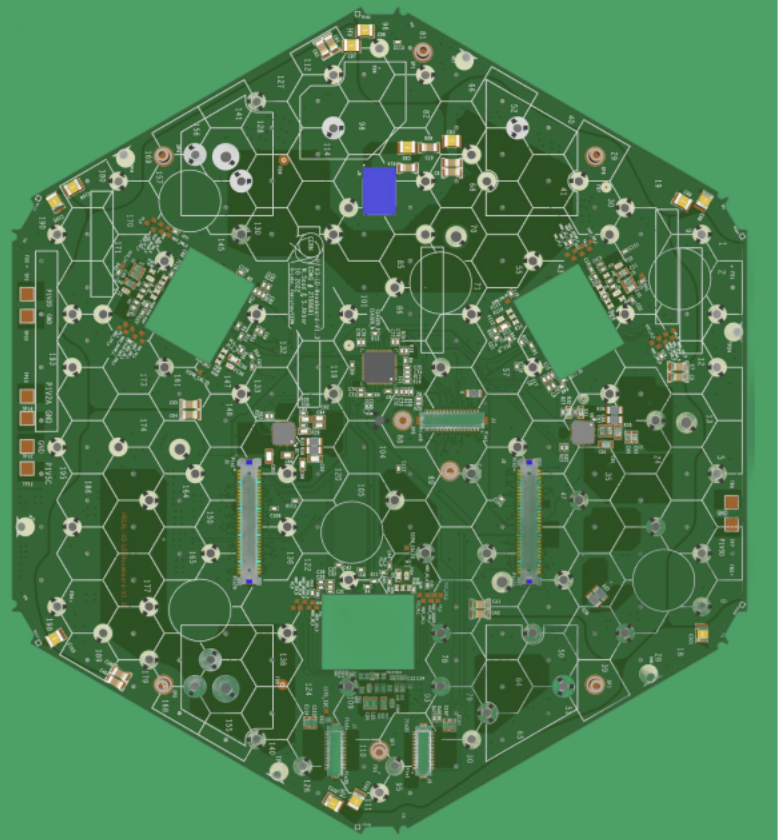




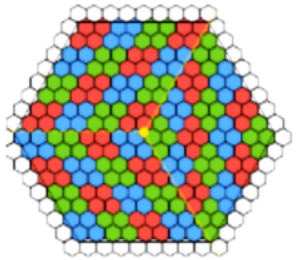


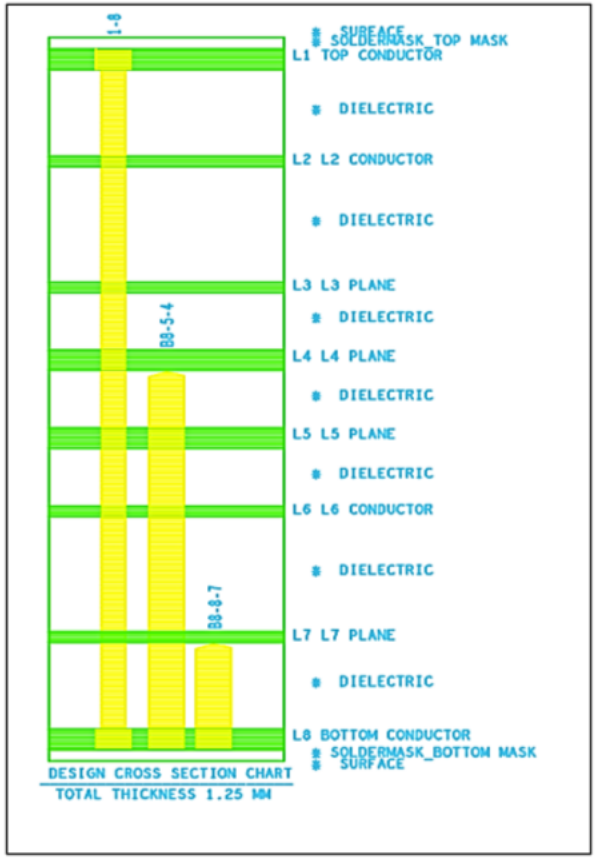
*ECON-D- elink concentrator daq

Hexaboard



Interfaces:
Slow and fast controls
Data concentrator board
DCDC Module
ASICS:
3x HGCROC for readout
72 DAQ channels per ROC
(LD - 64 channels readout)
TPG*: 12 super cells with 4 trigger cells each





V3-LD-Hexaboard Stack-up

*TPG- trigger primitive generator

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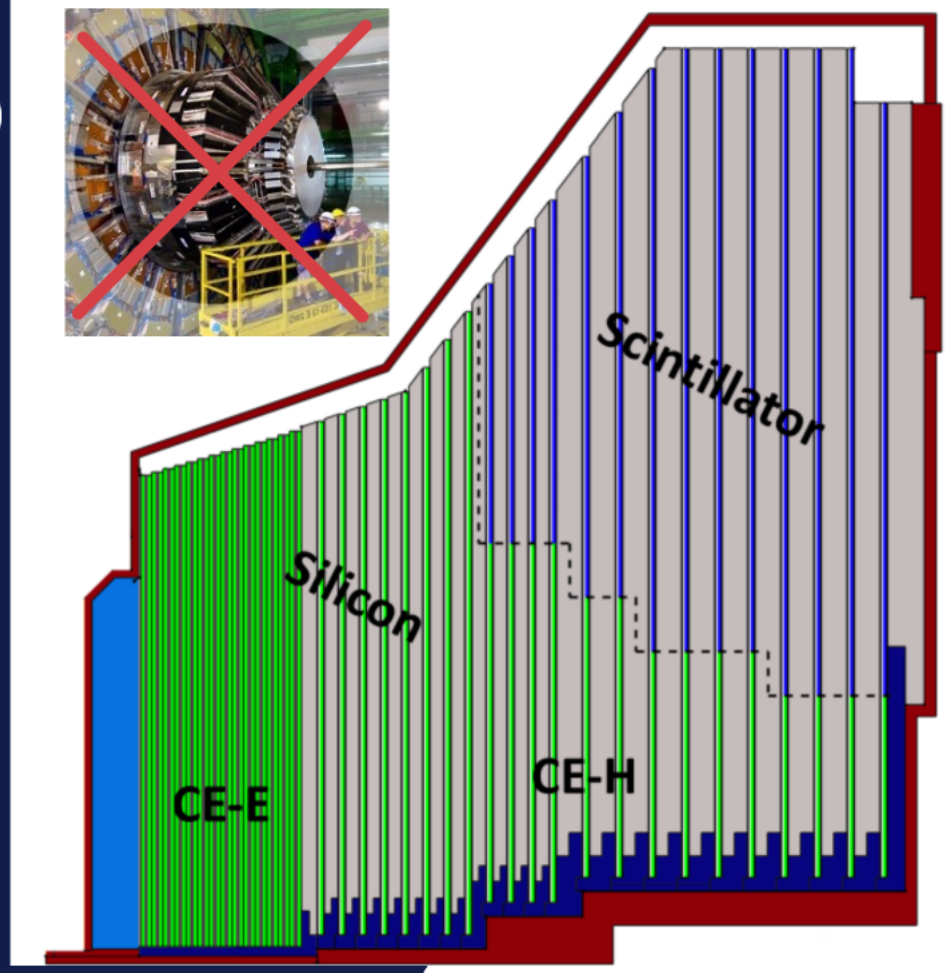

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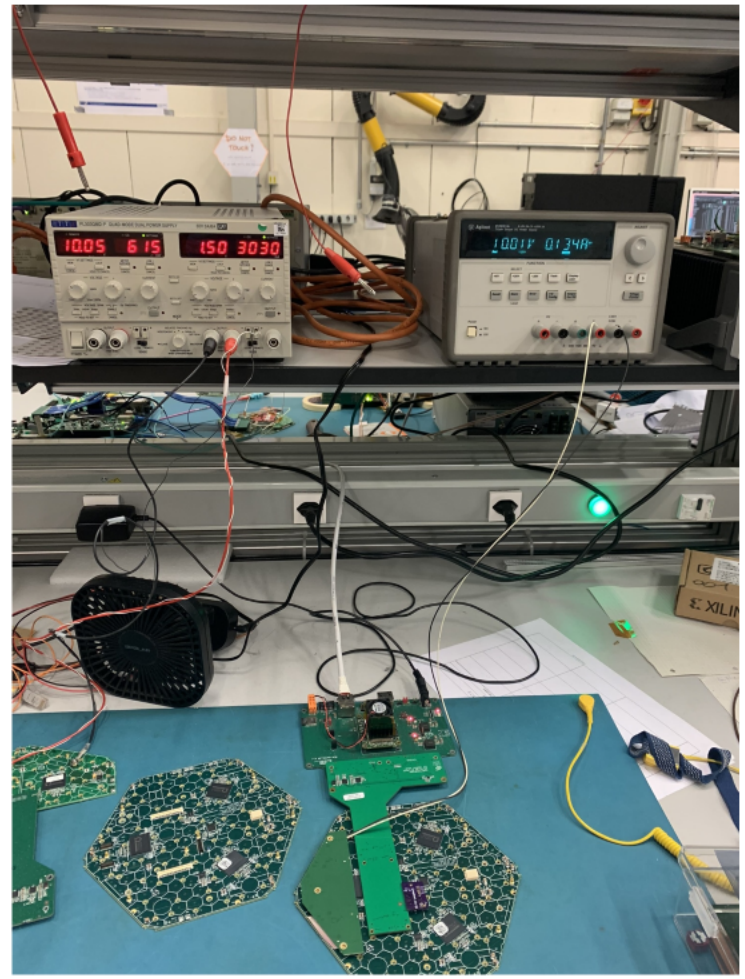
Hexaboard testing

DAQ System

LD Hexaboard testing - Performance evaluation

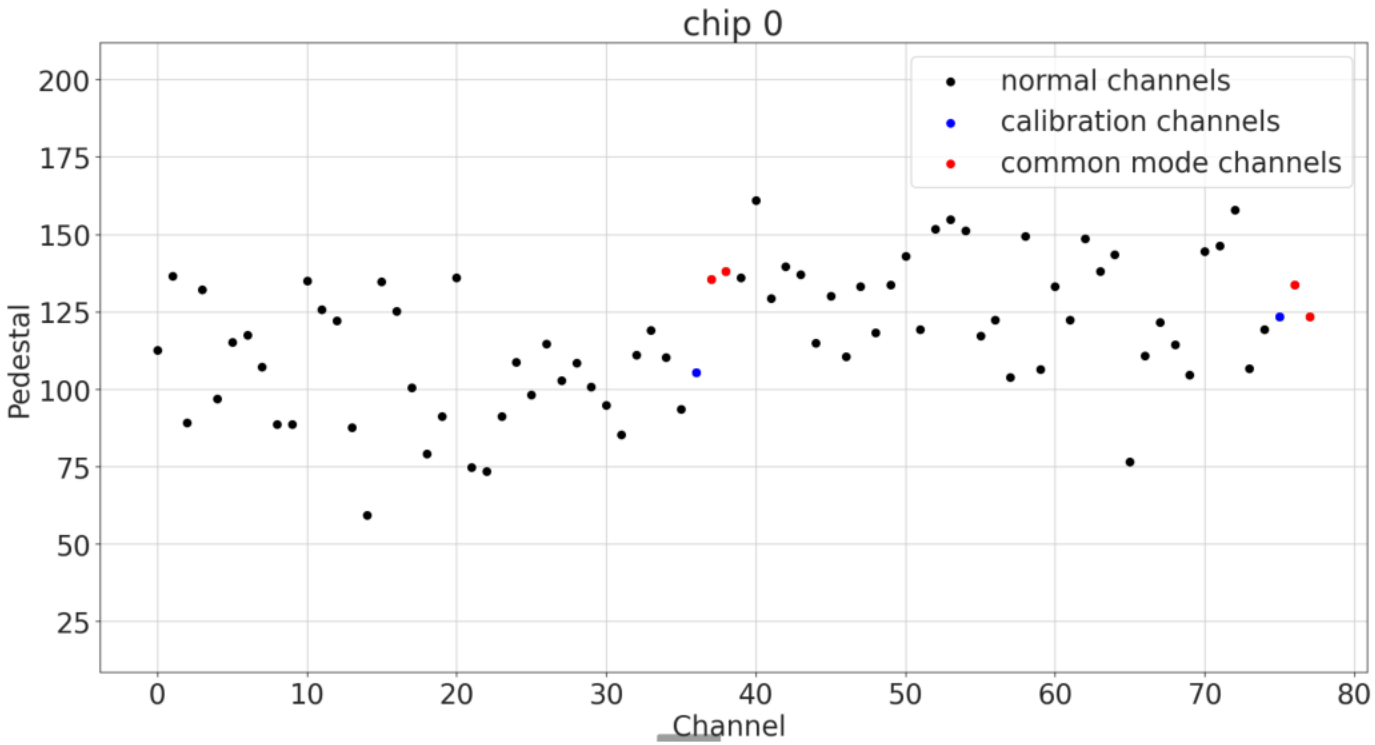
- Optical inspection
- **Testing Asics HGCROCs:**
  - **Noise and pedestal**
  - **Digital modulation: Δ Pedestal**
  - **Phase scan**
  - **daq_tpg_checker**
  - **Power before and after configuration file**
- Thermal cycling

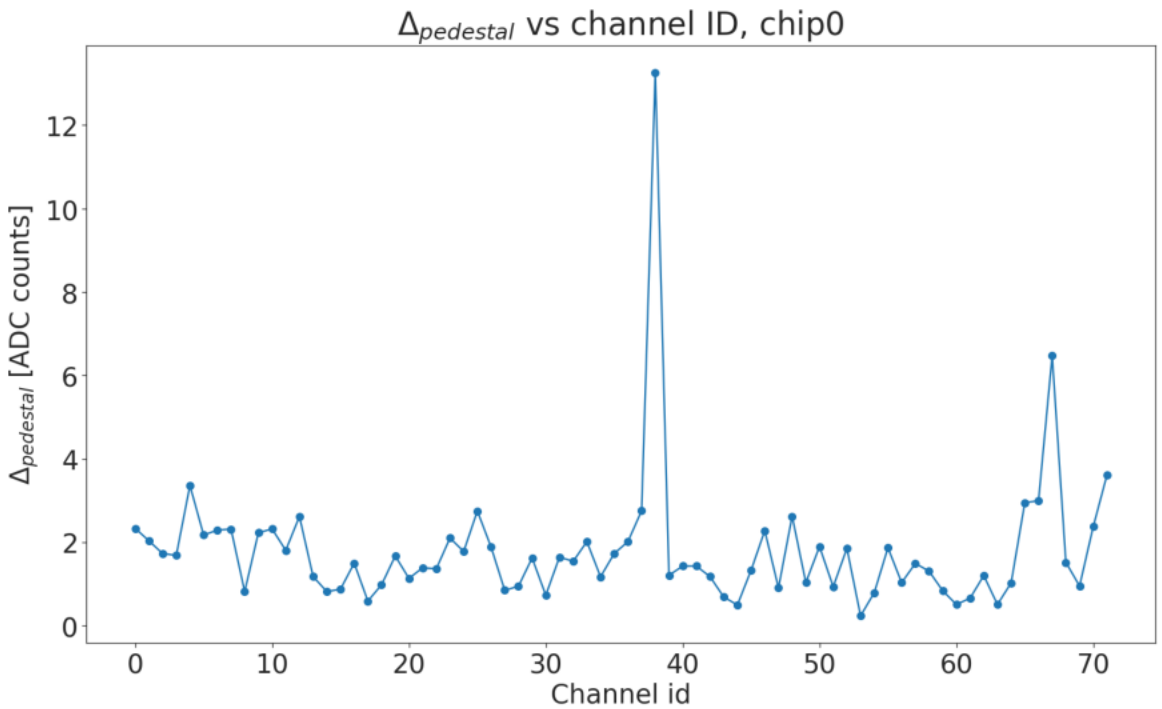


Pedestal and delta pedestal

Noise characterisation

Pedestal and ΔPedestal

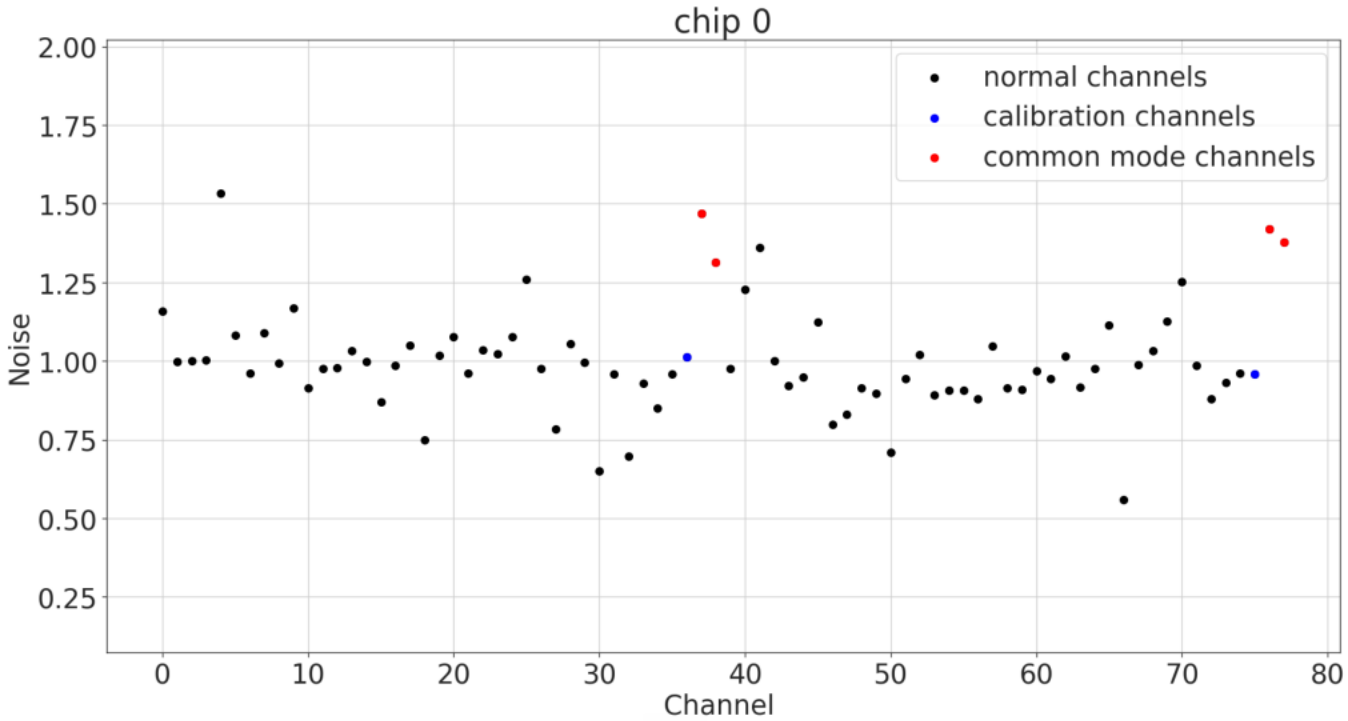


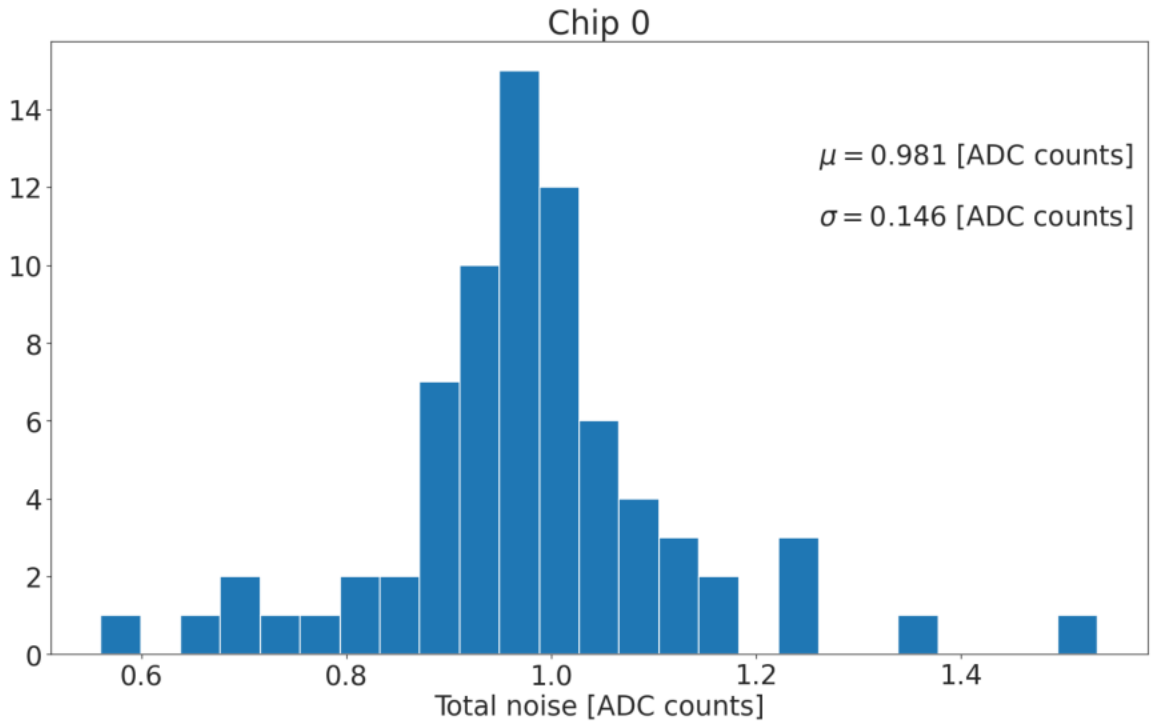


Pedestal: effective offset

Δ Pedestal : maximum difference of pedestals for varying ADC sampling phase

Noise characterisation of hexaboard without sensor





Noise: standard deviation of the pedestal distribution of each channel in ADC counts

Very good results

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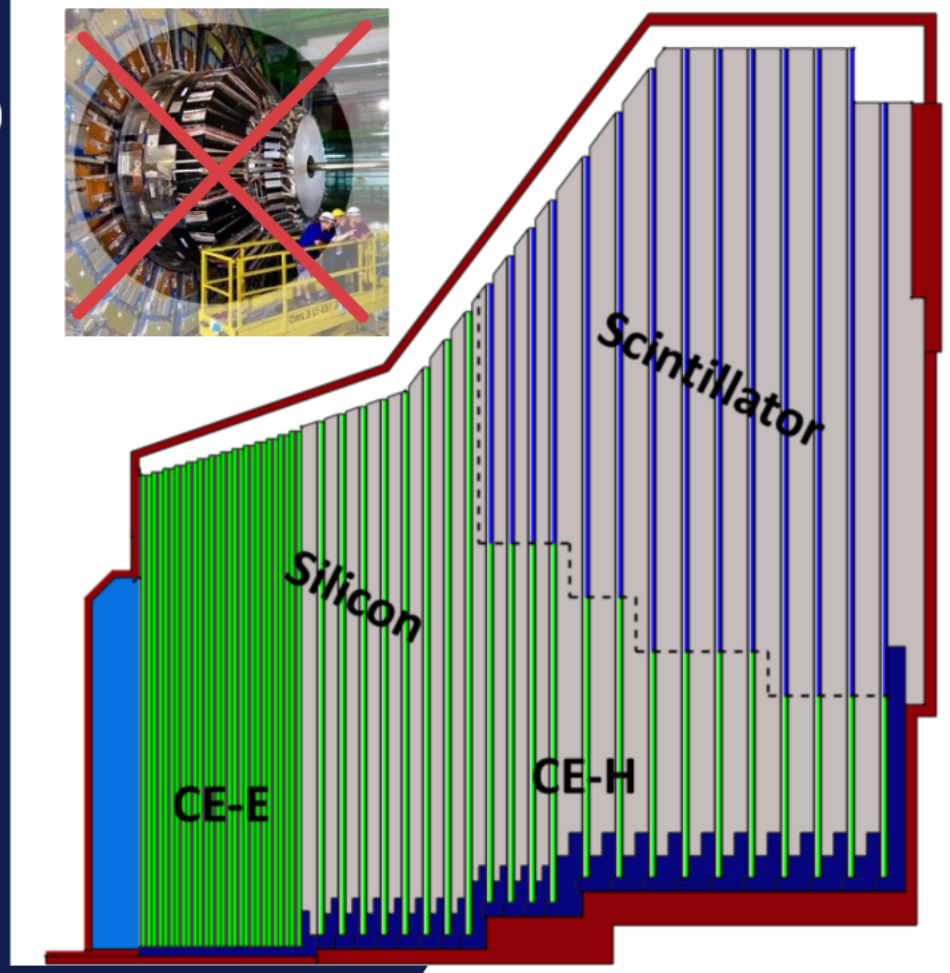

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Hexaboard testing

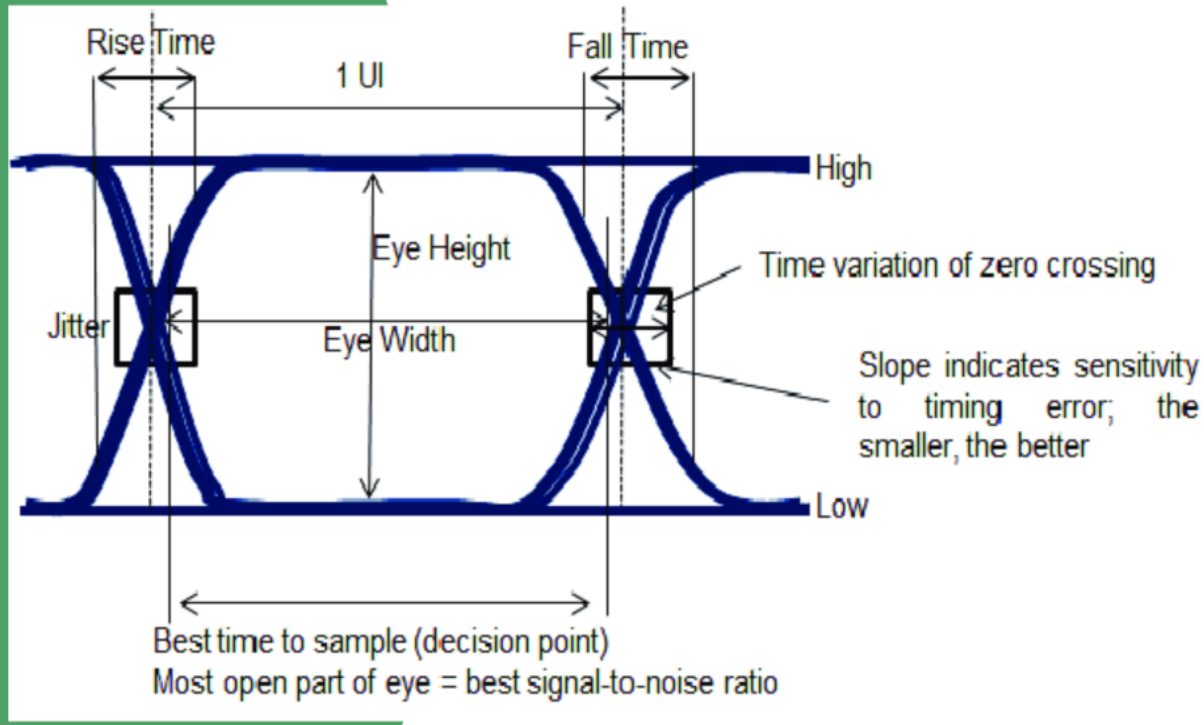
DAQ System

DAQ* System

ECON-D concentrator ASIC in production missing

FPGA Emulator: monitor signal integrity - Unicorn Board

Timing in the sampling phase: link alignment



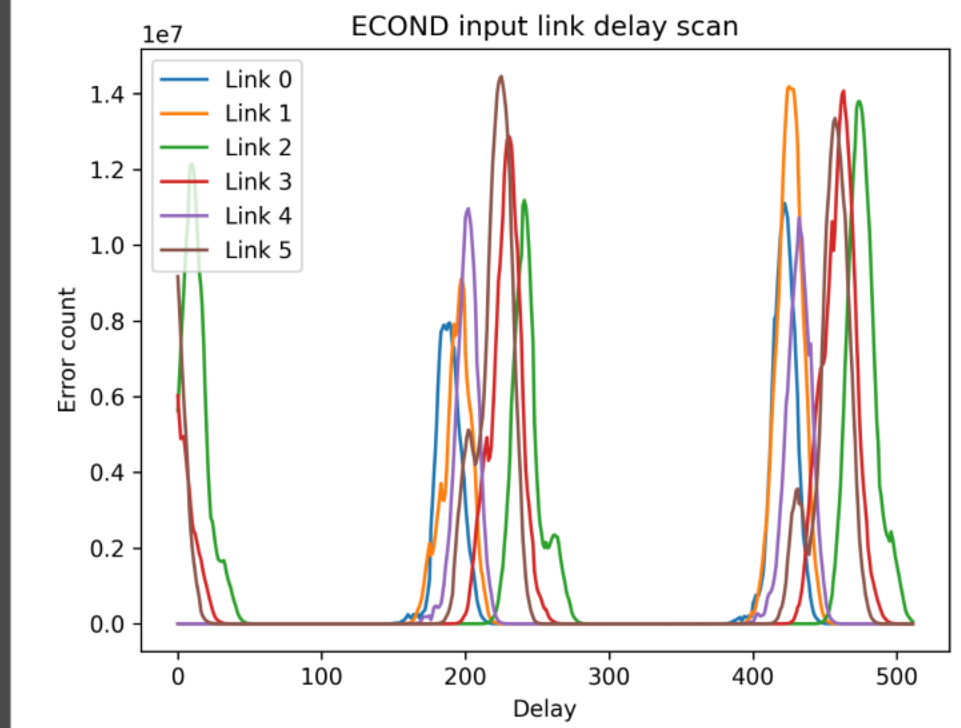
Sampling of links

DAQ System: Phase tracking in FPGA

FPGA needs to know at which time to sample the different links:
6 different links from the 3 ROC's

→ Scan for the most optimal delay to use

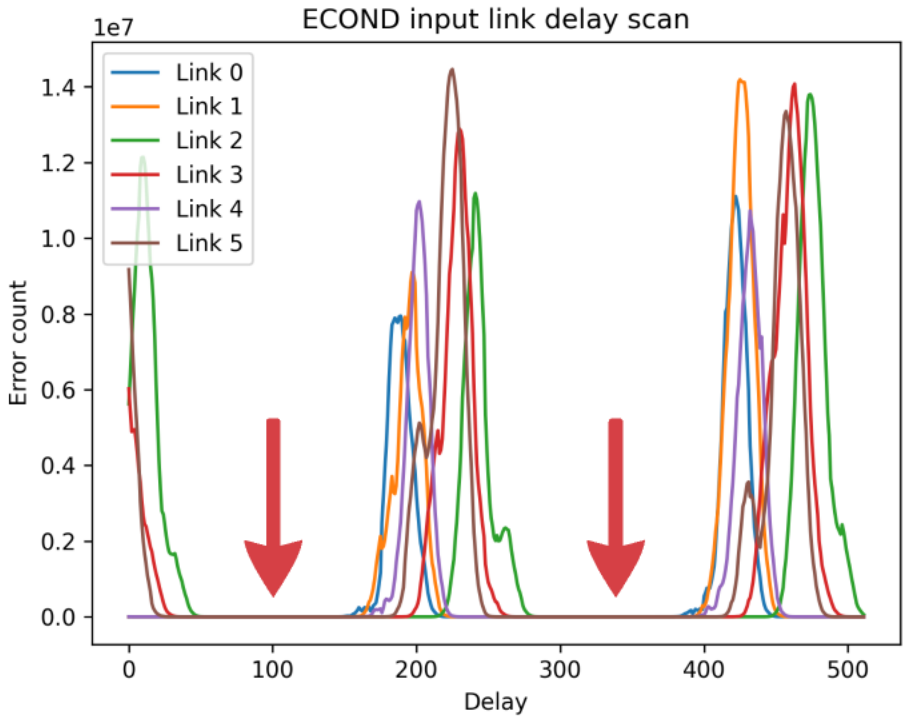
→ Error count vs delay at which to sample



DAQ System: Phase tracking in FPGA

FPGA needs to know at which time to sample the different links:
6 different links from the 3 ROC's

- → Scan for the most optimal delay to use
  - → Error count vs delay at which to sample
    - → Two possible eyes to choose from



Future work

Beam tests (August and September)

Test of irradiated sensor modules in silicon lab

Cold box testing of hexaboards and sensors