Introduction to Electronics for Particle Physics Experiments

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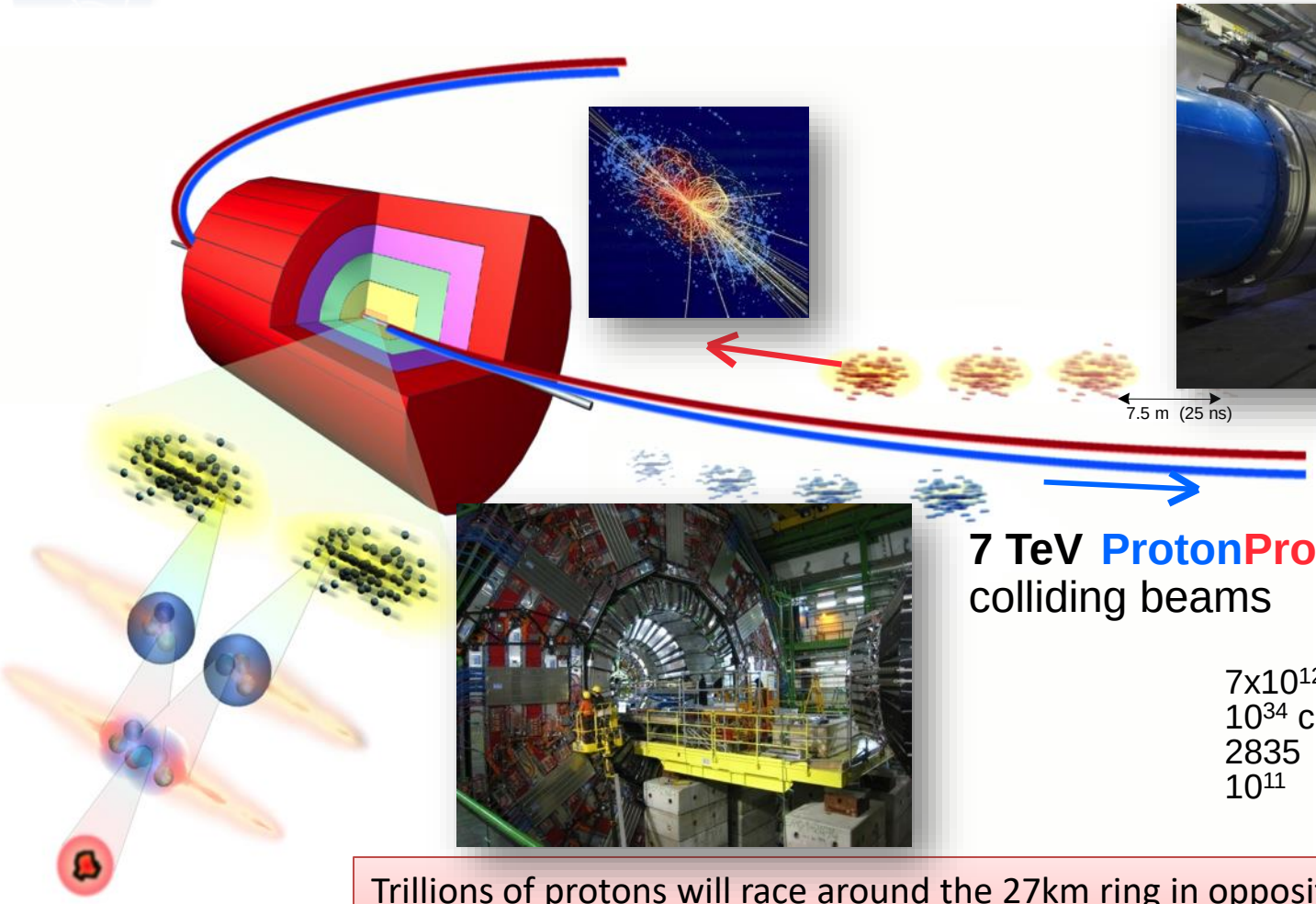
Electronics System for Experiments group
Microelectronics section

Welcome to CERN

- Research & Discovery
- Technology
- Collaboration
- Education & Training

The Large Hadron Collider

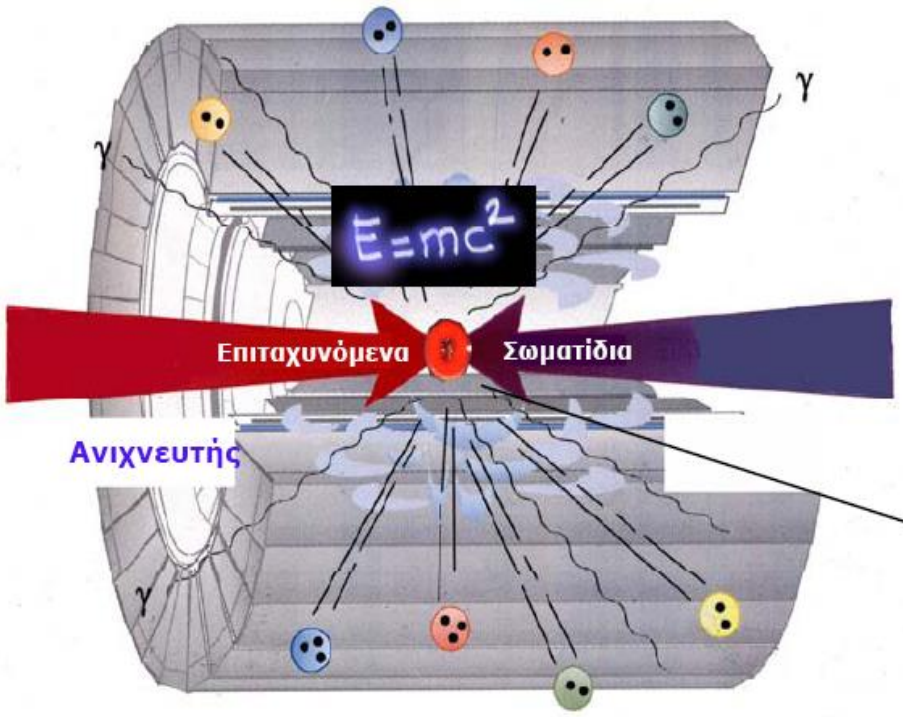


7 TeV ProtonProton
colliding beams

7×10^{12} eV	Beam Energy
10^{34} cm^{-2} s^{-1}	Luminosity
2835	Bunches/Beam
10^{11}	Protons/Bunch

Trillions of protons will race around the 27km ring in opposite directions over 11,000 times a second, travelling at 0.999999991 per cent the speed of light.

Μέθοδοι της Σωματιδιακής Φυσικής



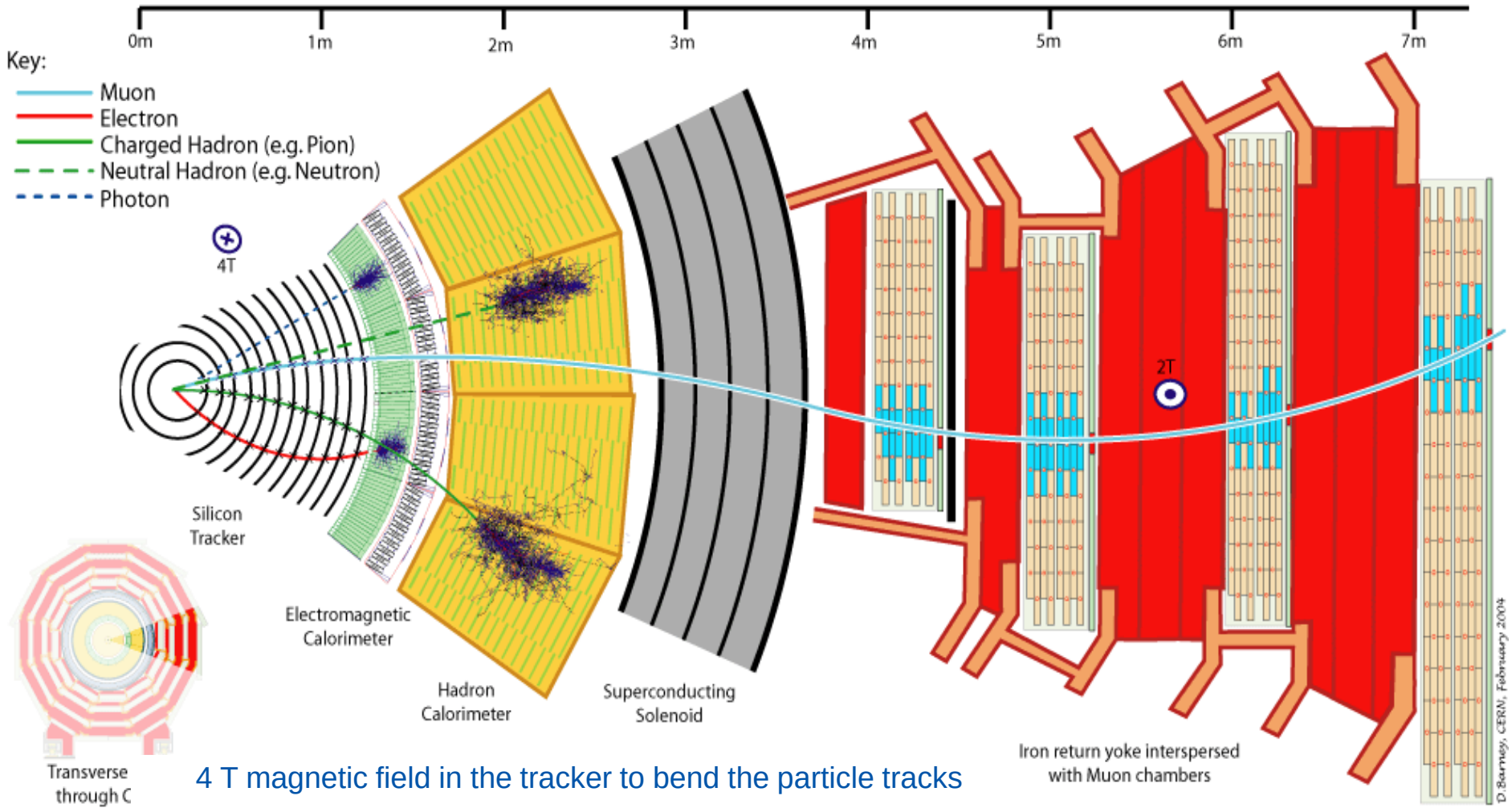
1) Συγκέντρωση ενέργειας στα σωματίδια (**επιταχυντής**)

2) **Σύγκρουση** σωματιδίων (δημιουργία συνθηκών ανάλογων του Big Bang)

3) Αναγνώριση παραγόμενων σωματιδίων από τον **Ανιχνευτή** (έρευνα για νέα φαινόμενα)

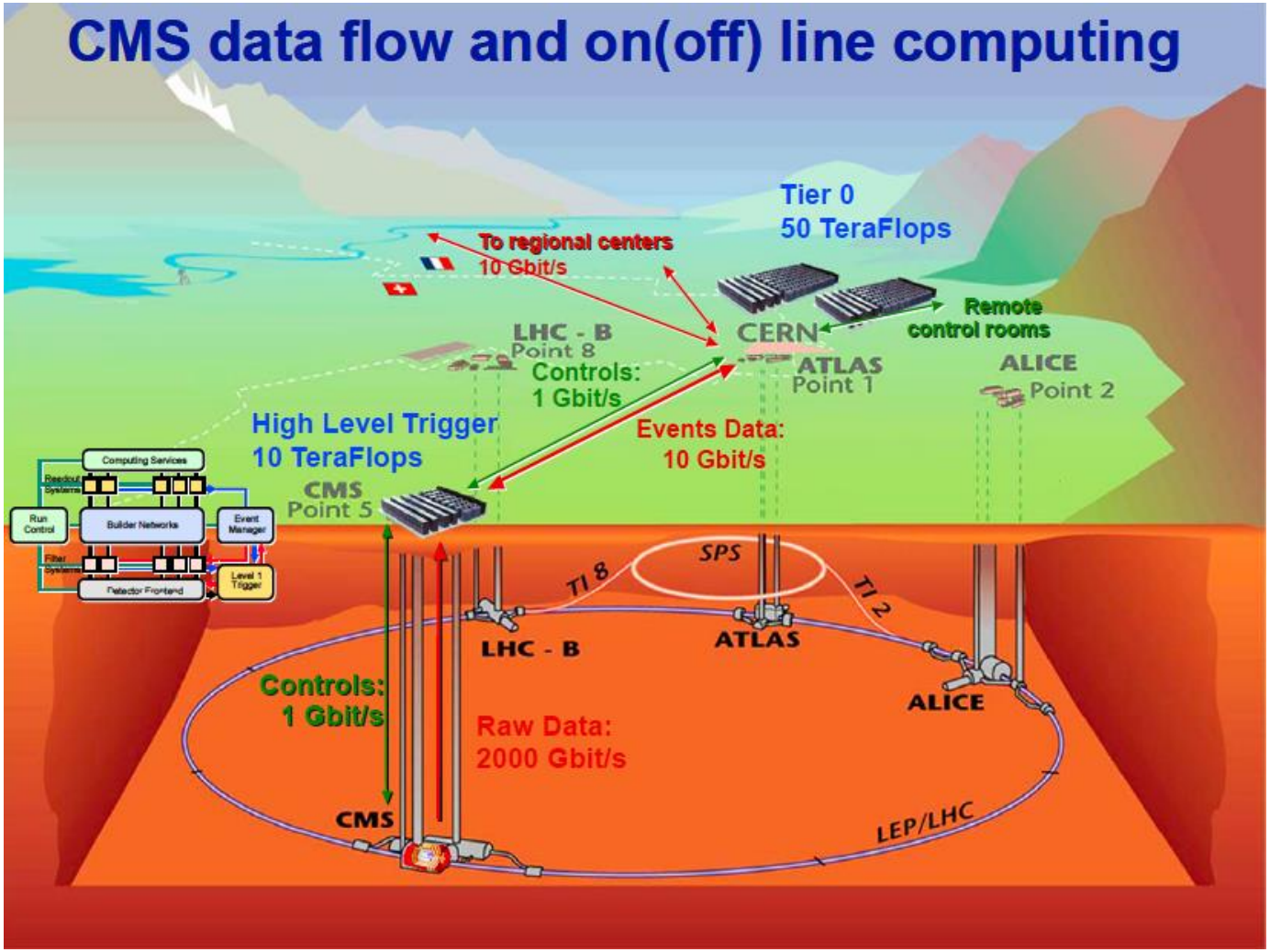
- Τα Σωματίδια συγκρούονται με ταχύτητες παραπλήσιες με αυτή του φωτός με αποτέλεσμα την παραγωγή νέων σωματιδίων. Η διαδικασία αυτή δίνει πληροφορίες για τους μηχανισμούς αλληλεπίδρασης των σωματιδίων και και τους θεμελιώδης φυσικούς νόμους που τα διέπουν.

Ανίχνευση Σωματίων



4 T magnetic field in the tracker to bend the particle tracks

The flow of Physics data at LHC



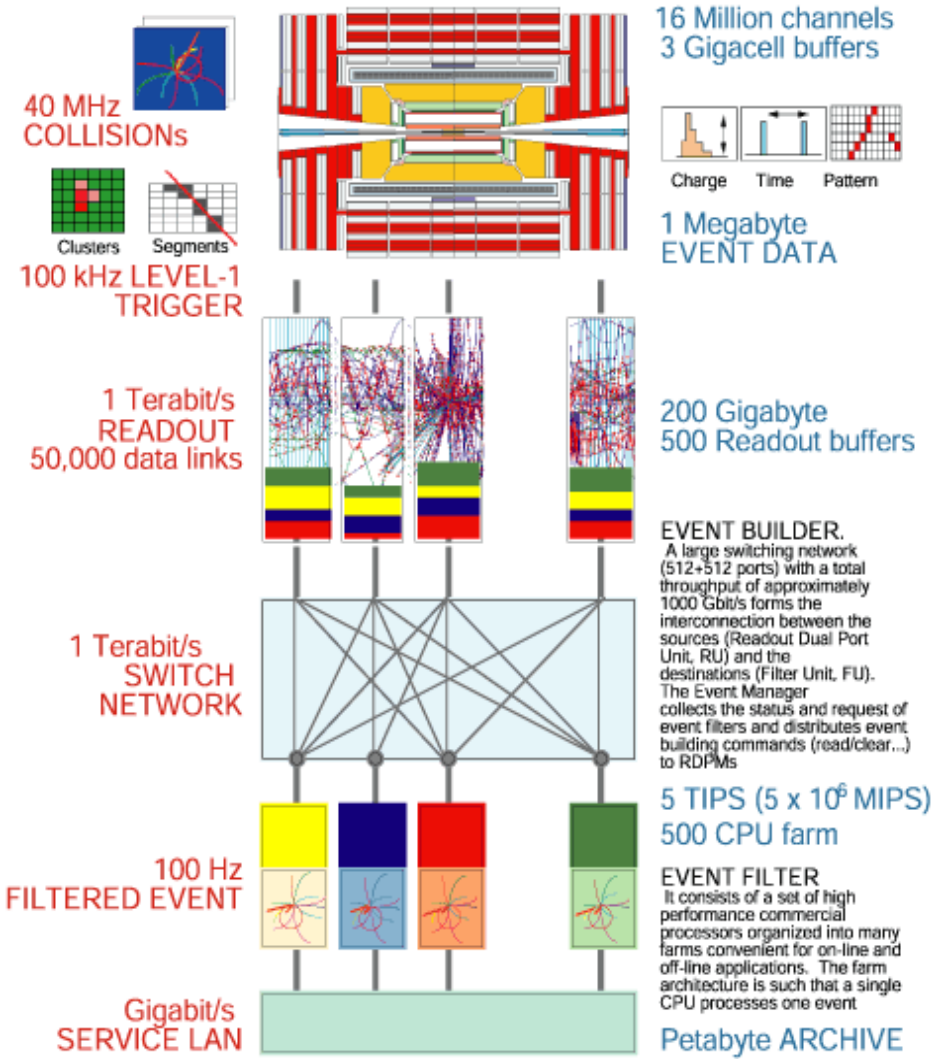
Συλλογή & Επεξεργασία Δεδομένων

- $40*10^6$ φωτογραφίες το δευτερόλεπτο
- 20 συγκρούσεις ανά φωτογραφία

- Το πρώτο φιλτράρισμα των μετρήσεων γίνεται στους ανιχνευτές δίνοντας $100*10^3$ φωτογραφίες ανά δευτερόλεπτο

- Το δεύτερο φιλτράρισμα των μετρήσεων γίνεται από συστοιχίες υπολογιστών δίνοντας 1 φωτογραφία ανά δευτερόλεπτο για εγγραφή και μετέπειτα ανάλυση

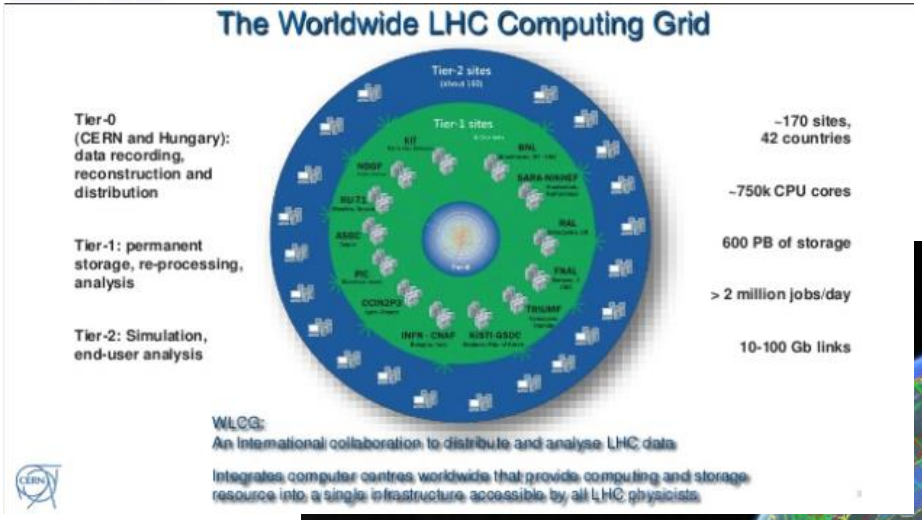
- Τα πειράματα του LHC παράγουν 10-15 Petabytes δεδομένων κάθε χρόνο (20 εκατομμύρια CDs!)
- Για την ανάλυση των δεδομένων χρειάζεται η υπολογιστική ισχύς που αντιστοιχεί σε ~100,000 γρήγορους μοντέρνους επεξεργαστές.

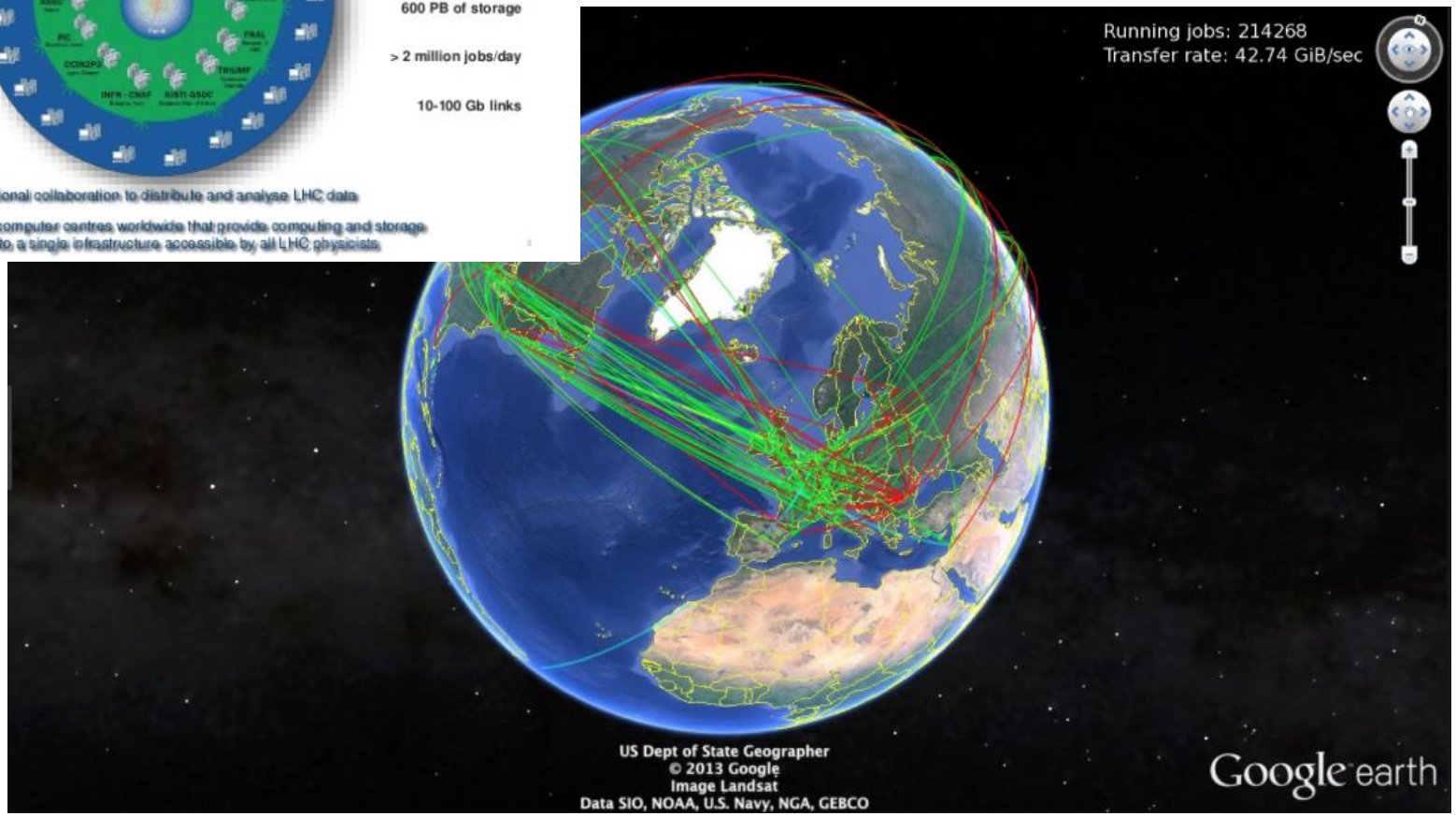


Υπολογιστικό κέντρο CERN

- 20,000 PCs

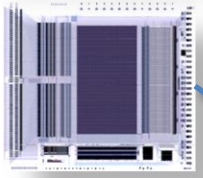
Παγκόσμιο Υπολογιστικό Δίκτυο





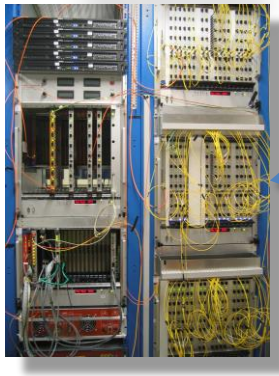
Microchips for Megastructures

On-detector ASIC

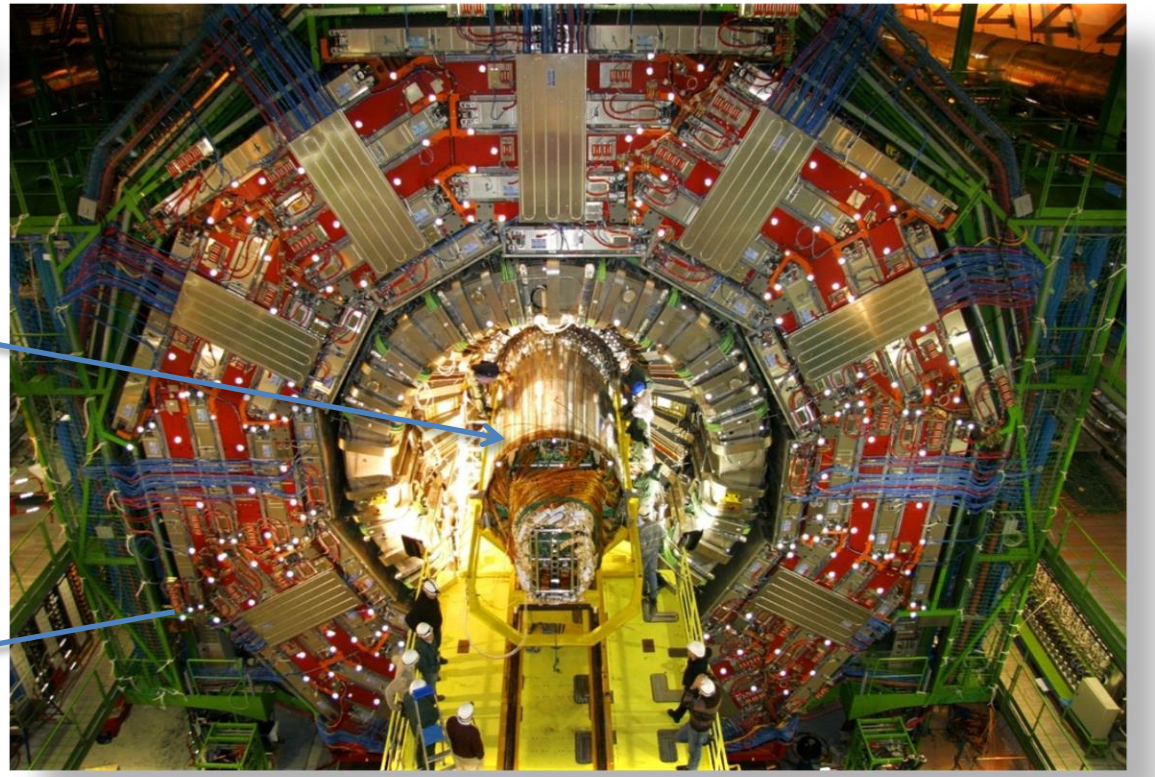


Silicon Tracker Hybrid

Off-detector electronics



CMS experiment at the LHC accelerator at CERN

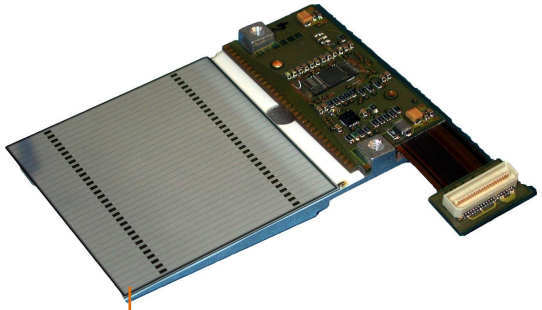


ASICs for High Energy Physics

- Highly customized functionalities
  - Unique Signal Processing techniques
  - High Resolution and High Dynamic range
- Very high number of Readout Channels
  - Low power consumption
- Intense Radiation Environment
  - TID (Total Ionizing Dose) of 500 Mrads up to 1 Grad
    - Space applications requirements: up to 200 Krads
  - SEE (Single Event Effects)
    - Particle fluence ~10^{15} cm^{-2} (inner tracker layers)

Silicon Strip Detector electronics

Silicon-strip detector



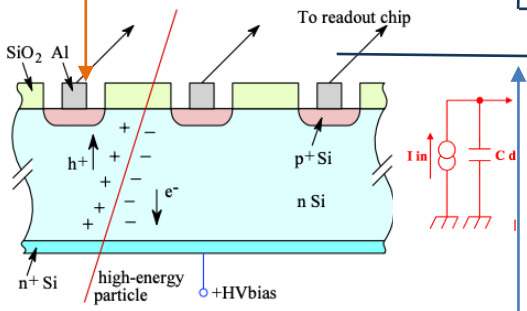
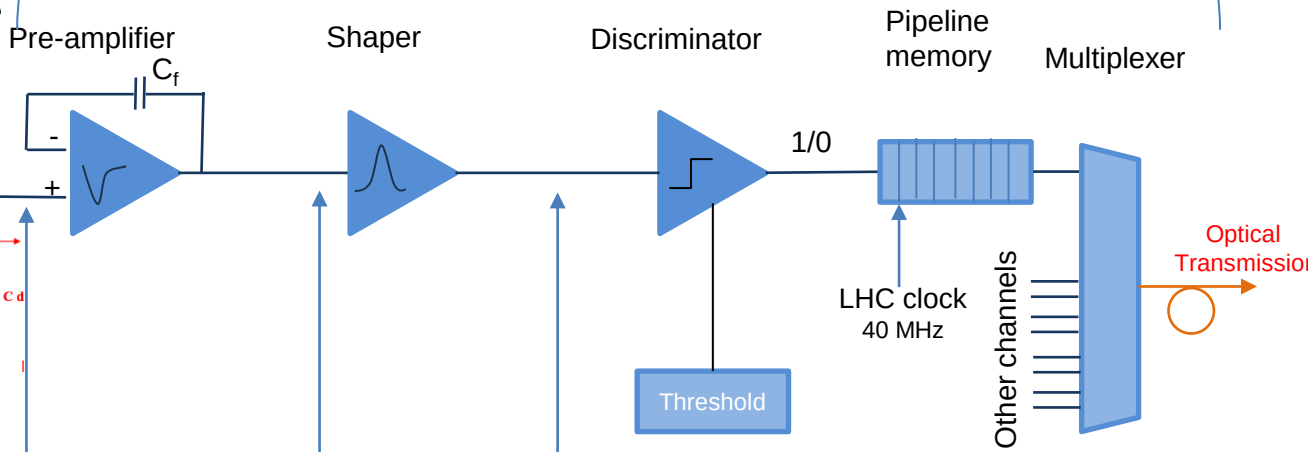
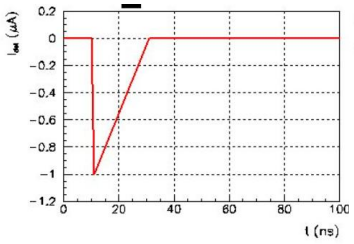


Fig.4: Schematic cross-section of a typical silicon strip detector.

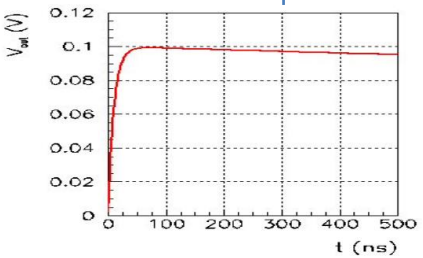
On-detector electronics

ASIC (Application Specific Integrated Circuit)

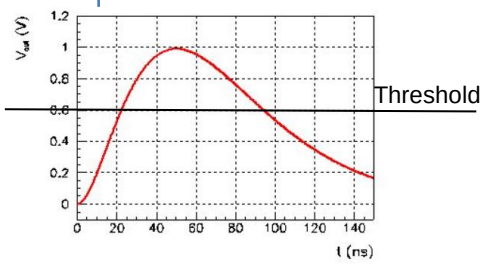




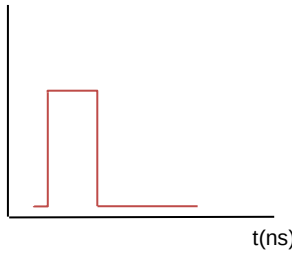
Very small signal (~fC)
Needs amplification



Charge-sensitive amplifier
$V = -Q/C_f$



Predefined signal shape
Noise reduction by optimizing useful bandwidth



Digitized signal (1/0)
Signal above a preset threshold

Readout of Silicon Strip Detectors

Silicon-strip detector

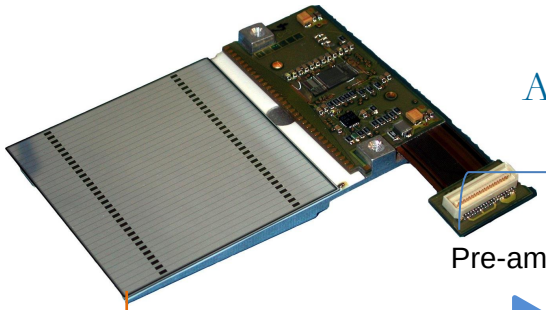
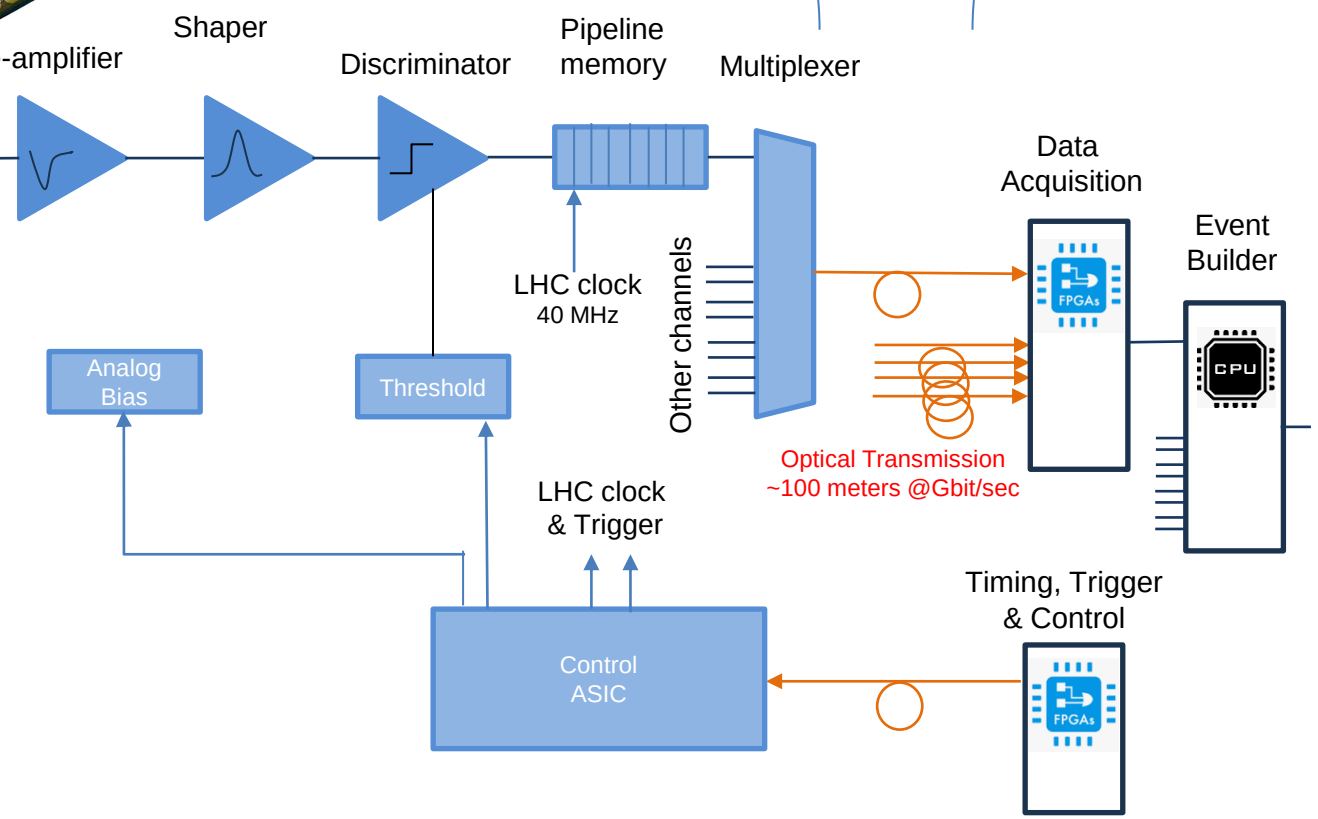


Fig.4: Schematic cross-section of a typical silicon strip detector.

On-detector electronics

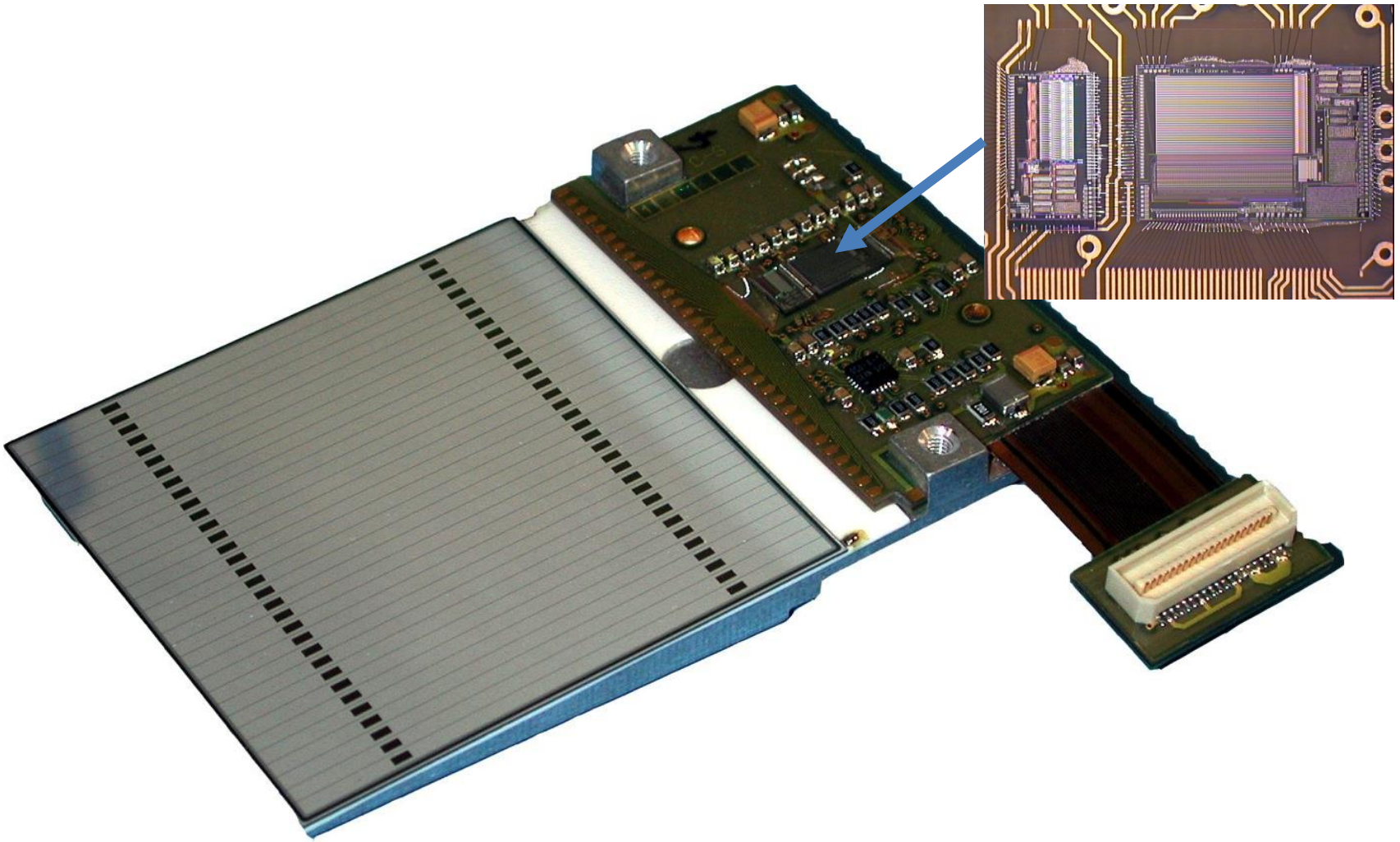
ASIC (Application Specific Integrated Circuit)

Off-detector electronics

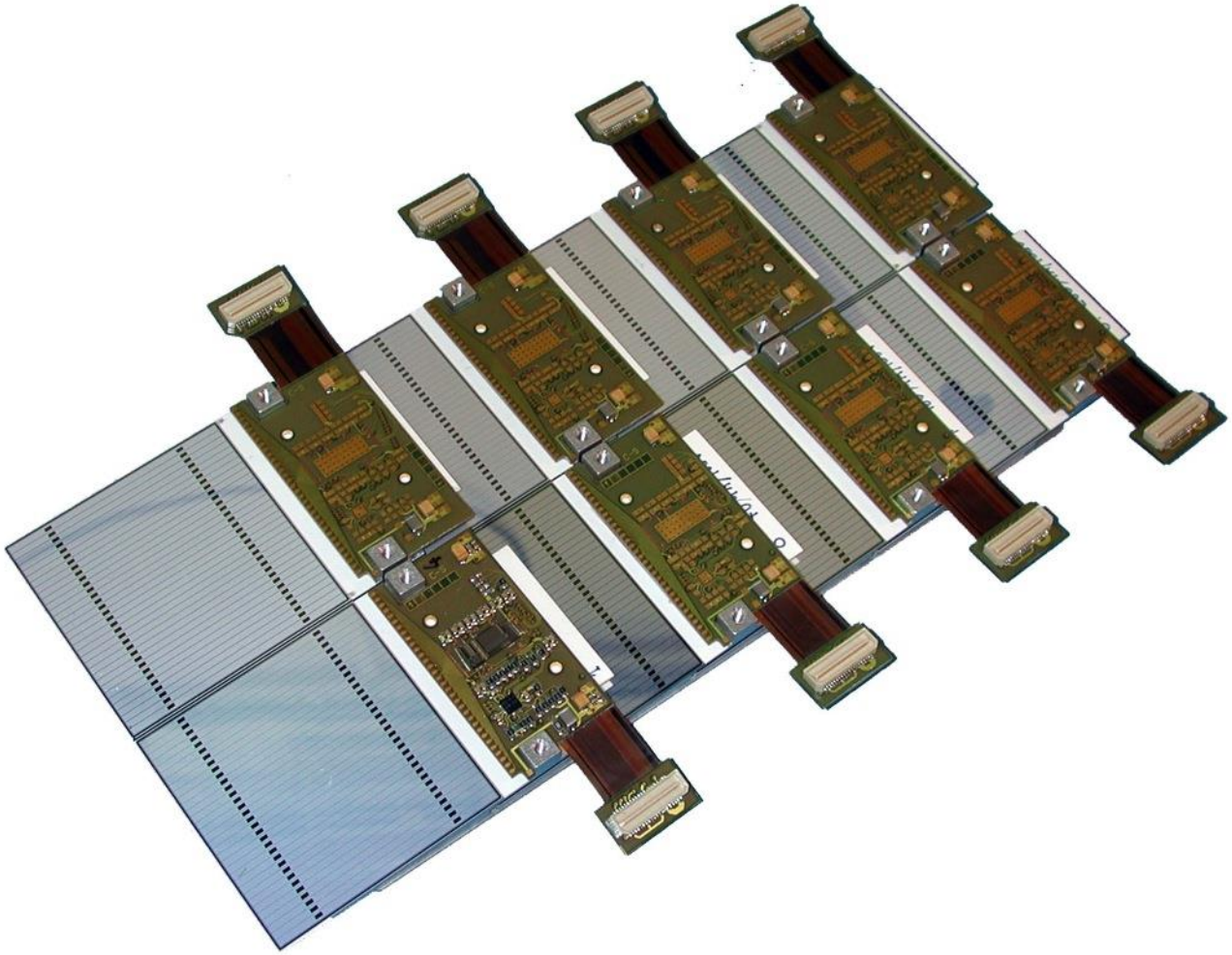


On-detector ASICs

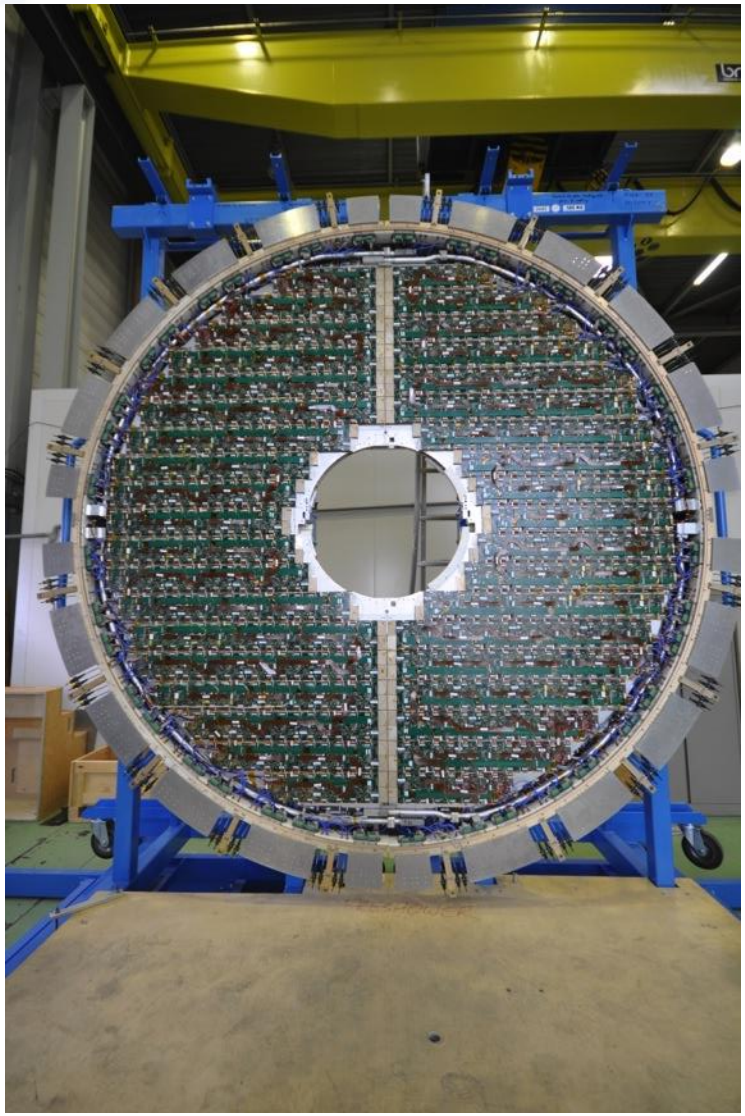
ASIC (Application Specific Integrated Circuits)



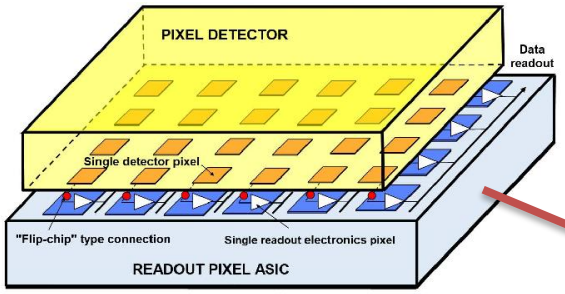
Sensor modules with ASICs

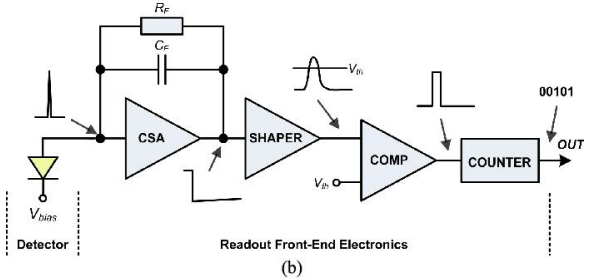


Detector Assembly

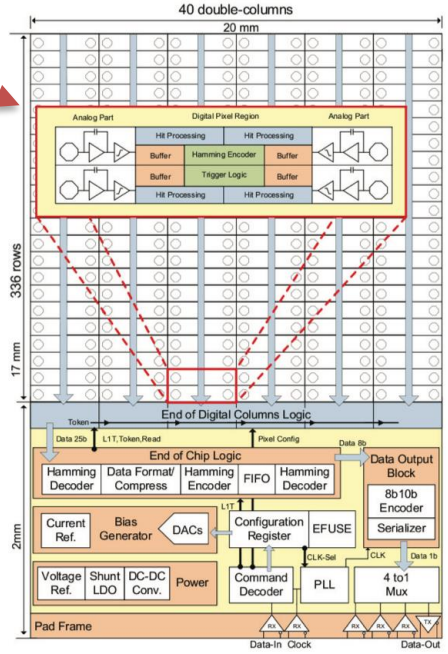


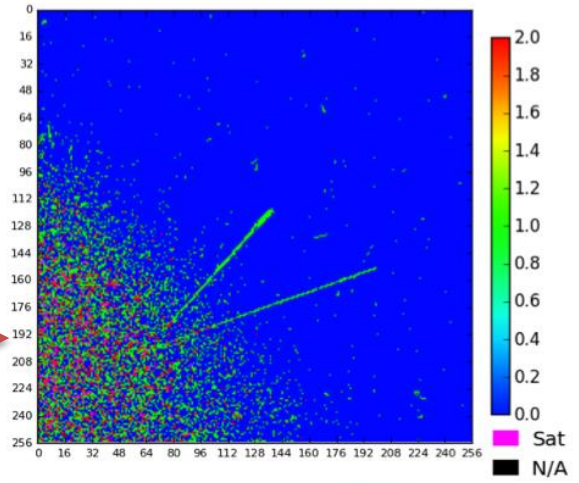
Pixel Detector electronics



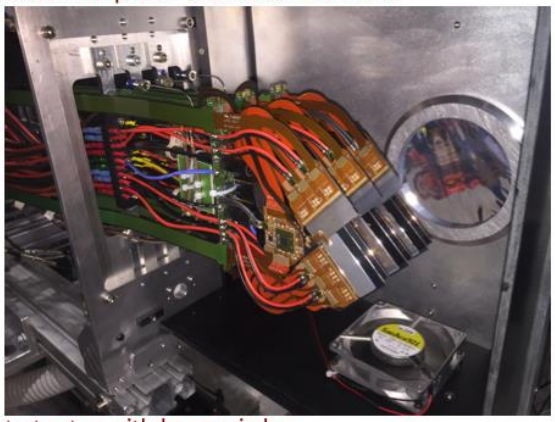


Velopix readout ASIC for the LHCb detector



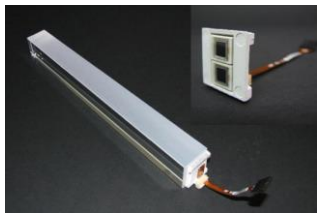


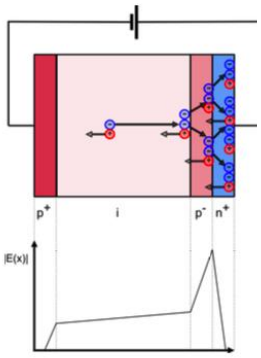
first data with proton beam over GWT link



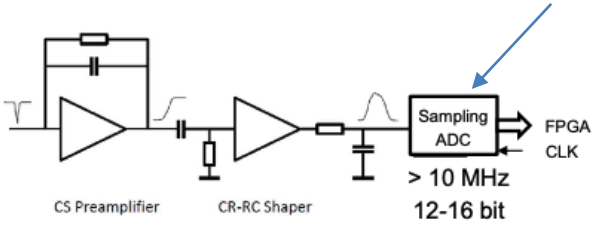
test setup with beam window

EM Calorimeter electronics



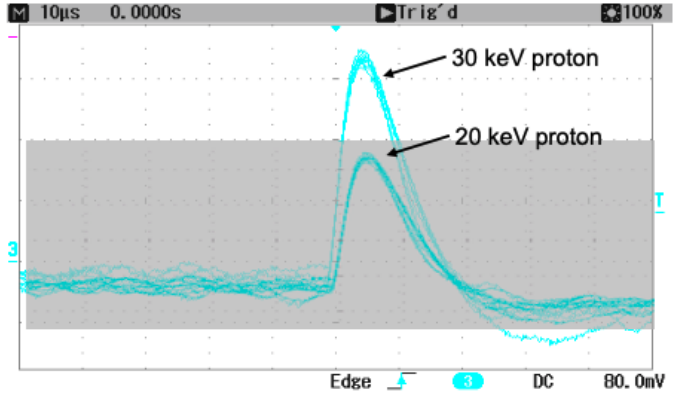


Analog to Digital Converter (ADC)



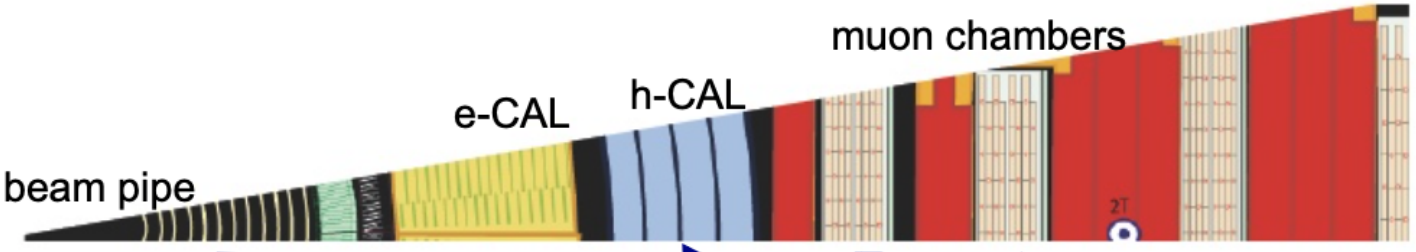
Created charge proportional to energy deposit
⇒ Amplitude measurement
⇒ Signal Time defines EVENT TIME

- Charge-sensitive (CS) preamplifier
- Shaping: CR differentiator and RC integrator



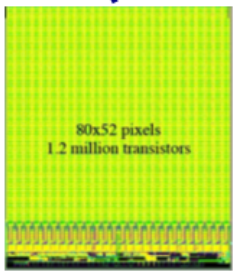
- Lead tungstate crystals
- Avalanche Photo-diodes
  Reverse-biased p-n junction
- Primary photoelectrons accelerated in electric field → avalanche
- Generated charge is proportional to deposited energy

Some examples of ASICs in CMS

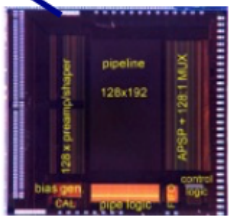


pixel detector

Si strip tracker



PSI46 pix det
16 800 chips
66 M segments
1 m² Si sensor



APV25 Si det
110 000 chips
9.3 M segments
198 m² Si sensor

QIE8 calorimeter
220 400 chips

MAD muon det
181 000 chips
25 000 m² gas-filled

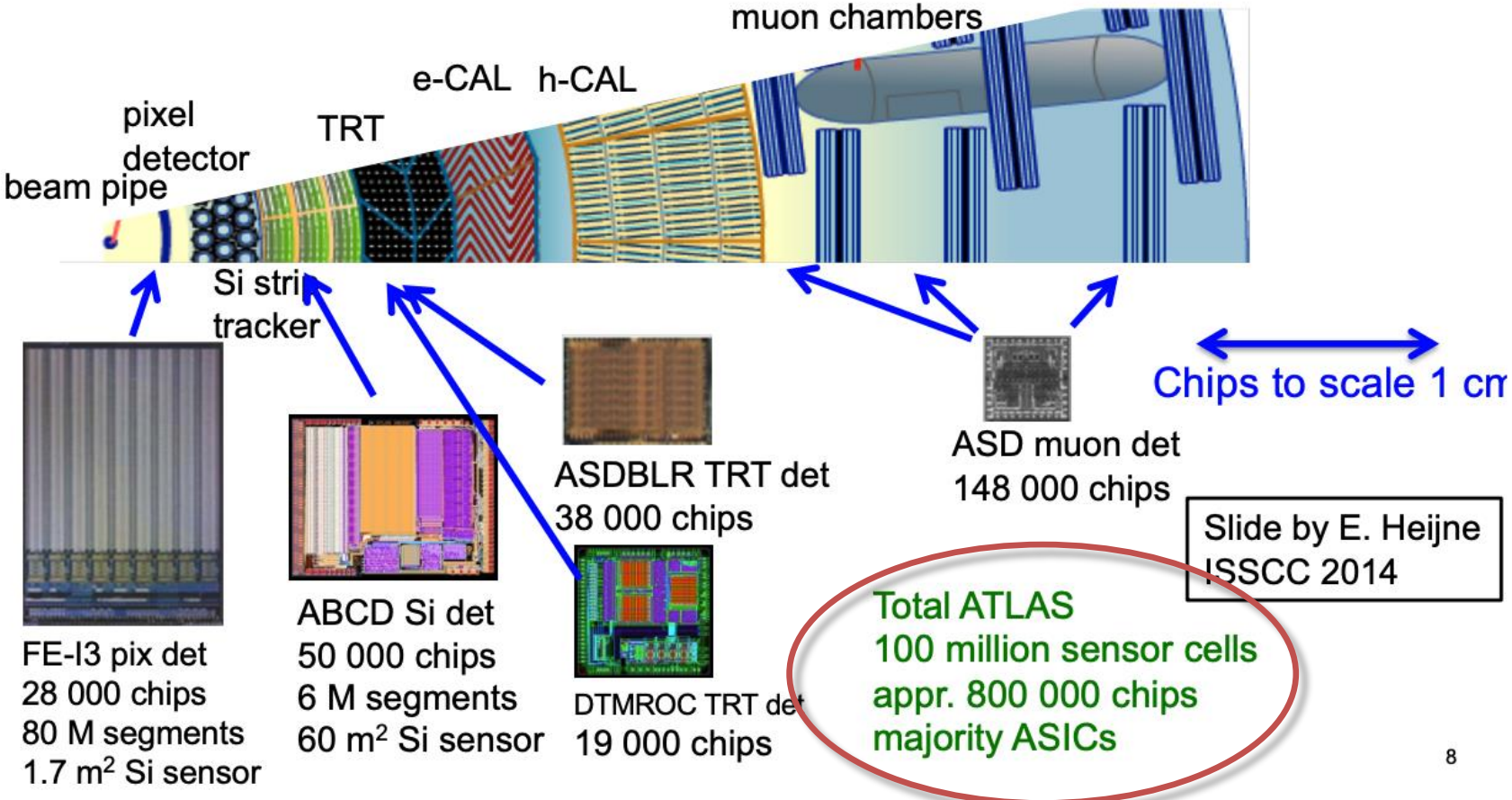
Chips to scale 1 cm

Slide by E. Heijne
ISSCC 2014

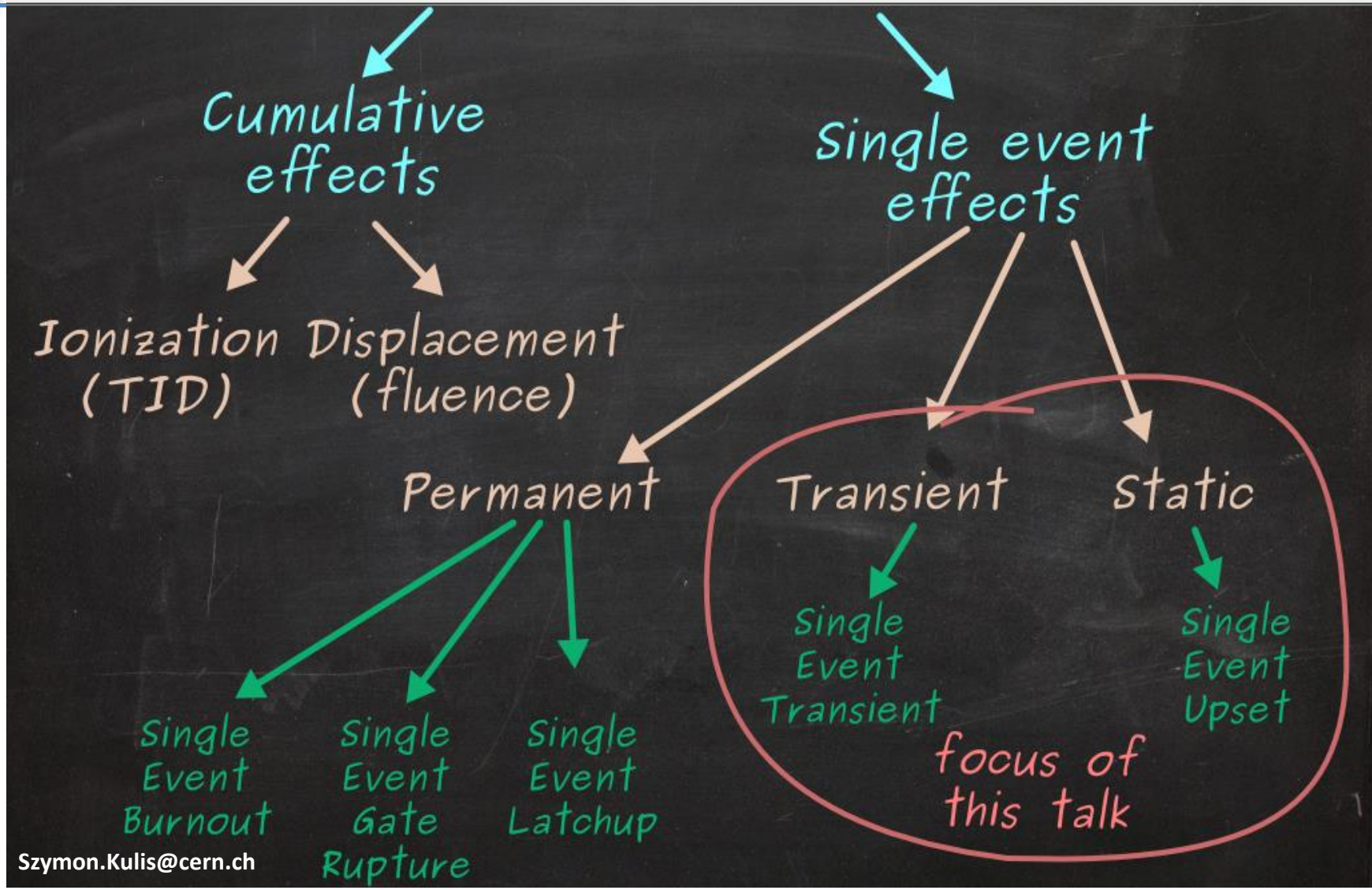
Total CMS
appr. 1 million chips
of which 700 000 ASICs

9

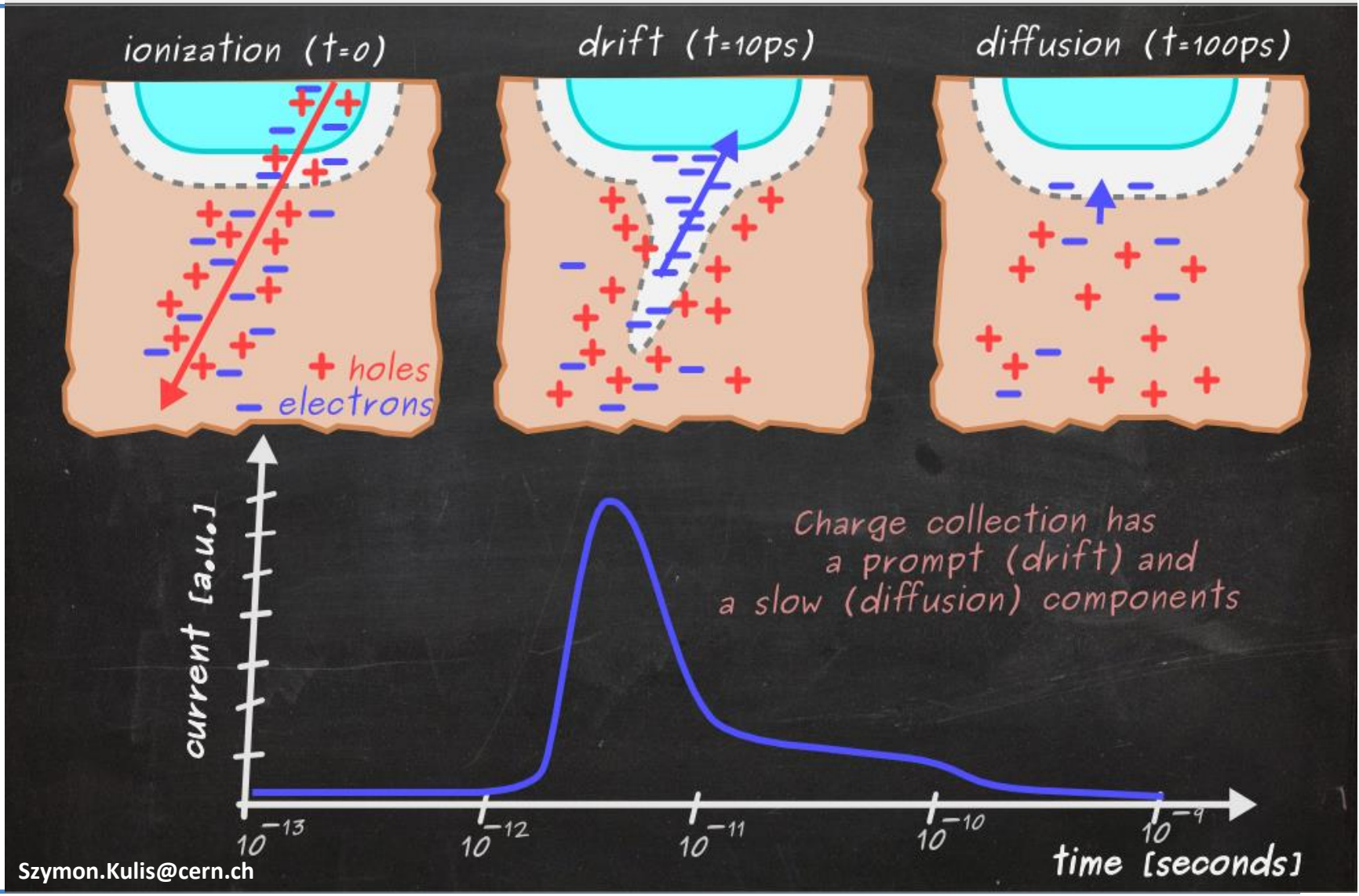
Some examples of ASICs in ATLAS



Radiation effects



Single Event Effects



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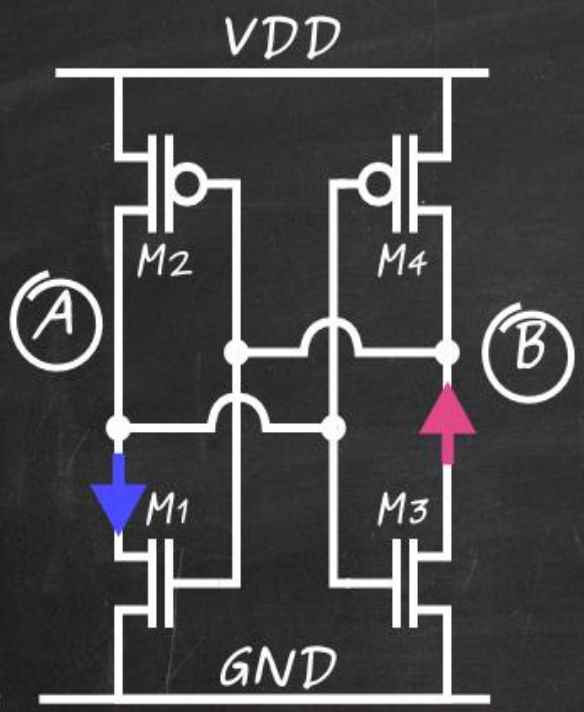
Single Event Effects – example



SRAM cell
(pass gates missing)

1) initial state : A=VDD, B=GND
2) charge deposited at drain of M1
3) transient current changes temporary the state of node A (VDD-> GND)
4) before the desposited charge is evacuated, the second inverter (M3-M4) switches (node B GND->VDD)
5) The change of node B enforces the wrong state at node A -> the error is latched into the memory cell

How much charge is needed to flip the value?

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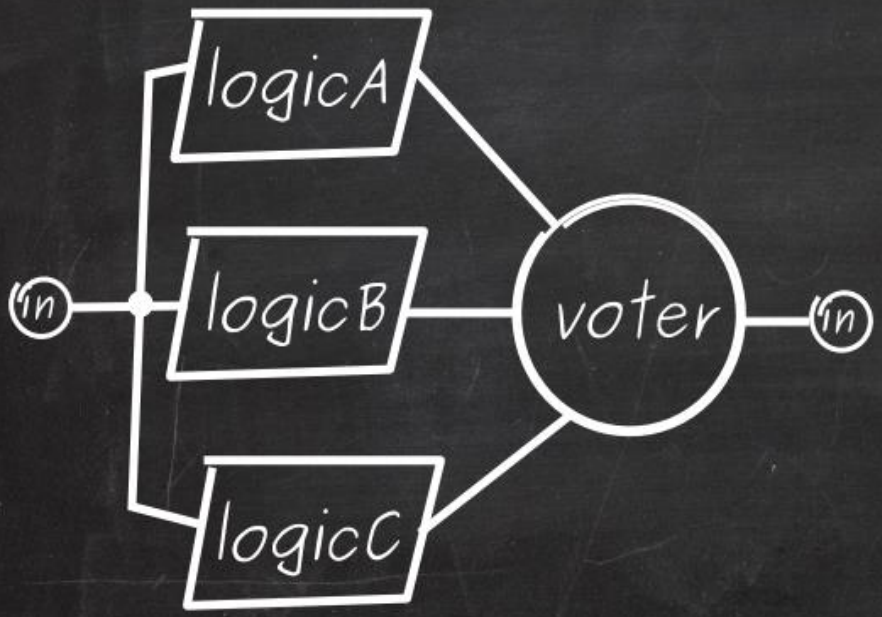
Triple Modular Redundancy (TMR)

TMRG

Normaly, the three blocks give the same output



A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
1	0	0	0
0	1	1	1
1	0	1	1
1	1	0	1
1	1	1	1

voter truth table

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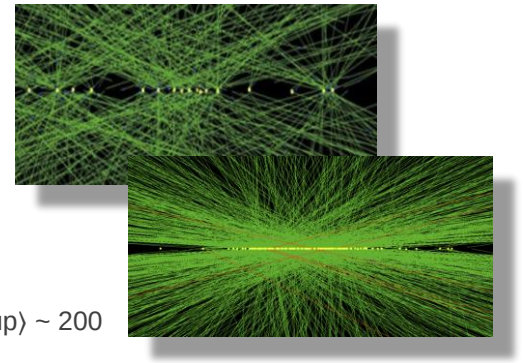
CMS Phase-2 upgrade challenges

- **LHC → HL-LHC**: sustained luminosity of $5x10^{34}$ $cm^{-2}s^{-1}$
  - From 20 → 200 pileup events per BX
  - μ, e and jets at exceedingly high rates
    - Increasing thresholds would affect physics performance
    - Performance of algorithms degrades with increasing pile-up

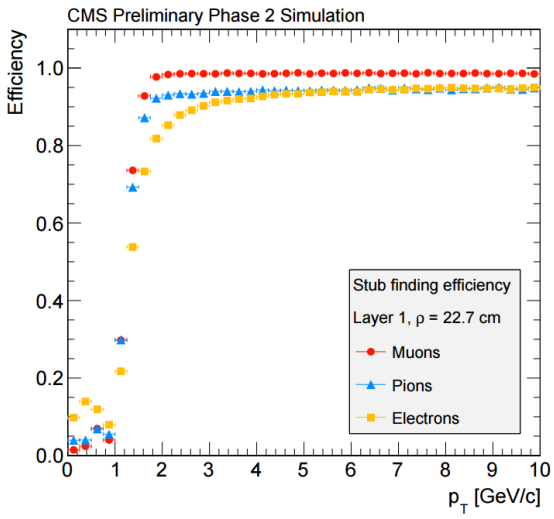


⟨Pile-up⟩ ~ 20

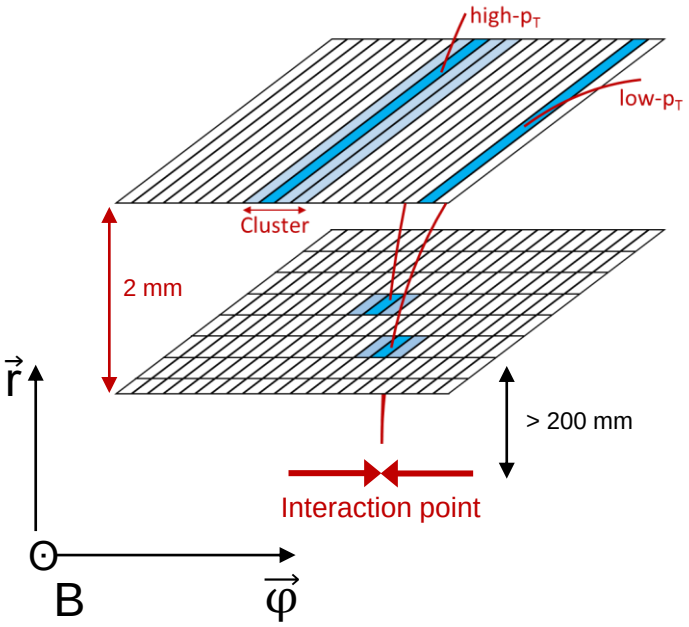
⟨Pile-up⟩ ~ 200

- Track Triggering
  - Add tracking information to the Level-1 trigger decision to keep trigger rate at an acceptable level
    - Trigger Rate 100 kHz → 750kHz
    - Trigger Latency 3.2 μs → 12.5 μs

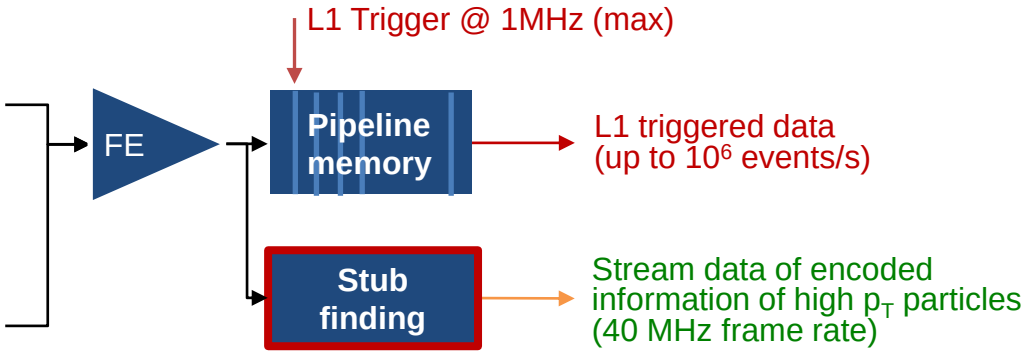
- Outer Tracker modules with p_T discrimination
  - Reject locally signals from low-p_T particles (< 2Gev)
  - Reduce data volume by one order of magnitude making transmission feasible for the available power budget
  - Simplify track finding algorithms



Intelligent particle tracking system



3.8T provided by the superconducting solenoid



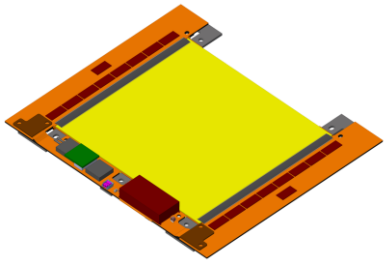
Discriminate particles locally based on their p_T transverse momentum and send only interesting particle hits to the Trigger System

- The CMS OT detector working principle of p_T discrimination
  - Exploit the strong magnetic field of CMS
  - Correlate signals between two closely spaced sensors to identify "stubs"
  - Stubs defined as a track coordinate + angle based on tracking window on parallel sensor
  - Transmit stub coordinates and momentum instead of a multiplicity of hits

Phase 2 CMS Outer Tracker

Outer Barrel

2S or Strip-Strip module



2 Strip sensors

No strips: ..... 2x 2 048 per side

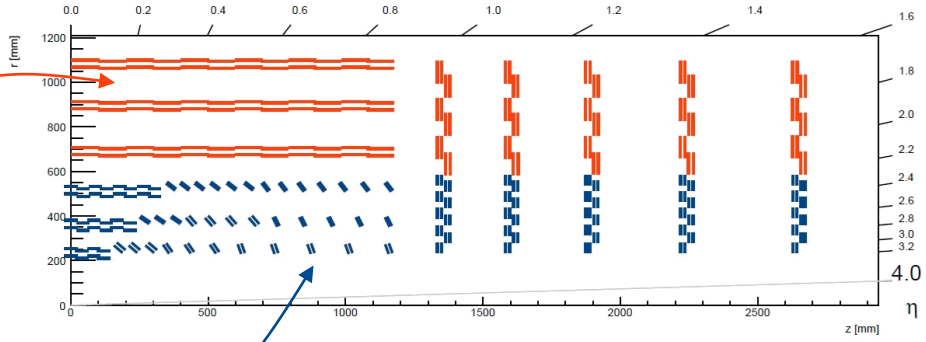
Strip size: ..... 5 cm x 90 μm

Spacing: ..... 1.8 mm and 4.0 mm

Active area: ..... 2 x 90 cm^2

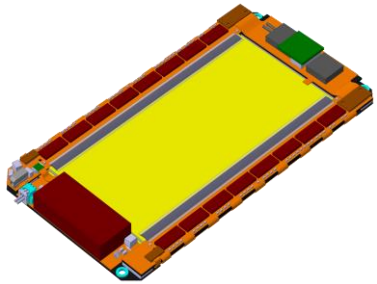
Total 2S modules:... 8 424

Phase 2 Outer Tracker Layout



Inner Barrel

PS or Pixel-Strip module



Pixel + Strip sensor

No strips: ..... 2 x 960 = 1 920 strips

Strip size: ..... 2400 mm x 100 μm

No pixels: ..... 32 x 960 = 30 720 pixels

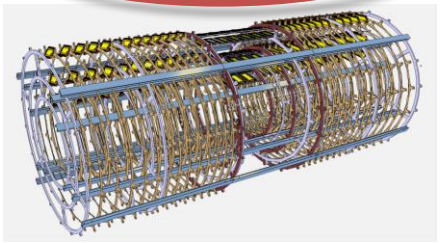
Pixel size: ..... 1.5 mm x 100 μm

Spacing: ..... 1.6 mm, 2.6 mm and 4.0 mm

Active area: ..... 2 x 45 cm^2

Total PS modules:... 5 708

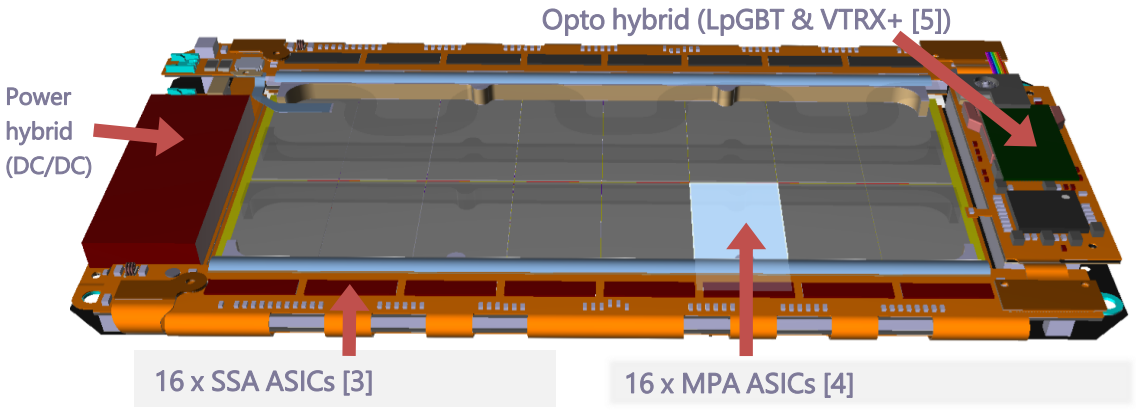
13 296 Modules
44 Mstrips + 174 Mpixels
200m^2 of silicon area

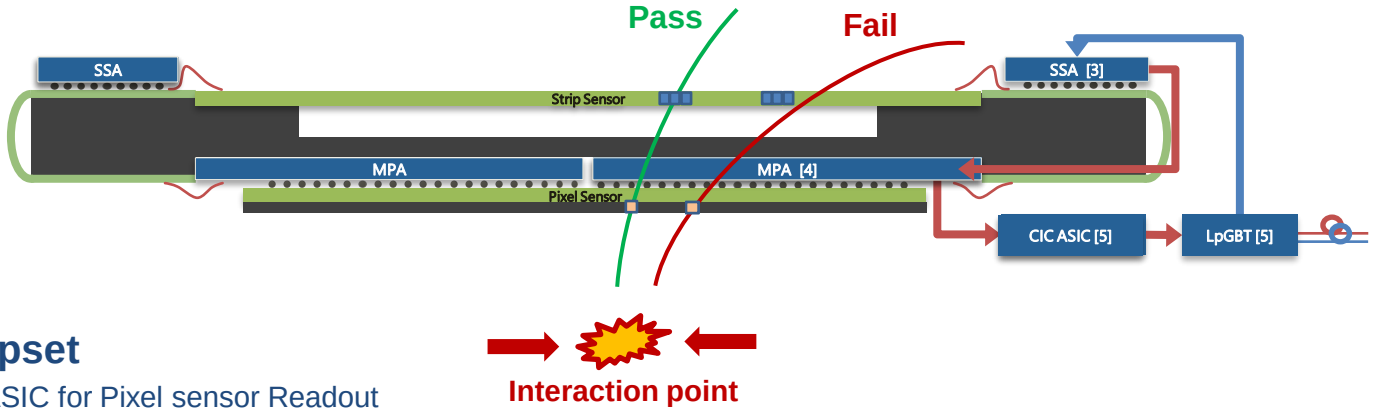


Power density: .... < 100 mW/cm^2

[1] CMS collaboration. "The phase-2 upgrade of the CMS tracker." CMS-TDR-014 (2017).
[2] Abbaneo, Duccio. "Upgrade of the CMS Tracker with tracking trigger." Journal of Instrumentation 6.12 (2011): C12065.

The Pixel-Strip (PS) module





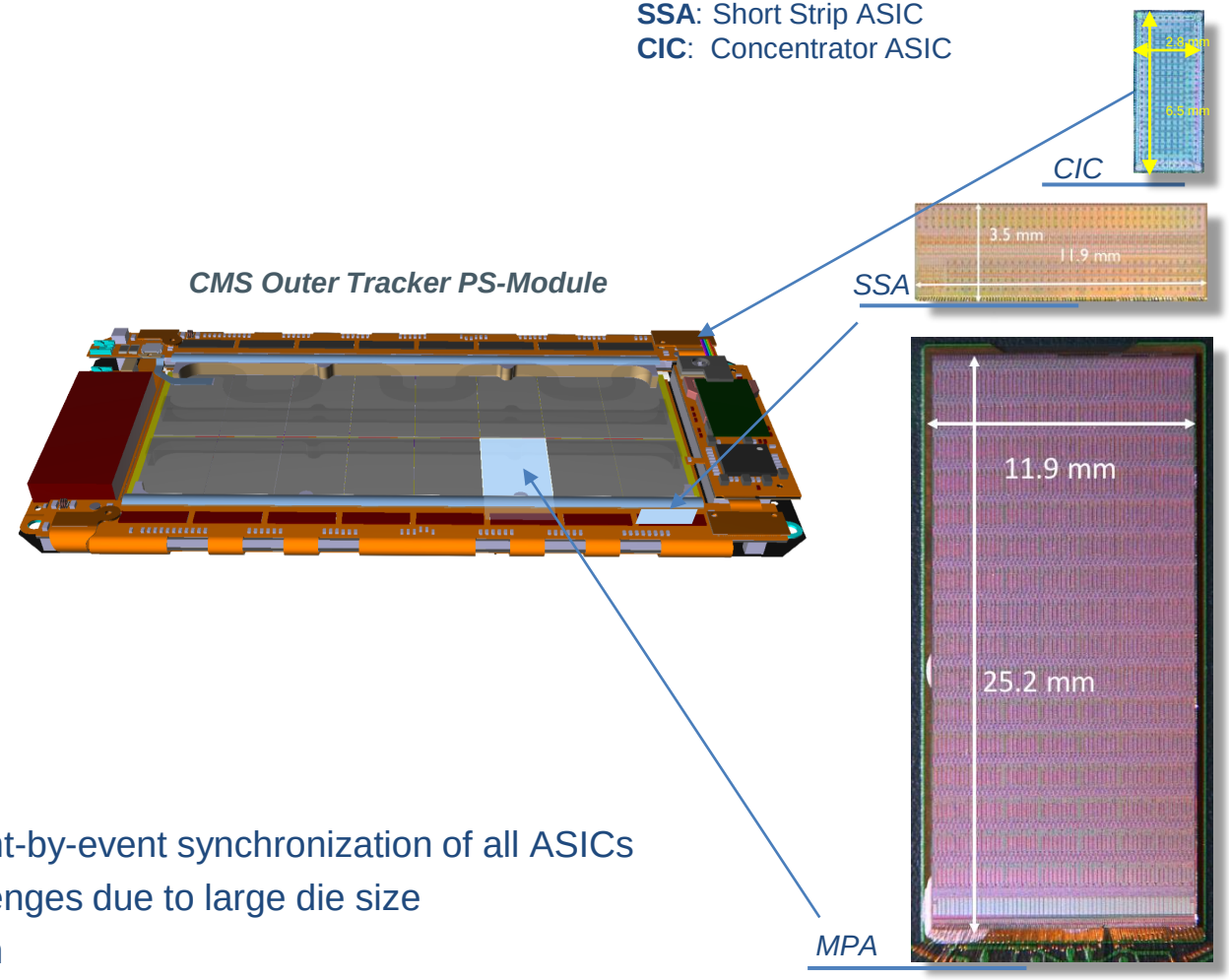
- Readout **ASIC chipset**
  - **MPA**: Macro Pixel ASIC for Pixel sensor Readout
  - **SSA**: Short Strip ASIC for Strip sensor Readout
  - **CIC**: Concentrator ASIC for data aggregation and transmission through optical gigabit link

[3] Caratelli, Alessandro, et al. Characterization of the first prototype of the Silicon-Strip readout ASIC (SSA). No. CMS-CR-2018-286. 2018.
[4] Ceresa, Davide, et al. Characterization of the MPA prototype, a 65 nm pixel readout ASIC with on-chip quick transverse momentum discrimination capabilities. No. CMS-CR-2018-279. 2018.
[5] Moreira, Paulo. "The LpGBT project status and overview." ACES. 2016.
[6] Nodari, Benedetta, et al. A 65 nm data concentration ASIC for the CMS outer tracker detector upgrade at HL-LHC. No. CMS-CR-2018-278. 2018.

PS-module ASICs Project

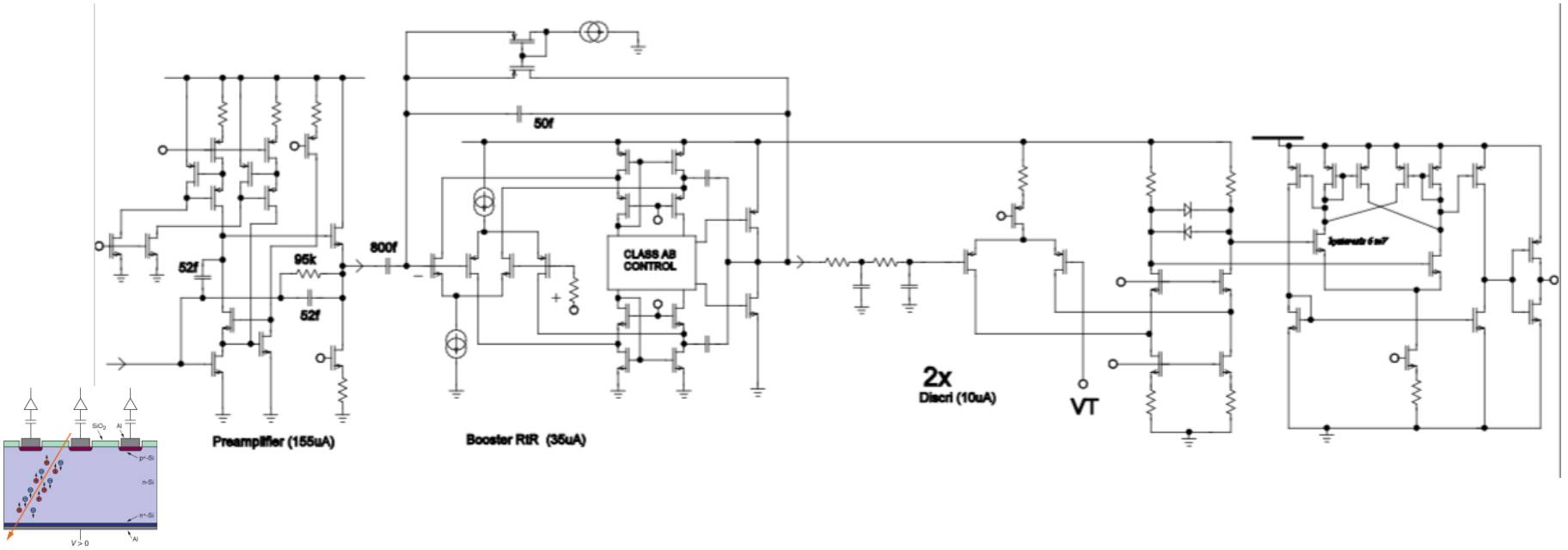
- Design Teams
  - **CERN (MPA, SSA, CIC)**
    - Alessandro Caratelli
    - Davide Ceresa
    - Jan Kaplon
    - Gianmario Bergamin
    - Kostas Kloukinas
    - Simone Scarfi
  - **Lyon IPNL/IN2P3 (CIC)**
    - Luigi Caponetto
    - Geoffrey Galbit
    - Benedetta Nodari
    - Sebastian Viret

MPA: Macro Pixel ASIC
SSA: Short Strip ASIC
CIC: Concentrator ASIC



- Challenging project
  - Interoperability and event-by-event synchronization of all ASICs
  - MPA ASIC design challenges due to large die size
  - Low Power consumption

SSA analog front-end architecture



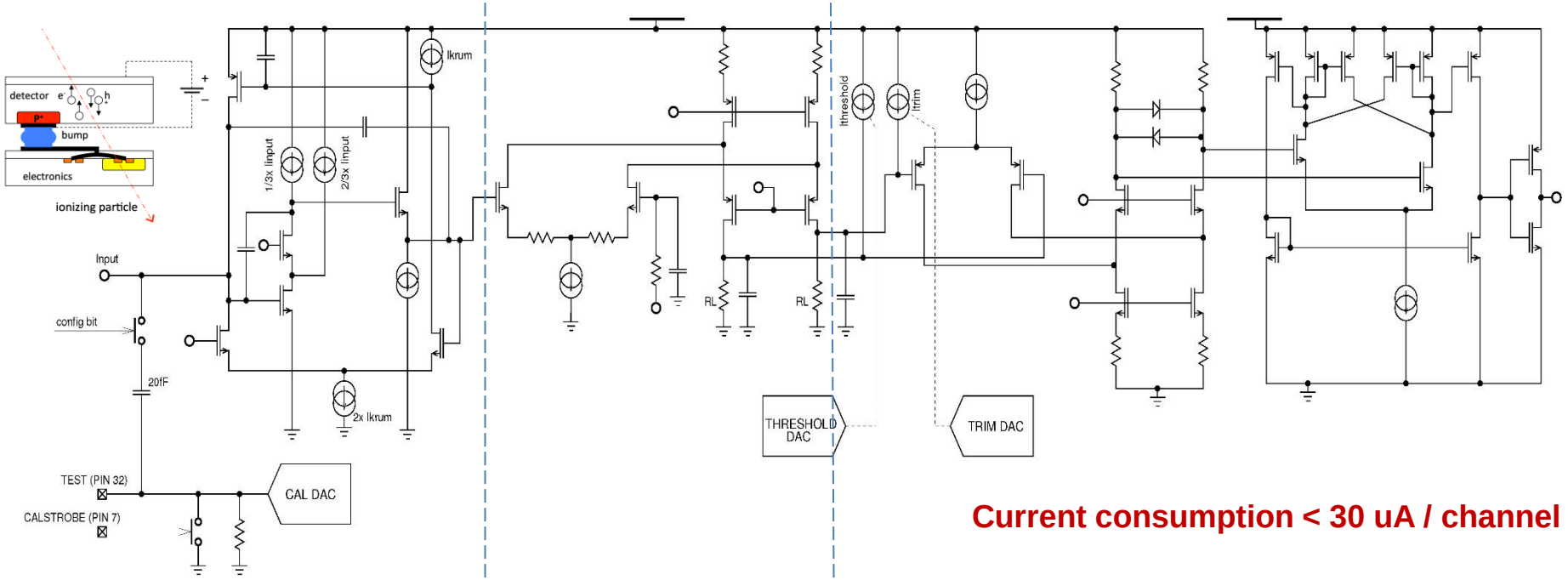
- Schematic design of the analog channel
  - **Preamp**: regulated cascode transimpedance amplifier
  - **Booster**: class AB buffer with active feedback for overshoot attenuation
  - **3 stage discriminator**, folded cascode with resistive feedback (Discriminator for HIPs not shown)

Design parameters

Peaking time:	17 ns
Gain:	60 mV/fC
GBP:	2.7 GHz
ENC (5 pF input):	< 800 e^-
Max consumption:	250 µA

Designer: Jan Kaplon

MPA analog front-end architecture



Current consumption < 30 uA / channel

Preamplifier

Transimpedance Preamplifier with Krummenacher feedback leakage current compensation for n^+ on p^- detectors

Shaper

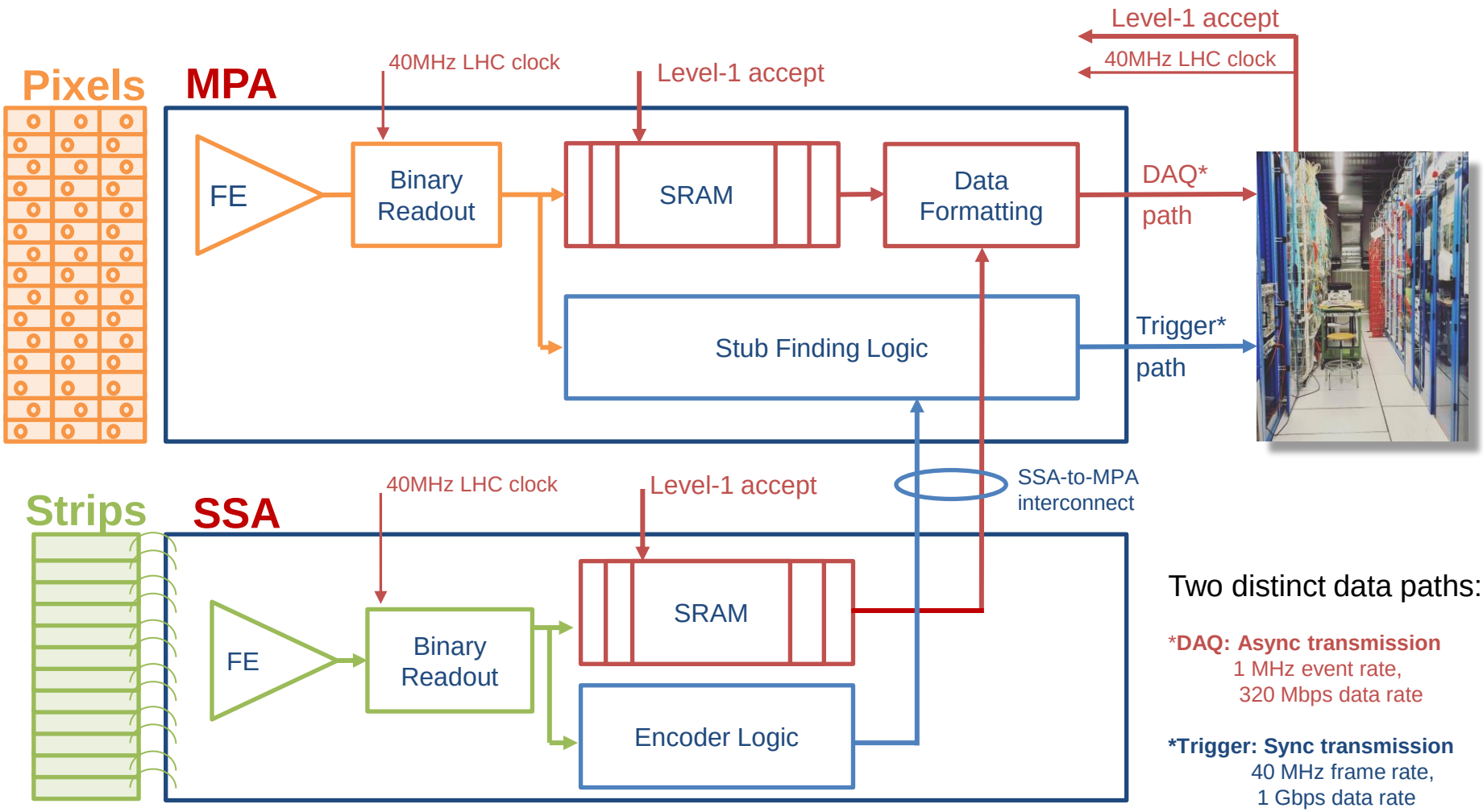
Single-ended to differential folded cascode stage with resistive load

Discriminator

- PMOS folded cascode input
- Swing limiter based on PMOS working in diode configuration
- Second stage with hysteresis (6mV)

Designer: Jan Kaplon

MPA-SSA Readout Concept



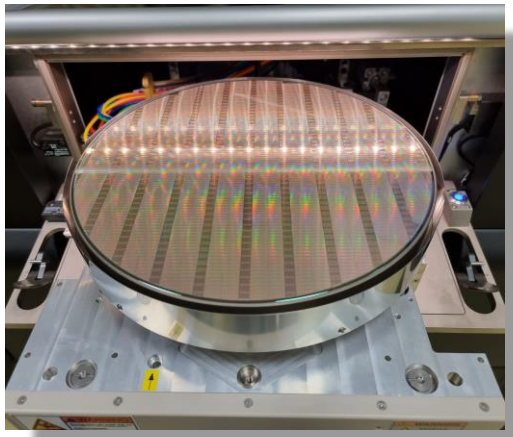
Two distinct data paths:

***DAQ: Async transmission**
1 MHz event rate,
320 Mbps data rate

***Trigger: Sync transmission**
40 MHz frame rate,
1 Gbps data rate

PS module ASICs

- Two full mask-set Engineering Runs on a 9-metal 65nm bulk CMOS process
- Prototype designs were tested
  - at die-on-board assemblies using custom made (FPGA based) test benches
  - at wafer level using a probe station at CERN
- Test routines include:
  - Scan-chain test for production defects
  - Functional test of digital circuits
  - Analog bias parameter caracterization
  - Front-end caracterization
  - Noise analysis
  - Serial ID and trimming in e-fuses

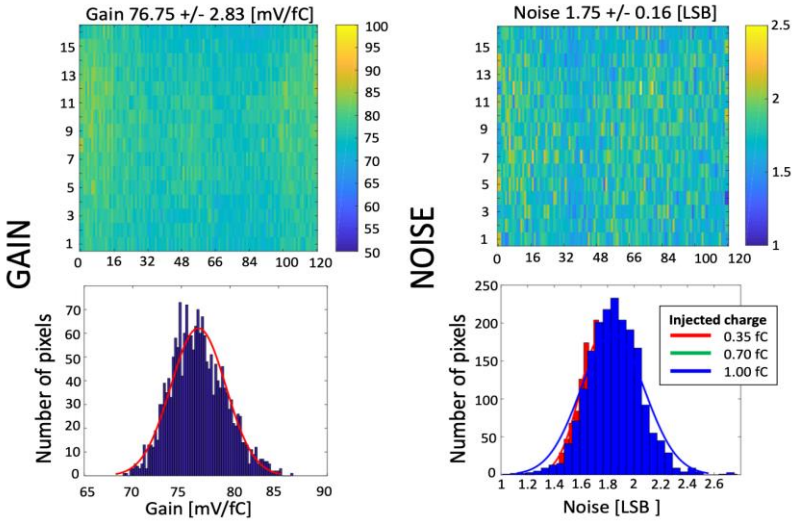


MPA prototype characterization

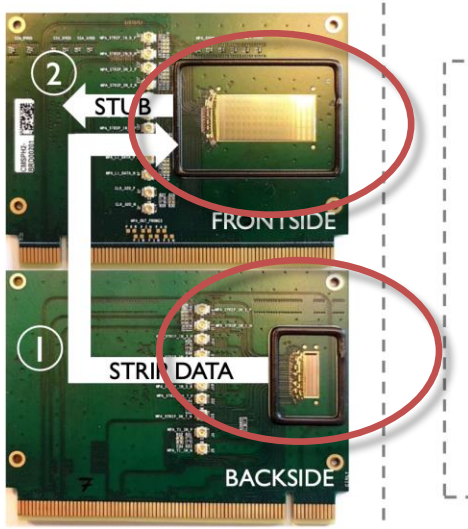
MPA and SSA first prototypes were proved functional and within specs…

FE results

- ENC < 200 e-
- Peaking time ~ 25 ns
- SNR >> 20
- Time walk < 15 ns
- Threshold 0.5 fC ~ 3120 e-



STUB GENERATION



POWER CONSUMPTION

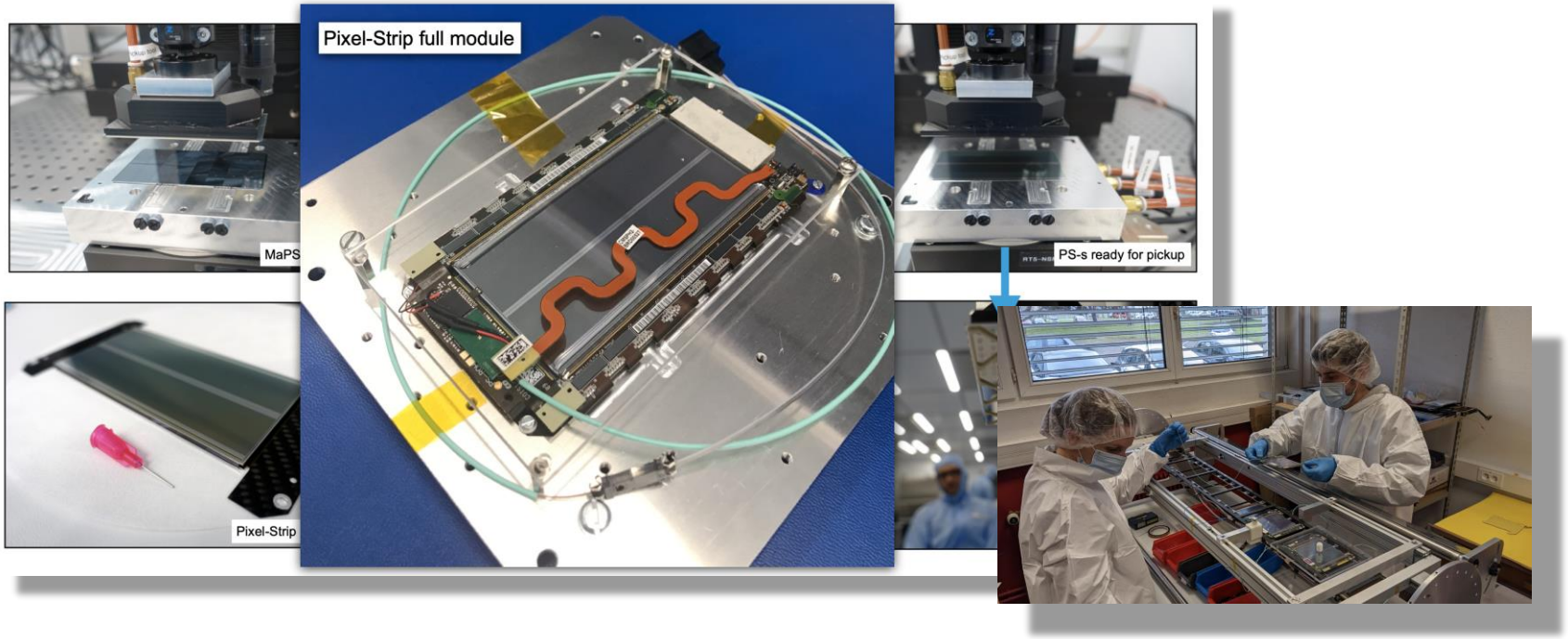
Configured w/o activity:
MPA: 184 mW
SSA: 67 mW

Increase w/ activity:
MPA: < +10 mW
SSA: < +2 mW

MAX power < 275 mW

Proved the feasibility of quick and on-chip particle discrimination

PS Module assembled

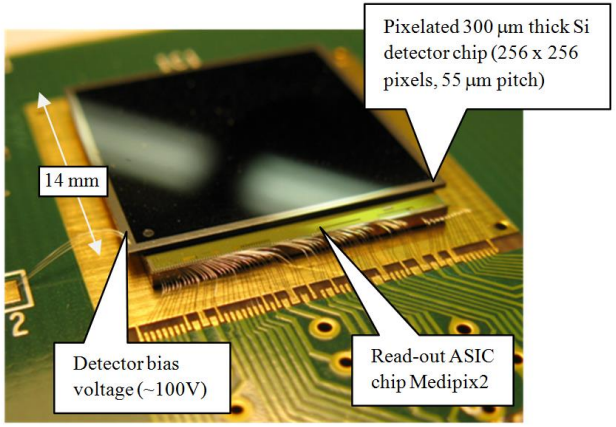


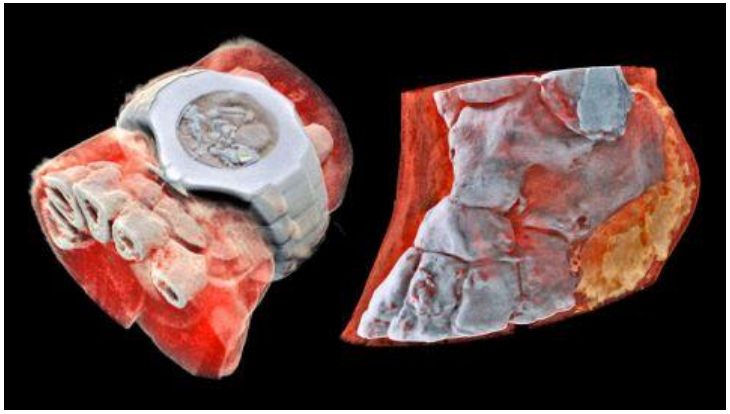
Pixel Sensors in Medical Imaging

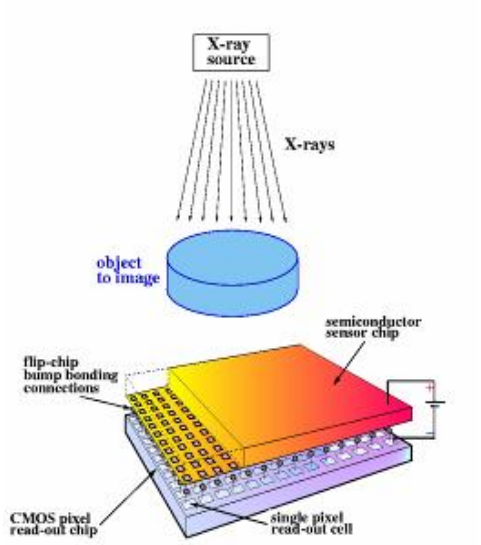
New X-ray technology produces striking 3D images in full colour

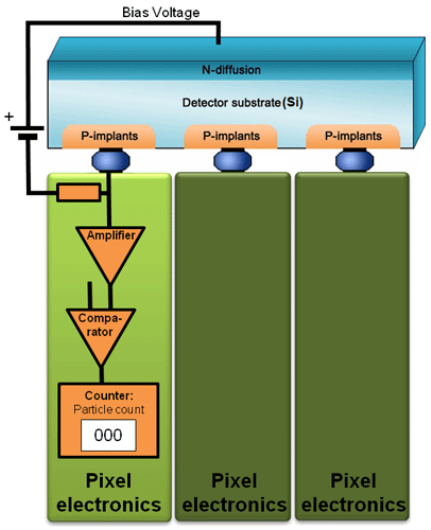
A new medical imaging device uses technology developed by particle physicists to produce full colour, 3D images of the human body.

A hybrid detector capable of counting each individual particle hitting the pixels and measure its energy.







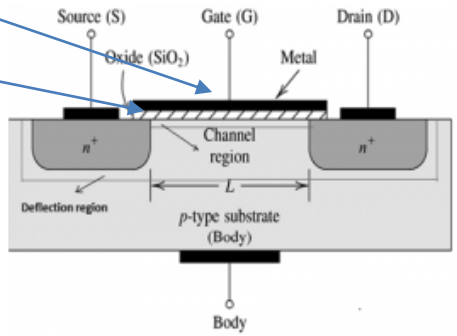


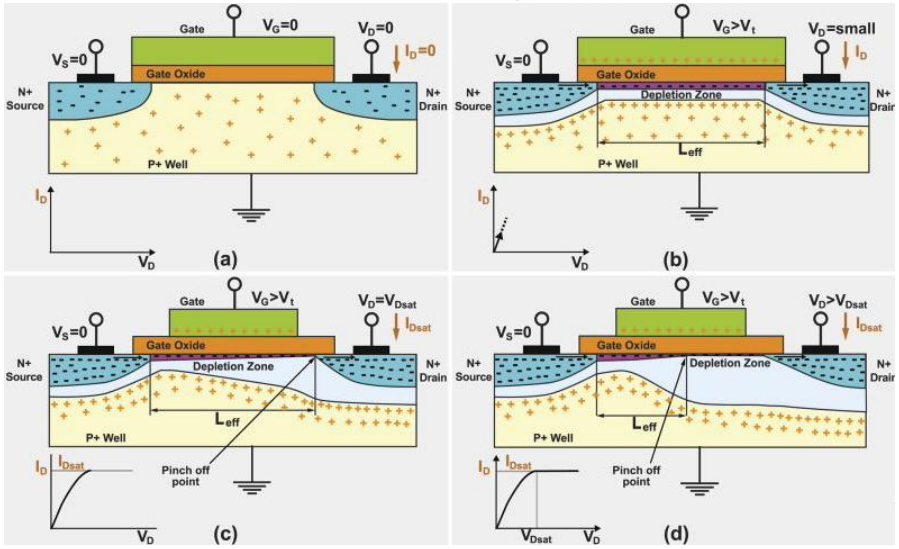
MOSFET

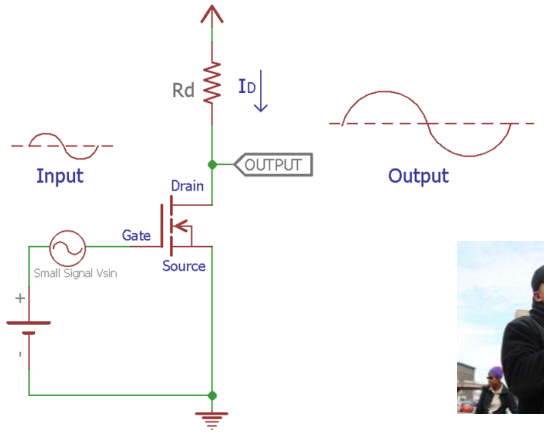
MOSFET : Metal Oxide Field Effect Transistor

Polysilicon Gate

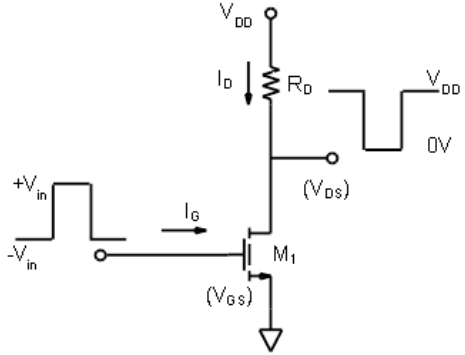
SiO_2 Dielectric







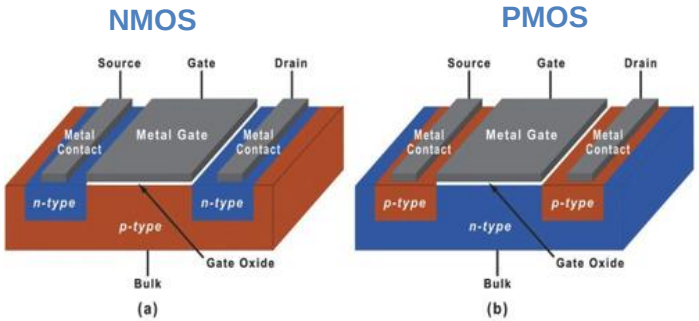
NMOS FET as an amplifier in **Analog circuits**

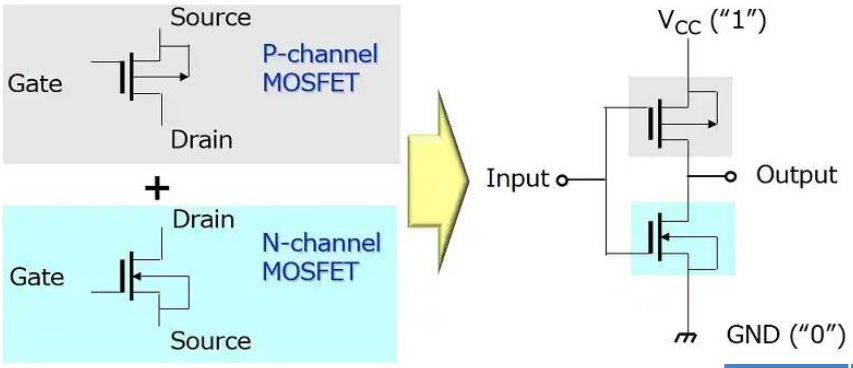


NMOS FET as a switch in **Digital circuits**

CMOS Transistors

CMOS : Complementary Metal Oxide Field Effect Transistor

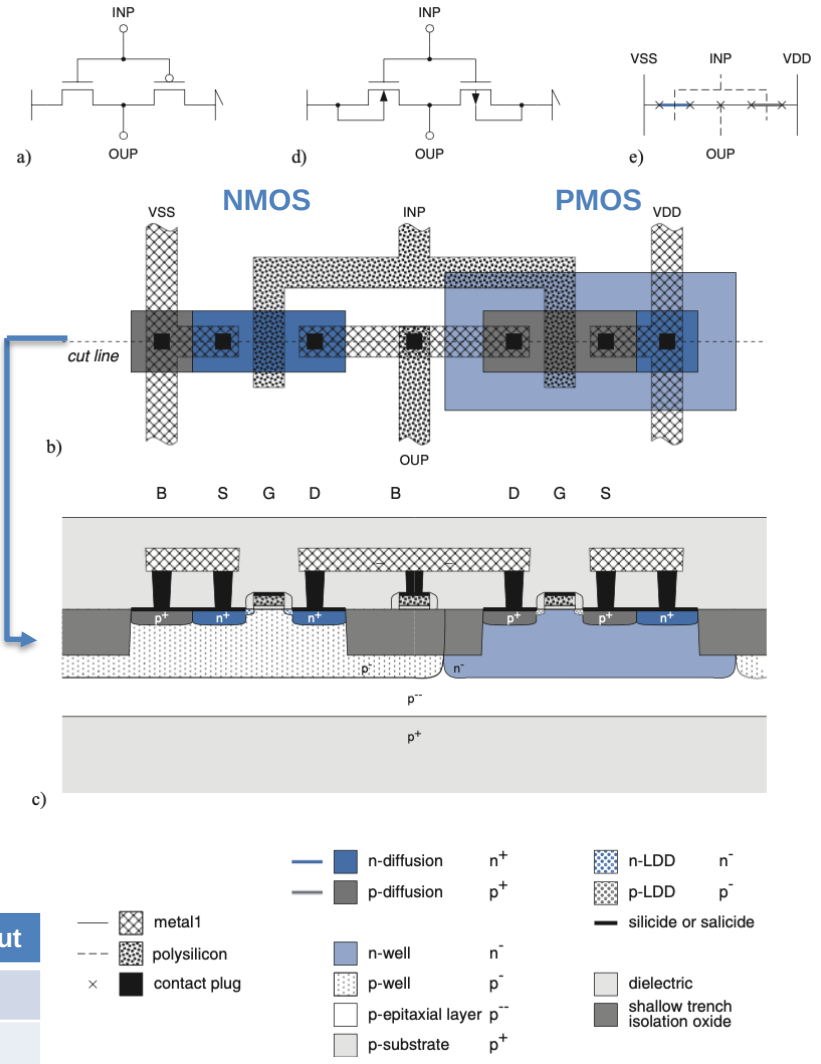




Input	Output
0	1
1	0

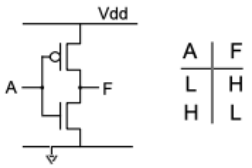
CMOS Inverter for **Digital circuits**

(solves the static current problem of NMOS circuits when the Output value is "0")



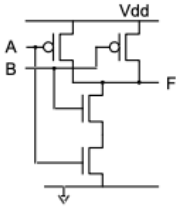
CMOS Logic Gates

Basic CMOS Logic Gates and their truth table



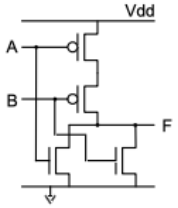
A	F
L	H
H	L

CMOS INVERTER



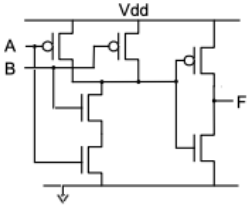
A	B	F
L	L	H
L	H	H
H	L	H
H	H	L

CMOS NAND



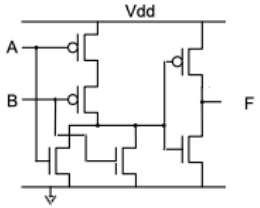
A	B	F
L	L	H
L	H	L
H	L	L
H	H	L

CMOS NOR



A	B	F
L	L	L
L	H	L
H	L	L
H	H	H

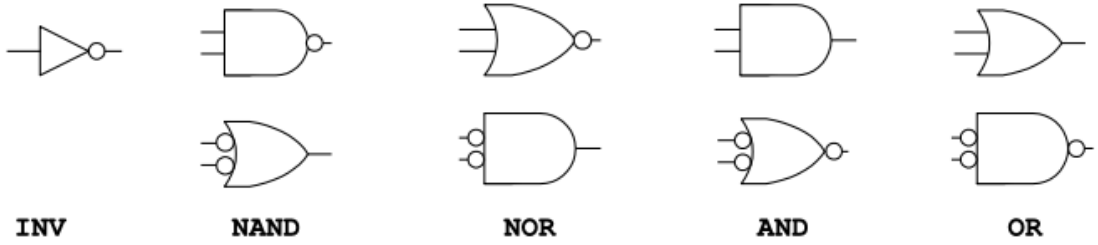
CMOS AND



A	B	F
L	L	L
L	H	H
H	L	H
H	H	H

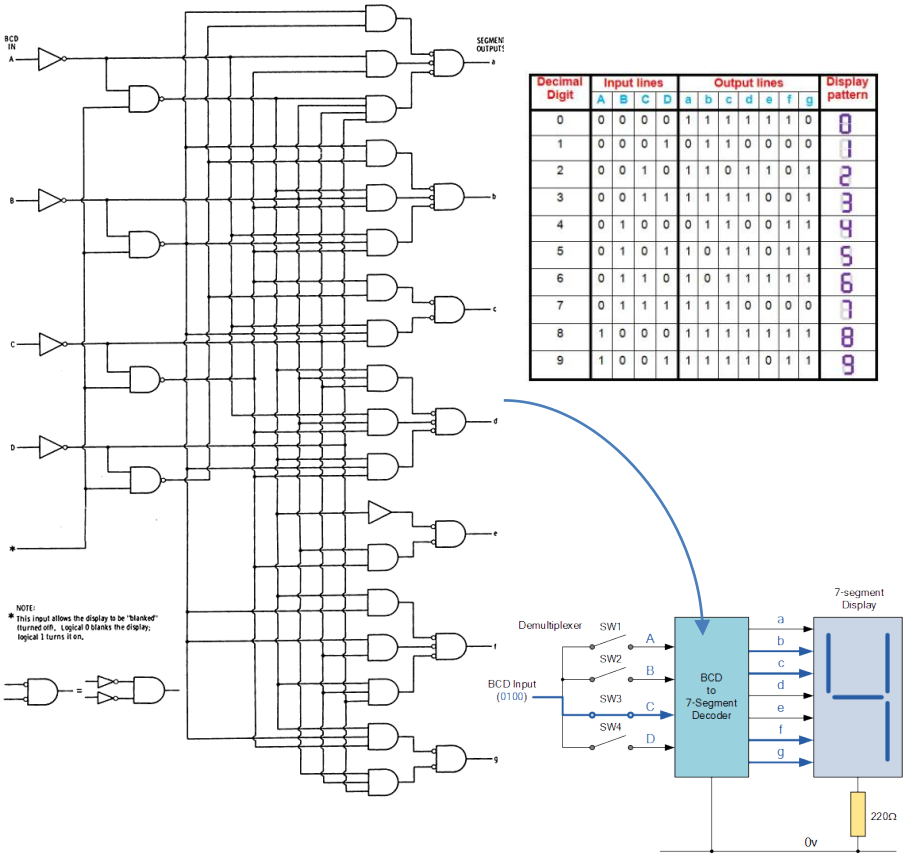
CMOS OR

Basic CMOS Logic Gate Symbols



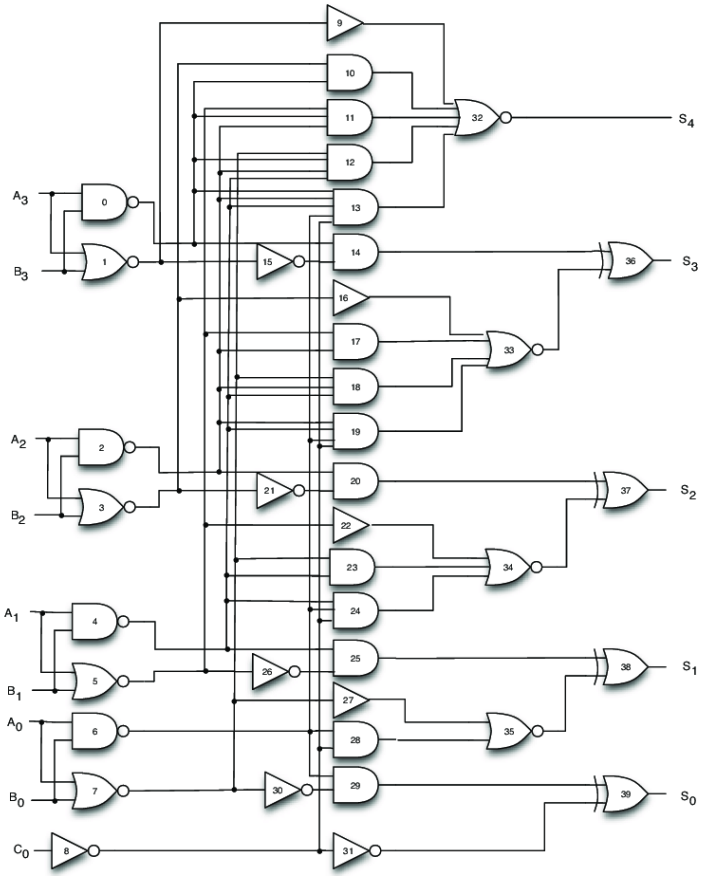
INV NAND NOR AND OR

Logic Gate Circuit examples



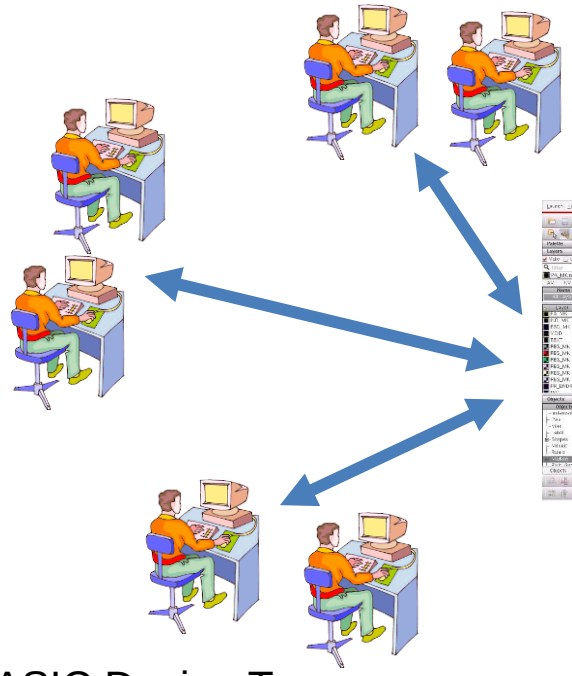
Decimal Digit	Input lines				Output lines							Display pattern
	A	B	C	D	a	b	c	d	e	f	g	
0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1	0	0	0	0	1
2	0	0	1	0	1	1	0	1	1	0	1	2
3	0	0	1	1	1	1	1	1	0	0	1	3
4	0	1	0	0	0	1	1	0	0	1	1	4
5	0	1	0	1	1	0	1	1	0	1	1	5
6	0	1	1	0	1	0	1	1	1	1	1	6
7	0	1	1	1	1	1	1	0	0	0	0	7
8	1	0	0	0	1	1	1	1	1	1	1	8
9	1	0	0	1	1	1	1	1	0	1	1	9

Binary to 7-segment display decoder



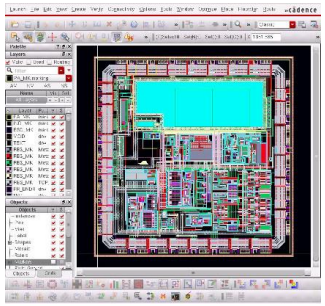
4-bit Adder with fast carry

ASIC design in HEP community



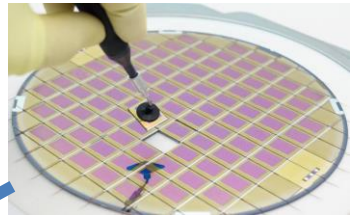
ASIC Design Teams

Computer Tools

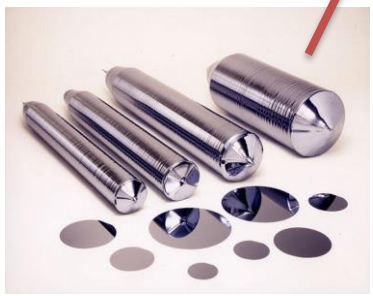


Fabrication Plant

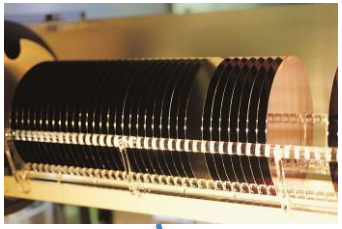
Dicing and shorting

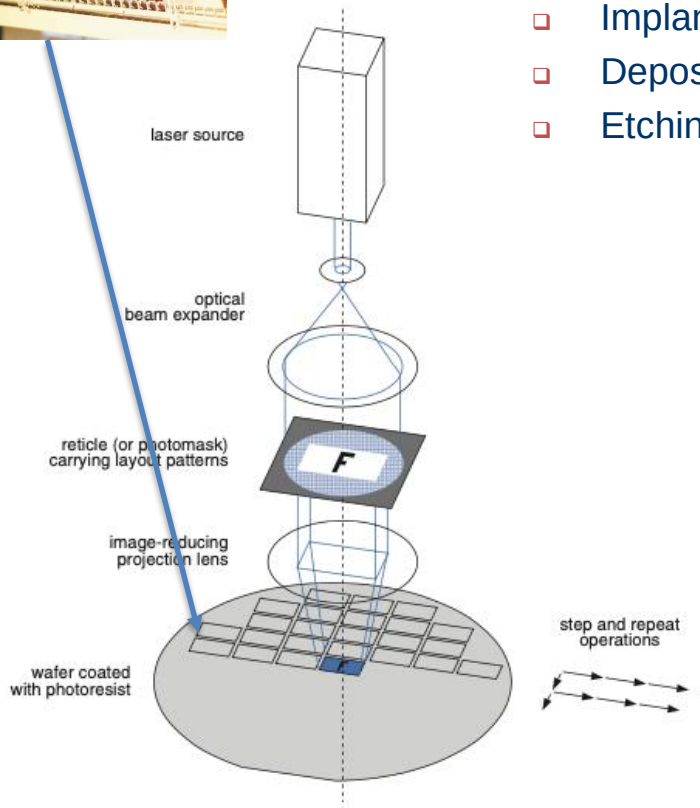


Semiconductor Manufacturing Process Flow Chart



CMOS Fabrication





Apparatus for optical lithography (greatly simplified).

- Fabrication Steps
  - Ilumination
  - Implantation
  - Deposition
  - Etching

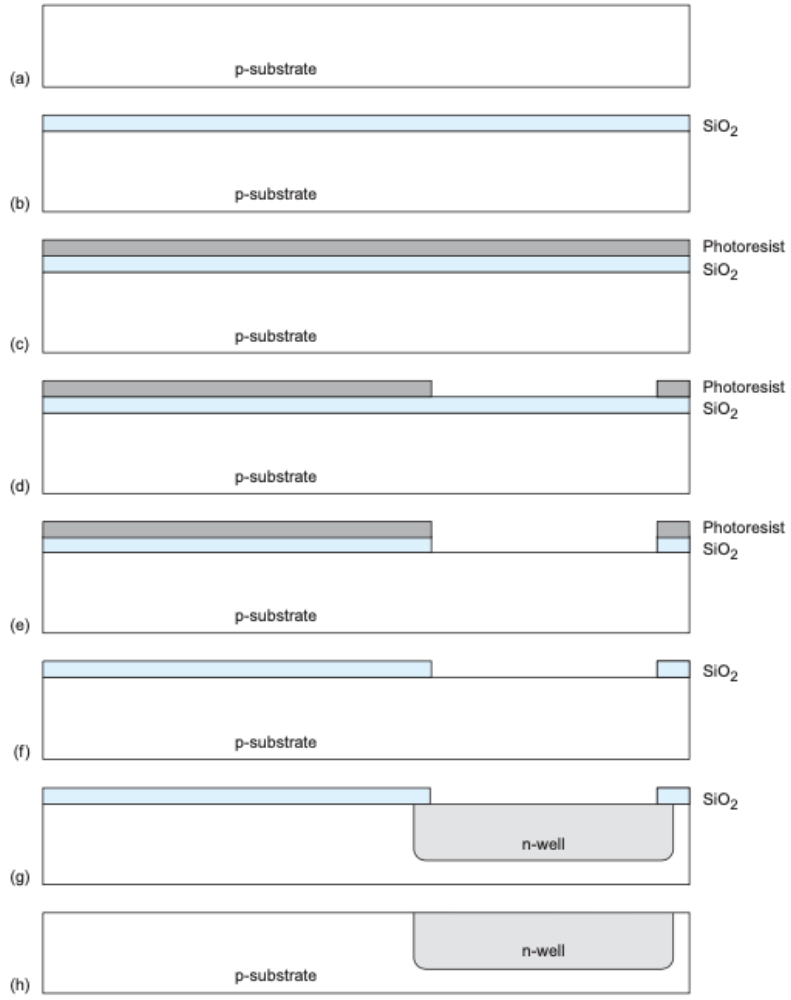


FIGURE 1.36 Cross-sections while manufacturing the n-well

CMOS Fabrication

Complementary Metal Oxide Semiconductor

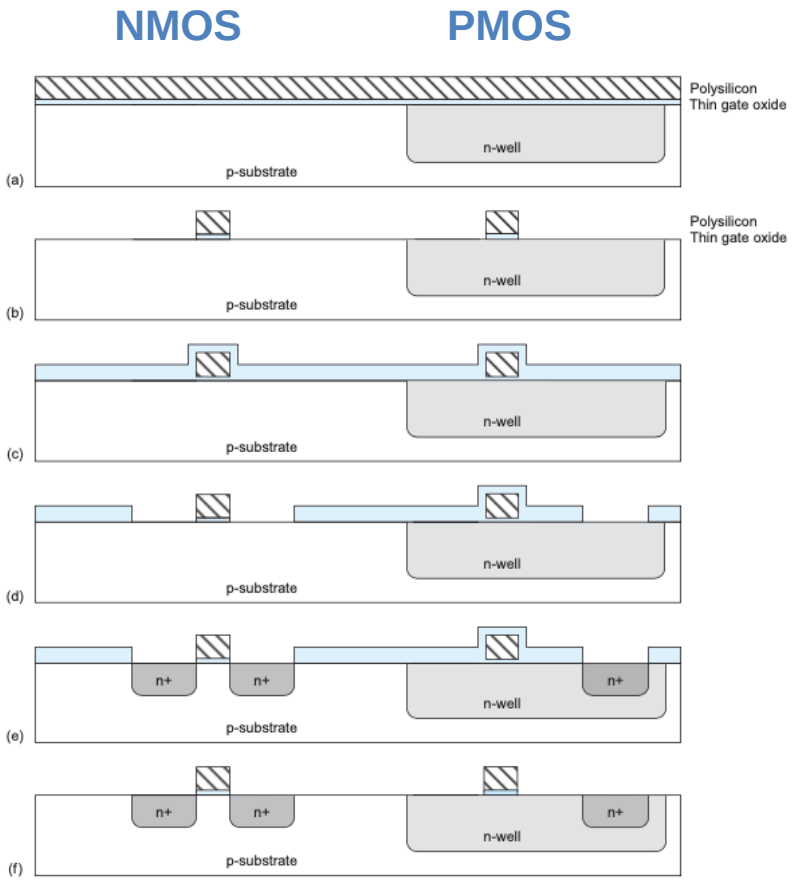


FIGURE 1.37 Cross-sections while manufacturing polysilicon and n-diffusion

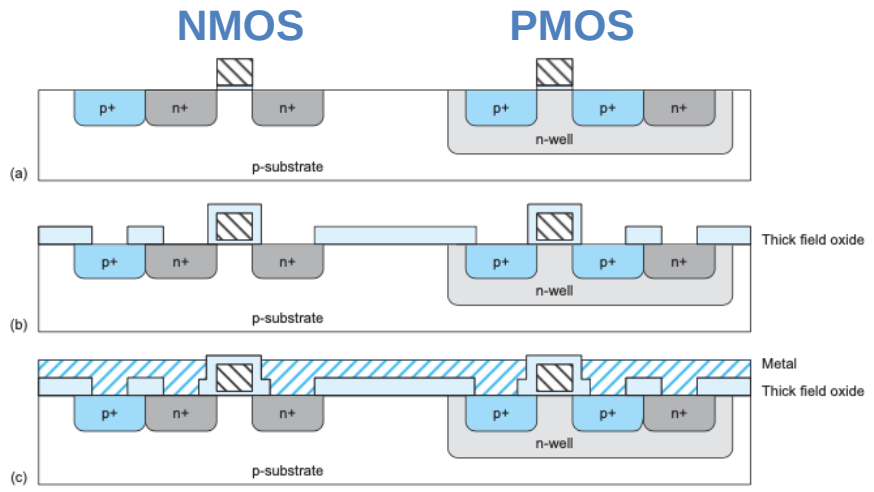
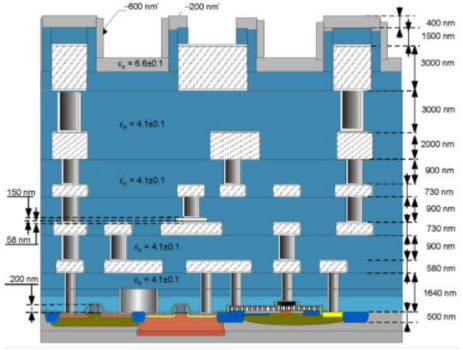
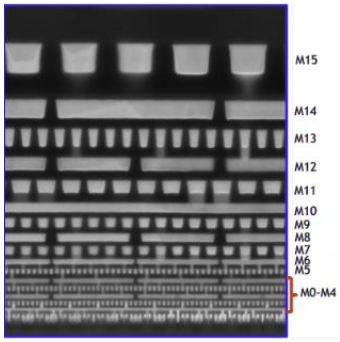


FIGURE 1.38 Cross-sections while manufacturing p-diffusion, contacts, and metal





CMOS Fabrication

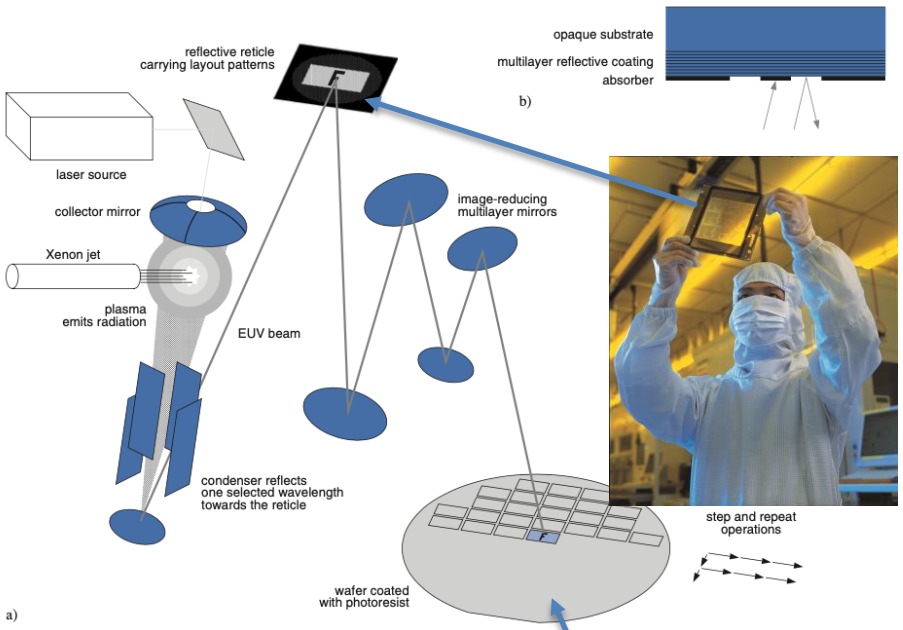


Fig. 14.25 Apparatus for EUV lithography (a) and cross section through a reflective mask (b), mirrors are the same with no absorbing coating (greatly simplifed).

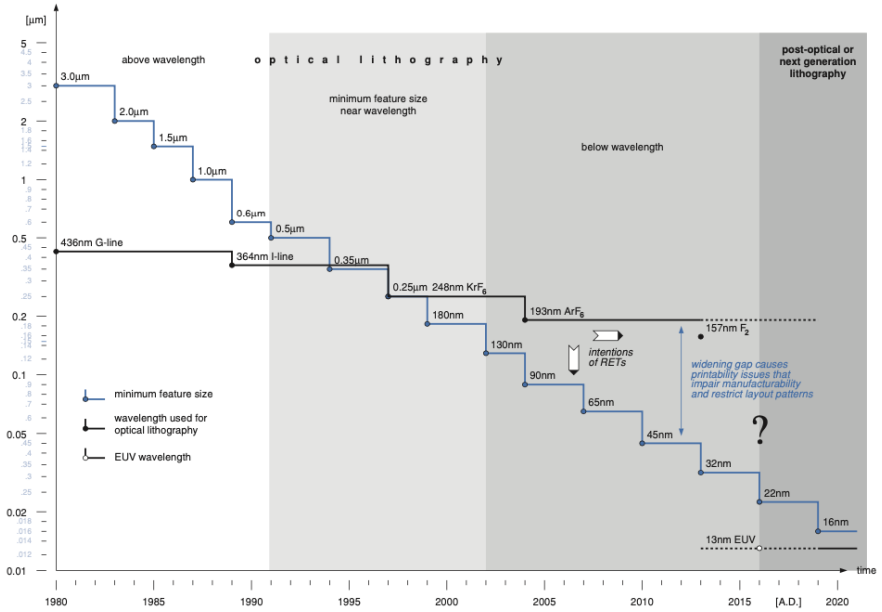


Fig. 14.22 Evolution of VLSI lithography.

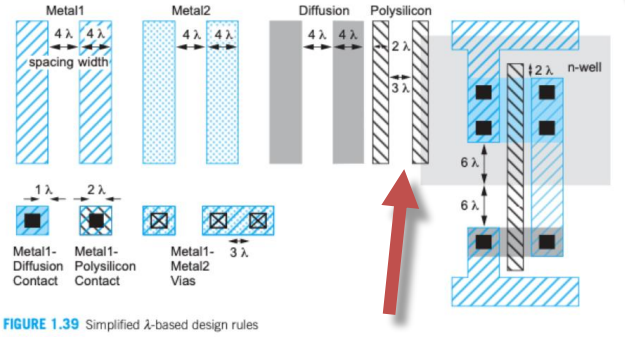
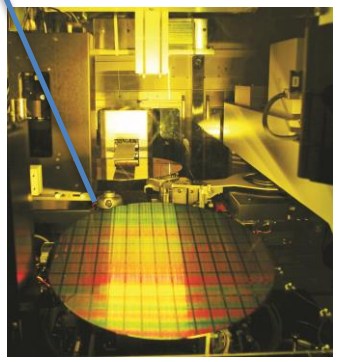


FIGURE 1.39 Simplified λ-based design rules



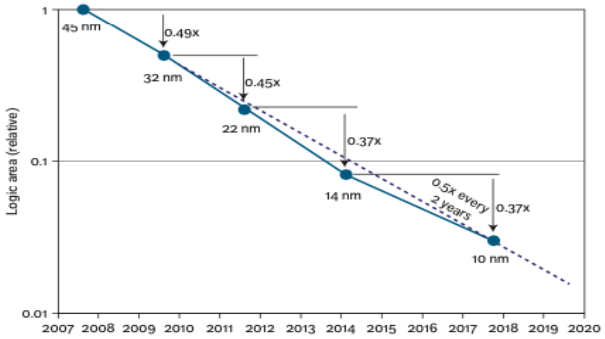
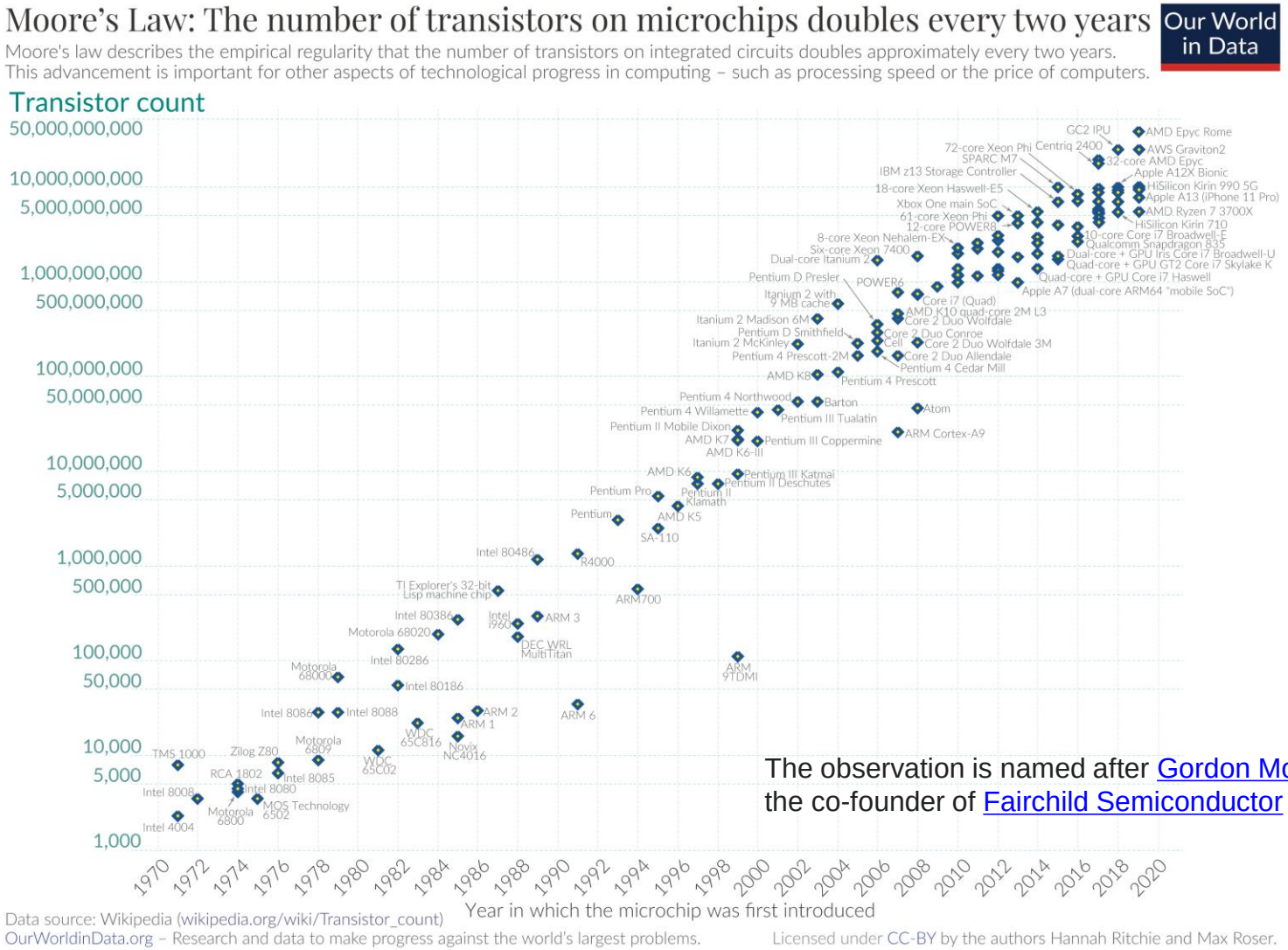


Figure 8. Intel's trend for scaling logic circuit area over the past five generations.

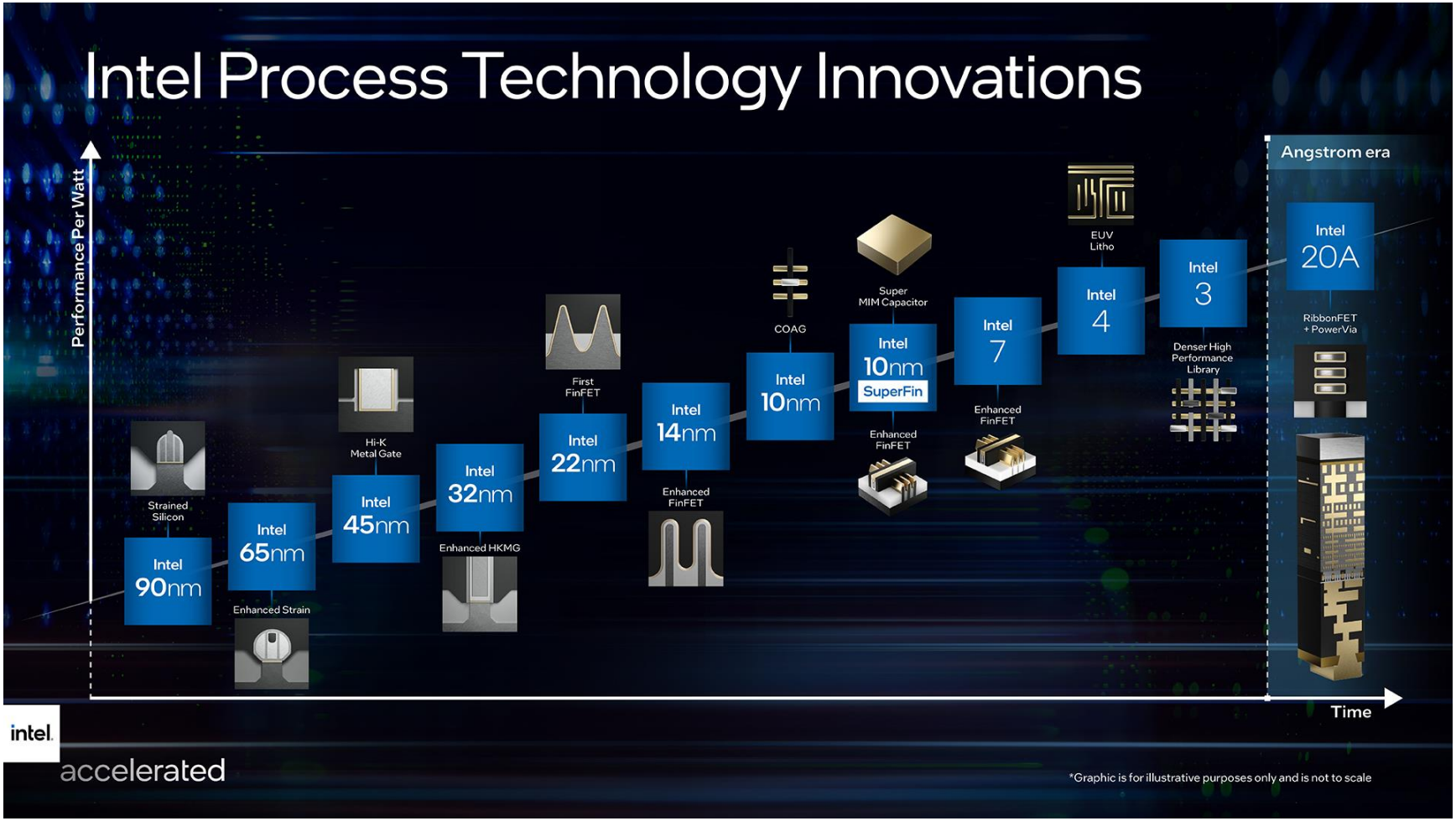
Moore's Law



The observation is named after Gordon Moore, the co-founder of Fairchild Semiconductor and Intel

Evolution of Intel Processors

Evolution of Intel Processors



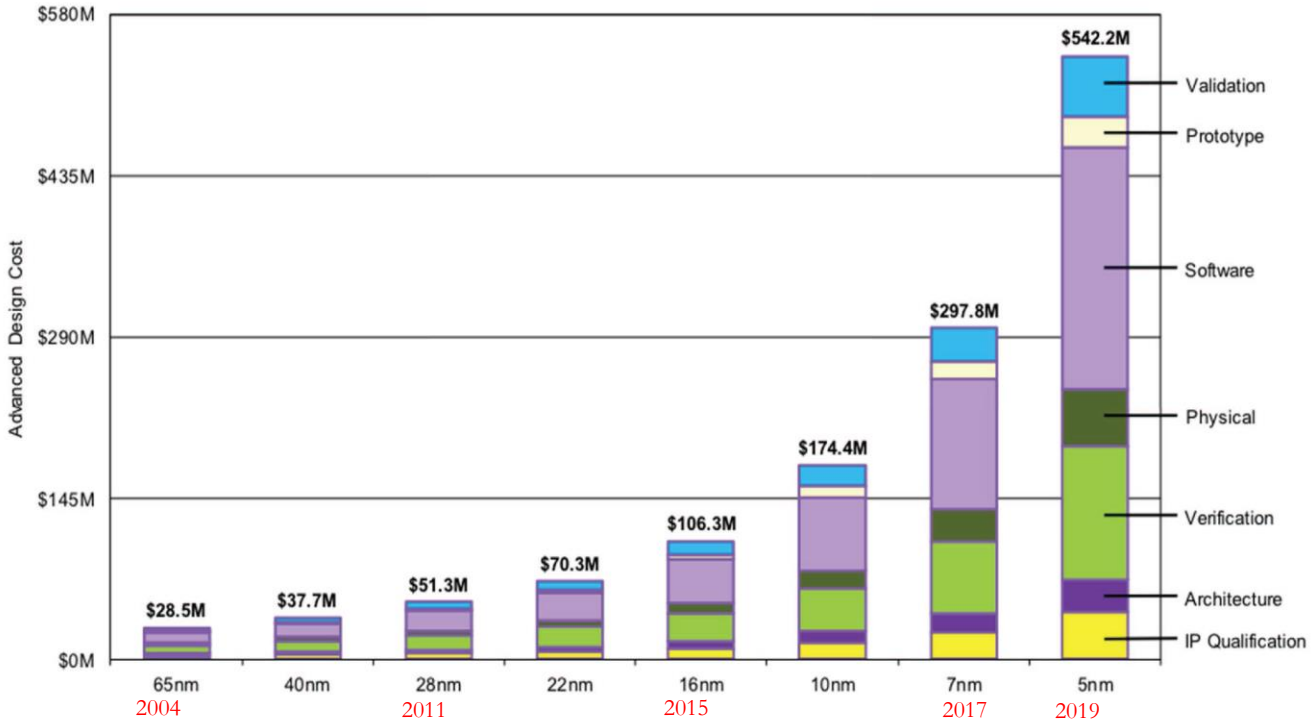
Semiconductor Foundry (Plant)

Construction cost of a modern Plant ~$20 billion

A Major Fab

Location	
AP1 **Hsinchu, Taiwan**	
AP2B **AP2C** *(Under construction)* **Tainan, Taiwan**	 
AP3 **Longtan, Taiwan**	
AP5 **Taichung, Taiwan**	
AP6 *(Under construction)* **Chunan, Taiwan**	

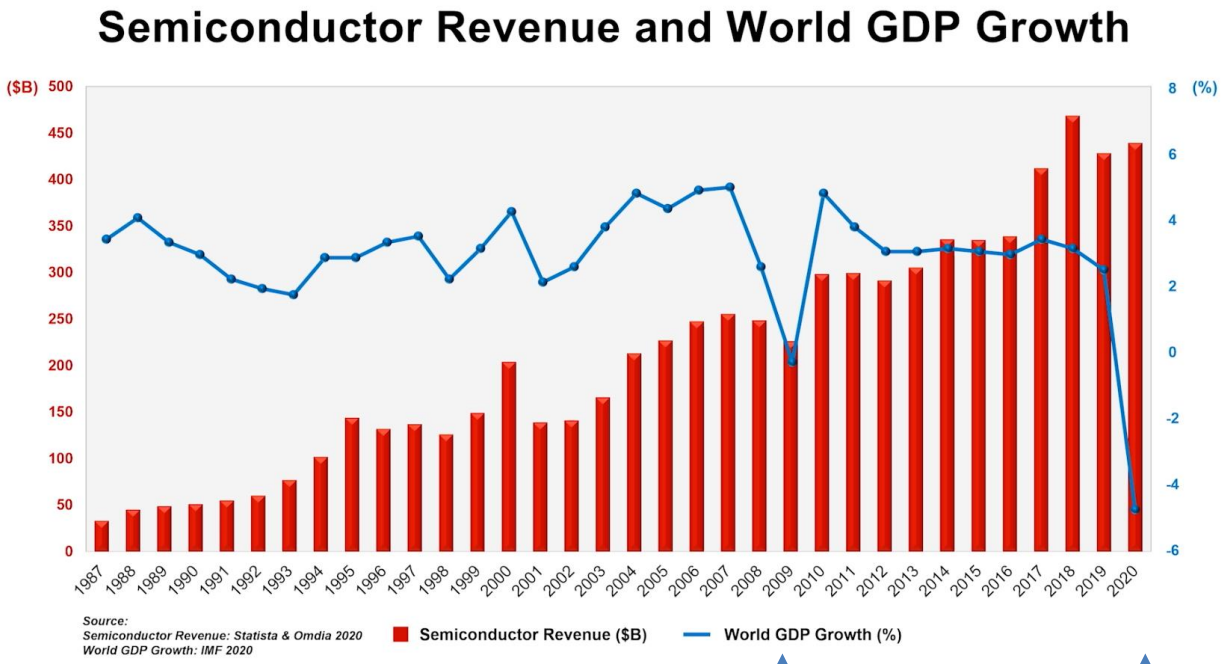
ASIC development costs



Chip Design and Manufacturing Cost under Different Process Nodes: Data Source from IBS*

* According to the survey from the *International Business Strategy Corporation (IBS),*
the increase of design cost for each generation technology has exceeded 50% after 22 nm process, including EDA, design verification, IP core, tape-out, and so forth.

Semiconductor industry

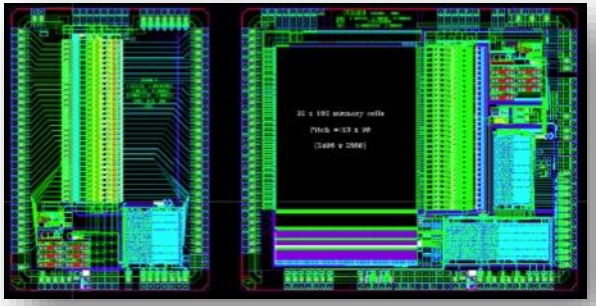


Summary

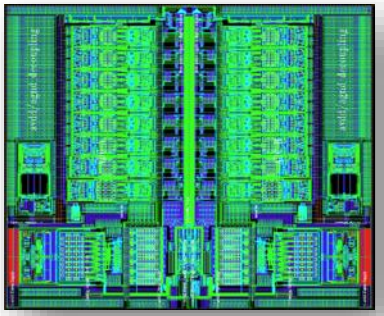
- Application-specific integrated circuits (ASICs) are the enabling technology for many complex detector systems
  - Customised electronic circuits for a well-defined application
  - Typically manufactured in CMOS processes
- Pros of ASICs
  - **Optimised** for demanding requirements: size, power, functions, performance,...
  - **Miniaturised**, ideal for high density HEP (large number of channels)
  - High **quality with low unit cost** on large scale
  - **Radiation hardness** using commercial processes
- Cons of ASICs
  - **Big development investment** required in both time and cost increasing as functionality (= complexity) increases
  - **Unchangeable** once complete, unless a lot of flexibility is built-in(adds complexity)
  - **Substantial design and evaluation** requiring specialist skills (industry pays well!)


Thank You

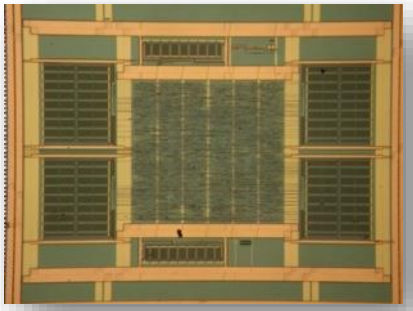
Typical ASIC designs at CERN



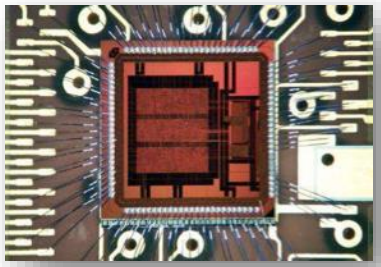
128ch pre-amp, analog memory chipset



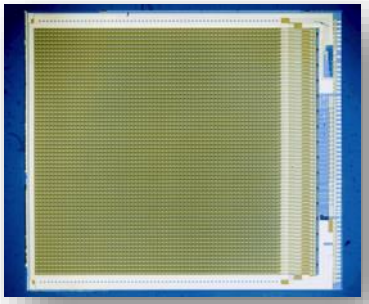
4ch 40Msps 12-bit ADC



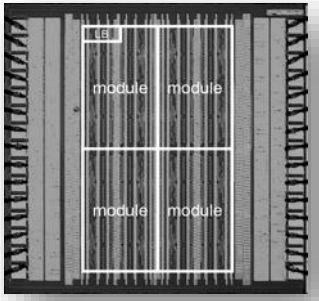
4ch data readout chip



Gigabit Optical Link



MEDIPIX1 Pixel chip



Rad-Tol FPGA

- Typical ASIC designs:
  - Analog circuits with complex full custom designs
  - Mixed Signal with large high performance analog and digital circuits
  - Digital circuits ~500K gates.

250nm ASICs

130nm Major Projects

- Gigabit Transceiver Project (GBT)
  - “GBLD” Gigabit Laser Driver chip final version in 2012.
  - “GBT-TIA” Transimpedance Amplifier chip in 2010.
  - “GBTX”, Transceiver chip, first prototype in 2009, second prototype in 2012.
  - “GBT-SCA”, Slow Control Adapter, first prototype in 2013.
- Design Projects for the XFEL Synchrotron facility
  - XFEL & DSSC ASIC designs
  - Prototype chips submitted in 2010, 2011, 2012.
  - DSSC full prototype submission scheduled for early 2014.
- CBC: CMS Tracker Front-End ASIC
  - First prototype submitted in 2010 MPW.
  - Second prototype submitted in 2012 MPW.
- S-Altro: ALICE TPC Readout ASIC
  - Submitted in 2010 on an MPW (24 wafers).
- NA62 Pixel Gigatracker detector
  - Test chips prototyped in 2010.
  - First prototype submitted in 2013.