Low Temperature Hybrid Graphene-Silicon Charge Amplifier

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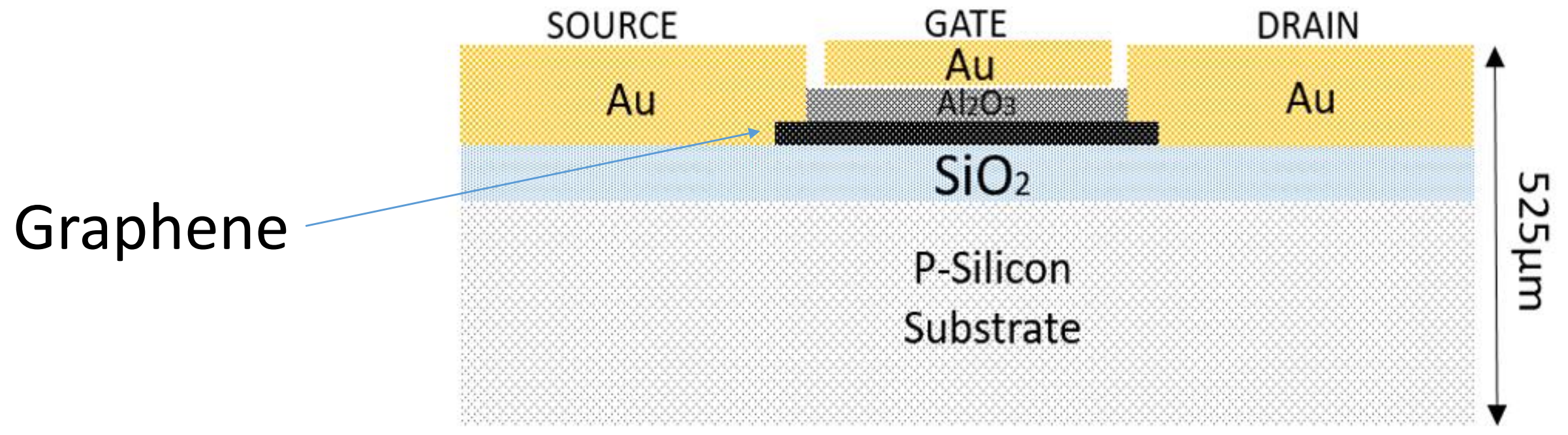
Abstract

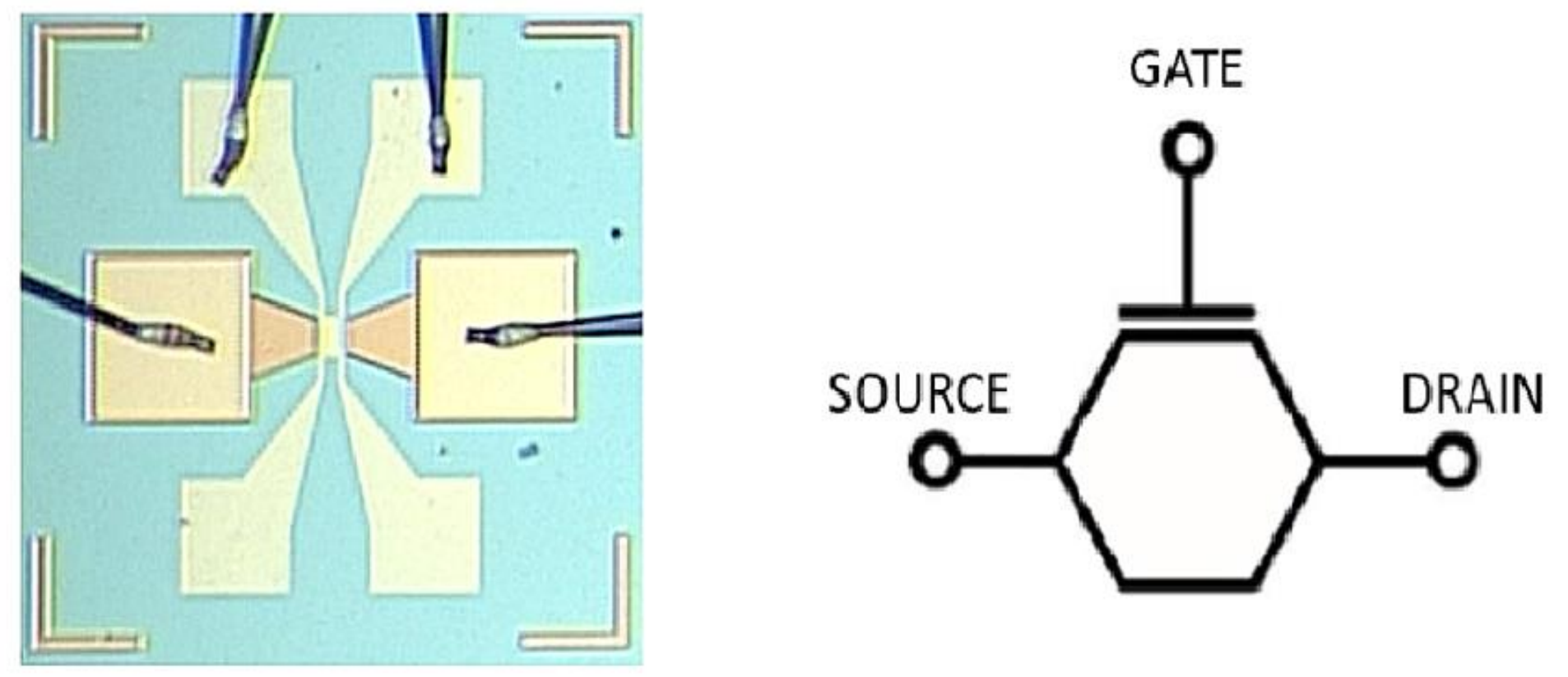
This study presents a novel charge amplifier tailored for amplifying signals originating from devices such as Silicon Photomultipliers (SiPMs) and High Purity Germanium Detectors (HPGe) at cryogenic temperatures (77K), commonly employed in fundamental physics experiments. The distinctive feature of the proposed charge amplifier lies in its utilization of a front-end transistor fabricated from graphene, integrated with a silicon-based differential amplifier. The graphene device employed is a Graphene Field-Effect Transistor (GFET), functioning analogously to a conventional Field-Effect Transistor (FET), with the unique capabilities provided by graphene. This device harnesses the inherent advantages of an FET, including high input impedance, while capitalizing on graphene-specific benefits such as low noise and high conductivity. These attributes make it particularly well-suited for the targeted application, enhancing overall performance.



Stack profile of the GFET utilized in this study.

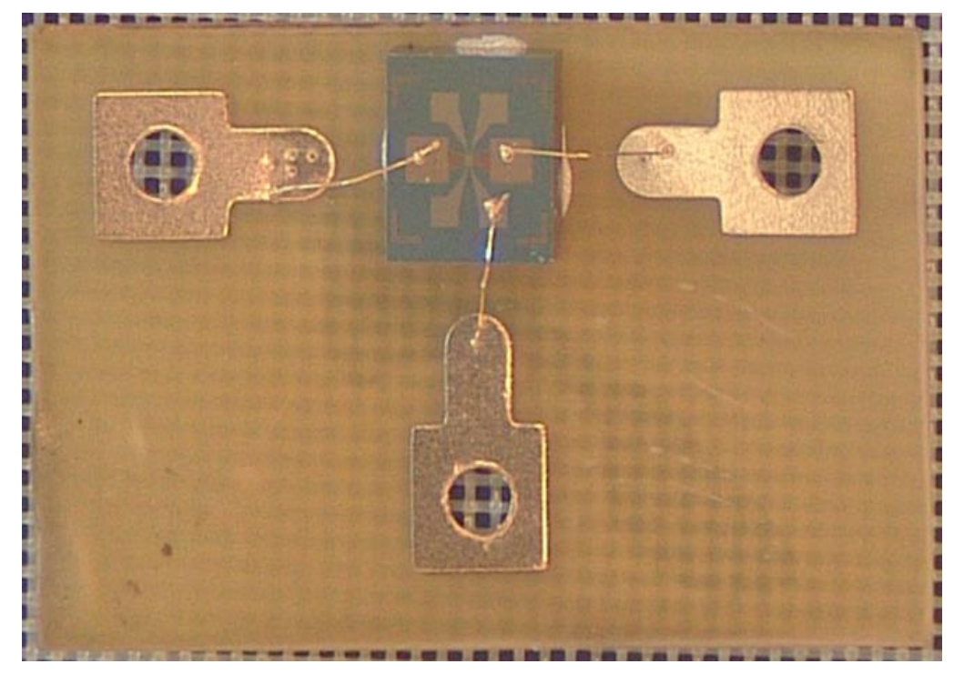
Graphene Field Effect Transistor

The GFET transistor employed in this study was fabricated by Graphenea and it is built with a channel measuring 50µm by 50µm and features a top-gated graphene structure. Its design closely resembles that of a conventional FET transistor, with the notable distinction of a graphene-based channel. The figure above represents the GFET stack structure with the pads at the very top providing access to the source, gate, and drain of the transistor.



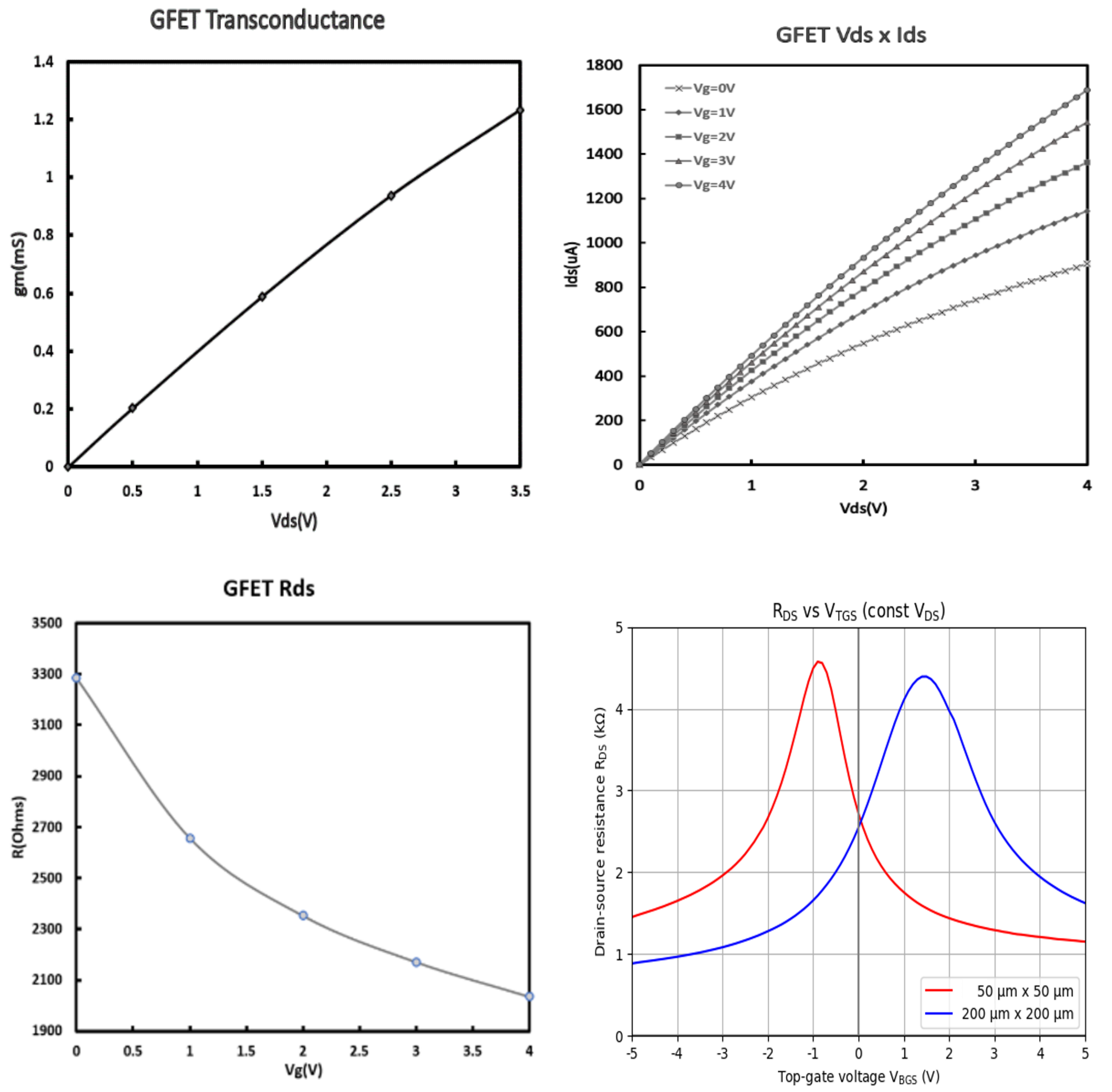
Wirbonded GFET with correspondent symbol.

GFET Characterization



The electric characterization of the transistor involved a thorough assessment of its behavior within the operational parameters required by the charge sensitive amplifier (CSA).

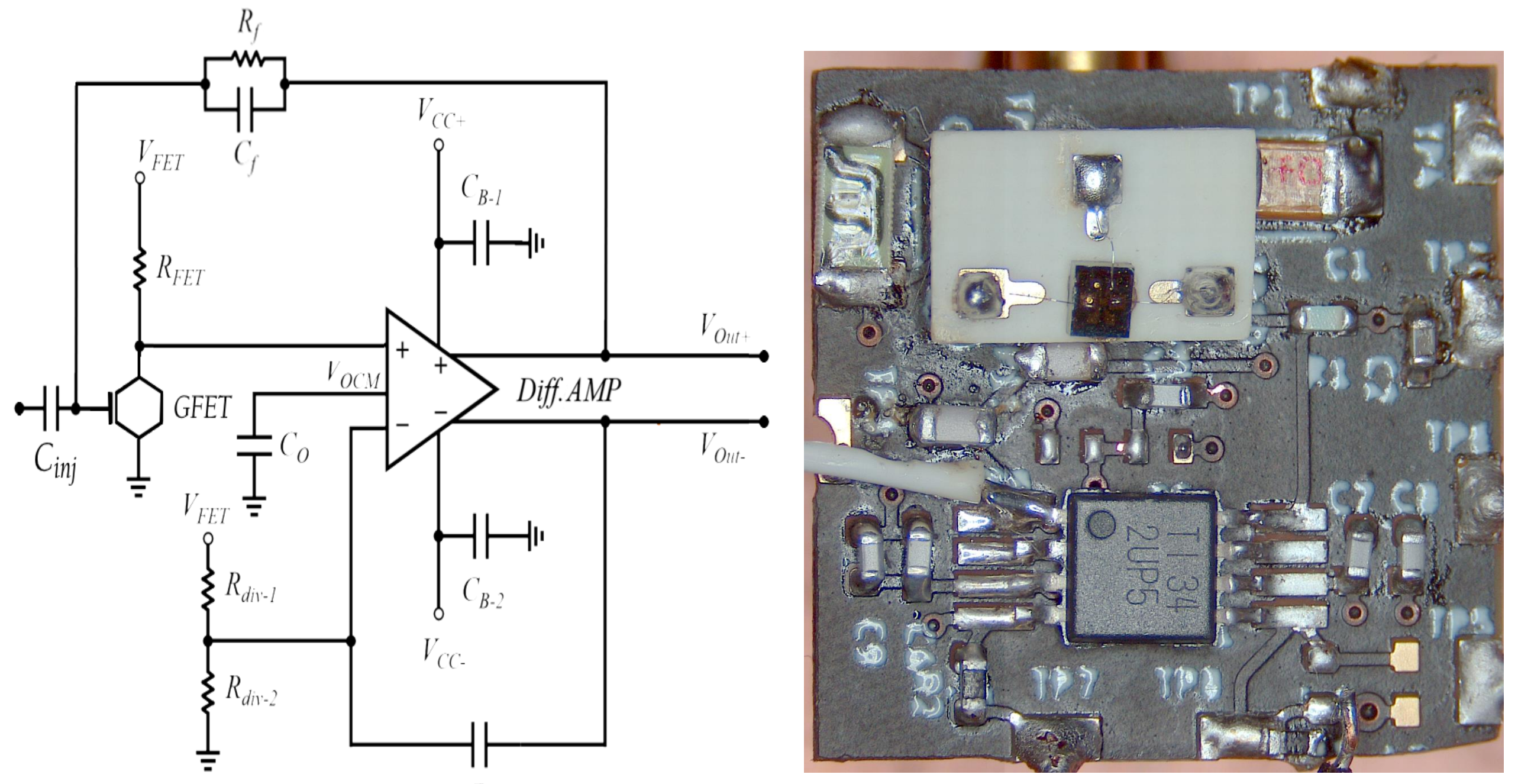
The drain-to-source voltage (Vds) spanned from 0 to 3.5V, while the gate-to-source voltage (Vg) was systematically varied from 0 to 4V. Across this operational range at room temperature, the transistor demonstrated its highest small signal transconductance (gm) reaching 1.24mS. The transconductance characterizes the transistor ability to amplify signals, making it a critical parameter for the charge amplifier developed in this work. A side effect of closely coupling the metal gate with the graphene channel through a thinner dielectric in this case aluminum oxide is the increase in the gate capacitance of the transistor.



Typical performance of the evaluated GFET with graphs illustrating its transconductance, IxV curves, and channel resistivity.

Charge Sensitive Amplifier

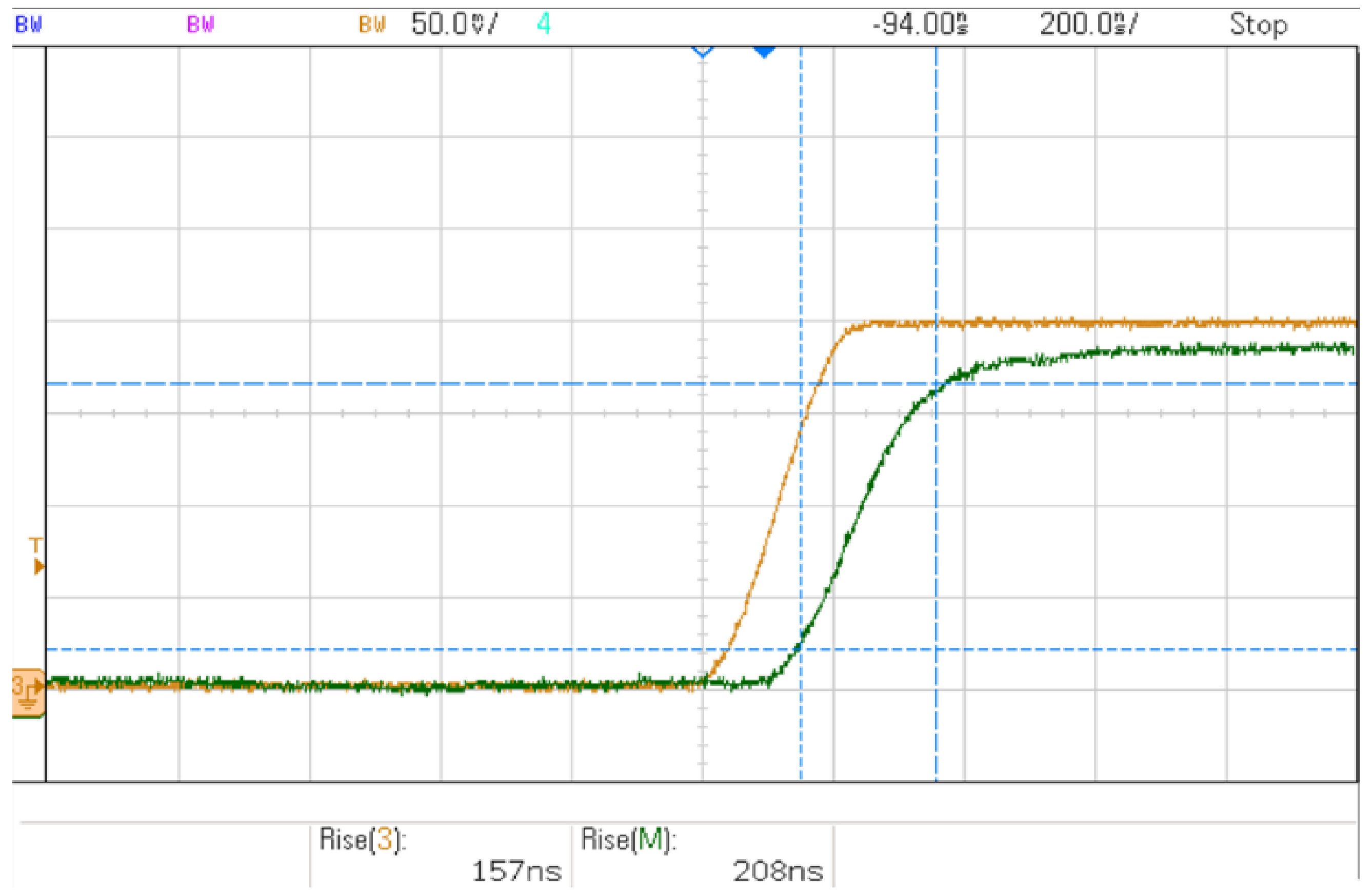
The GFET transistor was integrated with an operational amplifier, composing a charge sensitive amplifier. The inherent simplicity of its design, characterized by a minimal number of components, renders it particularly well-suited for applications in physics experiments requiring a low radioactive background. Integrated in the same substrate with the GFET to make the hybrid charge amplifier, is the fully differential Texas Instruments THS2630 operational amplifier.



This image shows the schematic circuit of the charge amplifier alongside its implemented design with the GFET is installed on the white interposer board.

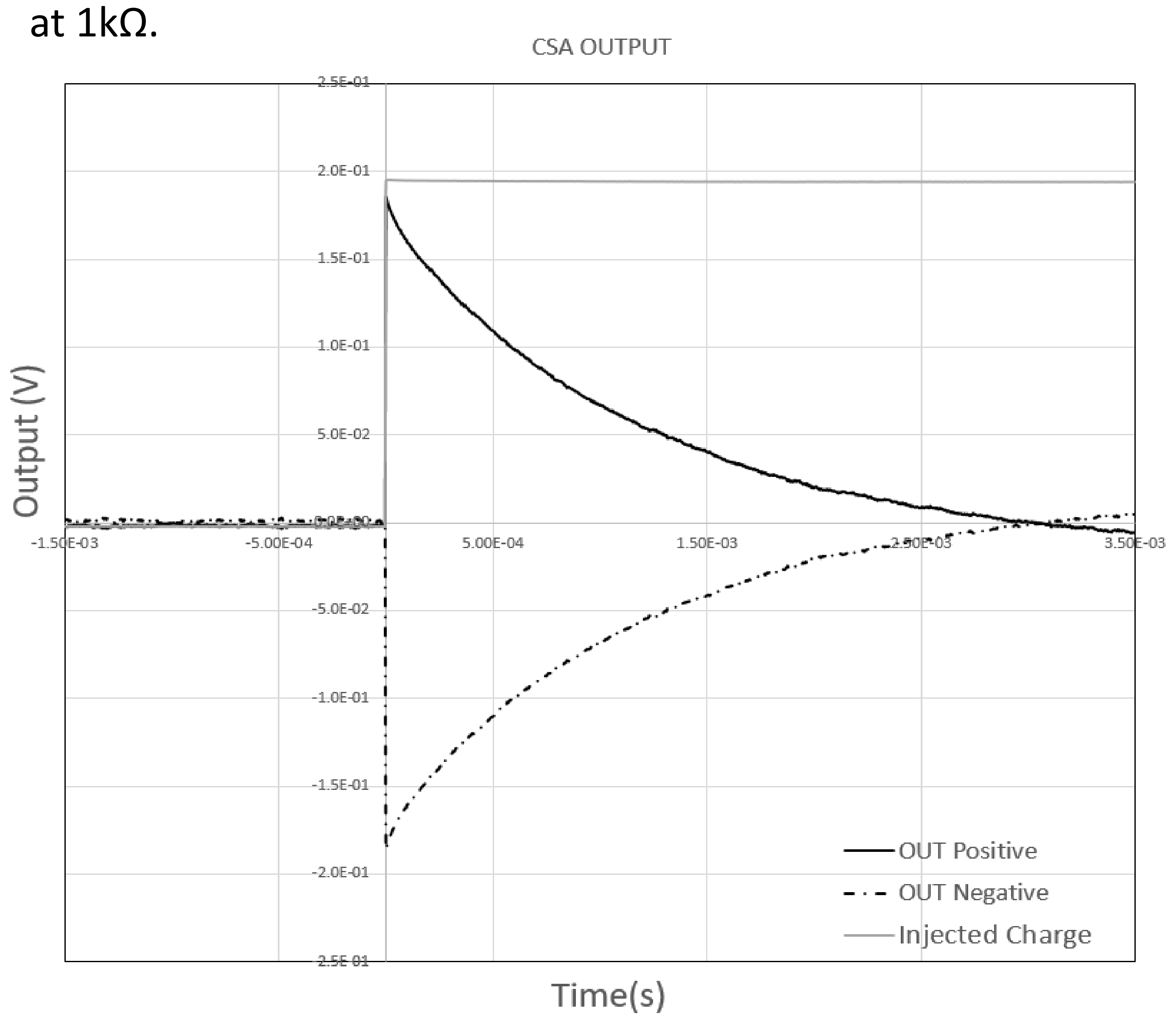
The preliminary characterization of the charge amplifier has substantiated the viability of employing GFETs for the construction of this kind of circuit. The initial characterization of this circuit was performed with a pulse injected through the 500fF injection capacitor (Cinj). This pulse, equivalent to a 1MeV charge deposition in HPGe, was utilized for the CSA evaluation. Operating under a bias of 1mA with a Vfet voltage set at 3V, the GFET-based charge amplifier exhibits a rising edge between 150ns and 210ns. This performance closely approaches that achieved by current amplifiers employed in prominent experiments such as Majorana and LEGEND 200, which typically exhibit rising edge responses in the range of 70ns to 120ns.

It is noteworthy that this represents a pioneering circuit, being the first of its kind to leverage a GFET as the front-end device. Notably, in this configuration, the GFET exclusively utilizes its top gate for operation.



Rising edge of the CSA (green) when excited with a 157ns pulse (orange).

The CSA differential output excels in common mode rejection. The feedback resistor (Rf) was selected at 10 GΩ ±5%, coupled with a feedback capacitor (Cf) of 500fF ±10%, resulting in a decay time of approximately 5ms. The GFET bias resistor is set at 1kΩ.



Differential output of the CSA for a 200mV pulse injection through a 500fF capacitor.

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