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Upgrade of Vertical Test Stand for 650 MHz Superconducting RF Cavities for CEPC

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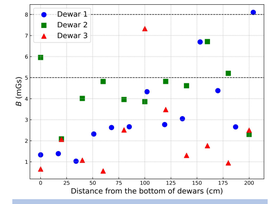
Abstract

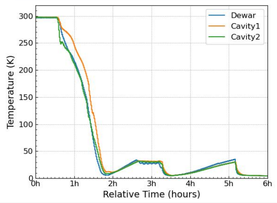
The vertical test stand (VTS) plays a crucial role in evaluating the performance of superconducting radio-frequency (SRF) cavities. The VTS at the Platform of Advanced Photon Source Technology R&D (PAPS) has been developed by the Institute of High Energy Physics (IHEP).The digitalization (based on FPGA) and integration functionalities of VTS was carried out, which simplified the vertical test and improved efficiency greatly. Several vertical tests have been conducted at this upgraded VTS successfully, which adopted digital self-excited loop (SEL) and EPICS.

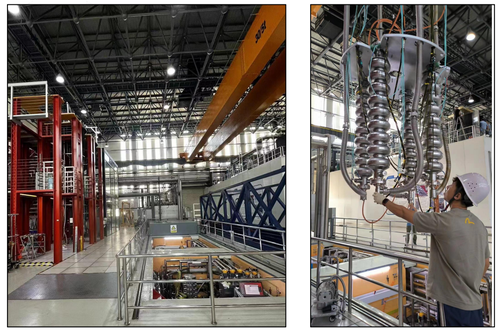
Upgrade of Cryogenic system

- The cryogenic system consists of vertical test dewars, phase separator, cryogenic heat exchanger, and JT valves, providing a cooling capacity of 300w at 2.0K.
- The VTS has three vertical test dewars, with two large dewars measuring 2.1 meters in diameter and 6.45 meters in depth capable of simultaneously testing five 1.3 GHz 9-cell SRF cavities. Testing up to 400 cavities per year
- All three vertical test dewars are equipped with magnetic shielding to maintain the ambient magnetic field around SRF cavities below 8 mGs
- Temperature sensors, magnetic flux gates, and radiation sensors are installed to monitor the status of SRF cavities.
- With the installation of four 1.3 GHz 9-cell cavities, thermal gradients inside the dewar can reach approximately 6 K/min



▲magnetic field inside the dewars

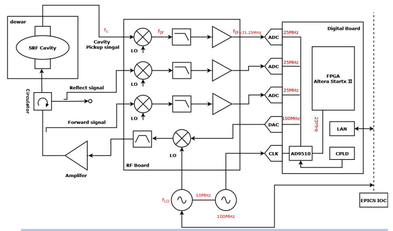




▲Photo of VTS & four 1.3 GHz 9-cell cavities installed for VT

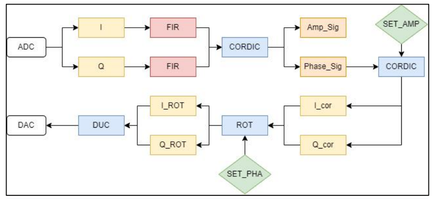
◄Cooling curve of a vertical test with four 1.3 GHz 9-cell superconducting cavities mounted.

Upgrade of RF system



▲►Schematic & photograph of digital SEL RF system

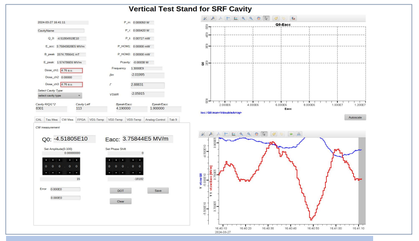
- The RF system consists of a RF front-end board and a digital signal processing board.
- One signal source provides a high-precision clock signal to the digital board, the other provides a LO signal to the up-down conversion system for measurements of different cavity types.
- The digital signal employs orthogonal IQ demodulation/modulation scheme with $f_{sample}/f_{IF}=5/4$.
- Implement phase shifting and amplitude limiting through internal digital algorithms in FPGA.



▲Algorithms in FPGA

GUI design and Error Analysis

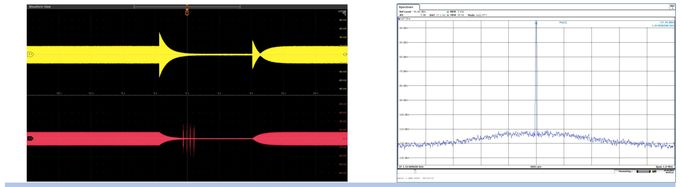
- Utilize EPICS to achieve DAQ, Q0-Eacc calculation, and data communication between cryogenic system and RF system.
- Design a GUI using CS-Studio Phoebus and establish a database in the host computer.
- Calculate measurement errors and display them using scripts.



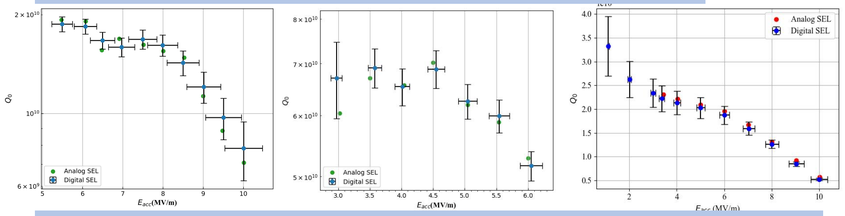
▲VTS OPI interface of CS-Studio Phoebus

Results of Vertical Test

- The upgraded test system was used to achieve self-excitation of superconducting cavities, and was employed in vertical tests of 324MHz, 650MHz, and 1.3GHz cavities. The test results of the digital system and analog system were in good agreement.



▲Waveform of the reflected and pickup signal with closed and open SEL



▲Comparison of vertical test results of 324MHz, 650MHz and 1300 MHz SRF cavity

Conclusion

- The upgraded vertical test station has three vertical test dewars, providing 300w@2K of cooling capacity, which can meet the testing needs of 400 cavities per year.
- Developed a digital vertical test system, including an RF front-end and digital signal processing system. Designed a GUI interface with database functionality and error analysis capabilities.
- Vertical tests of cavities at various frequencies were conducted using the new test system, and the digital test results matched well with the analog results.