Study of Surface Radiation Damage in Silicon Sensors

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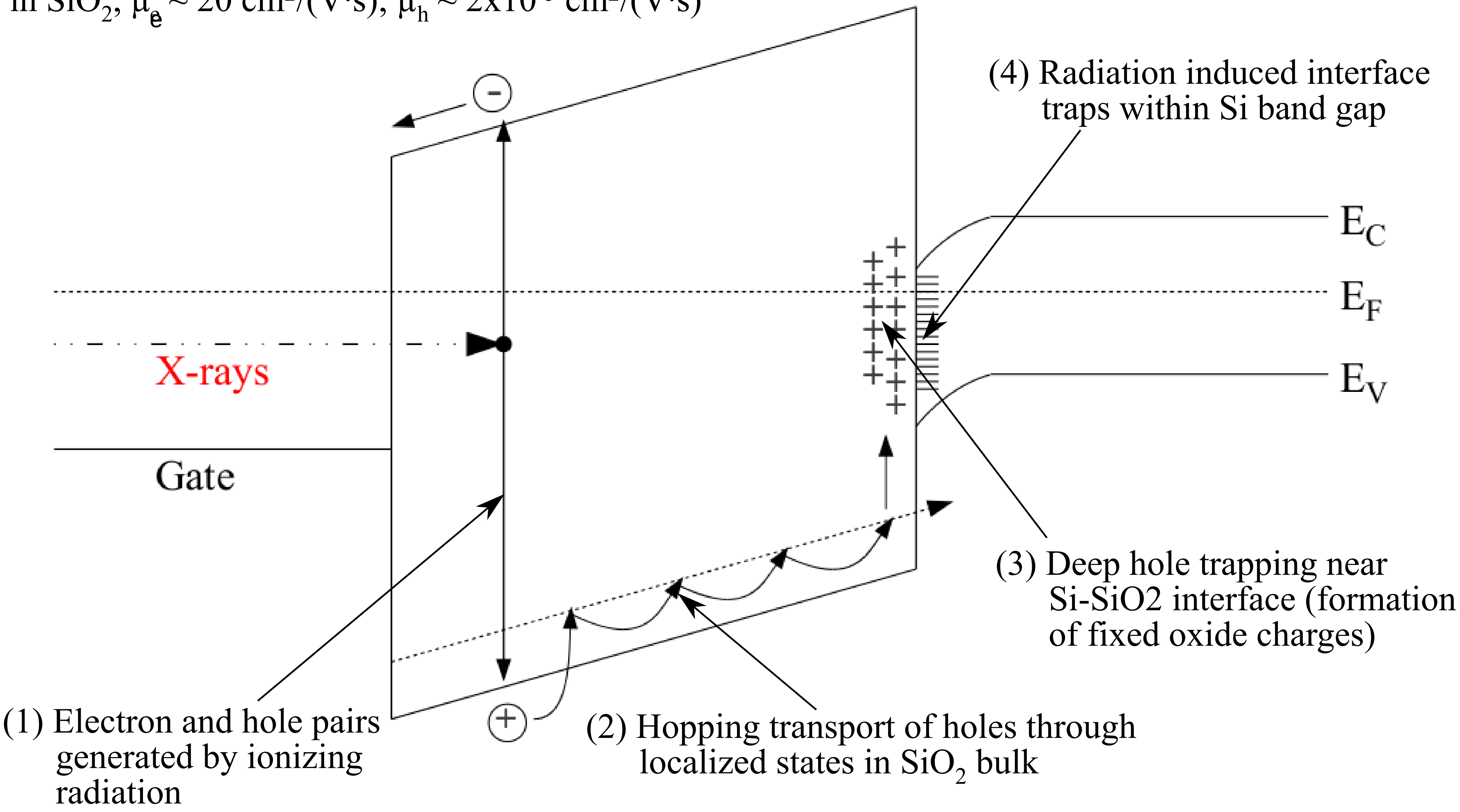
Outline

- Introduction
- Measurement techniques (TDRC, C/G-V)
- Determination of the concentration of defects
- Results:
    1) dose dependence of defects
    2) orientation dependence: <1 1 1> vs. <1 0 0>
    3) annealing kinetics of defects
- Influence on electric performance of segmented sensors
- Summary

Introduction to surface radiation damage

- **Formation of defects close to the Si-SiO_2 interface:**
  - Most electron-hole pairs recombine due to ionizing radiation
  - Electrons fastly escape from SiO_2; holes are much slower than electrons, finally get trapped near the interface: in SiO_2, $\mu_e \sim 20\ cm^2/(V\cdot s)$; $\mu_h \sim 2\times10^{-5}\ cm^2/(V\cdot s)$



(4) Radiation induced interface traps within Si band gap

(3) Deep hole trapping near Si-SiO2 interface (formation of fixed oxide charges)

(1) Electron and hole pairs generated by ionizing radiation

(2) Hopping transport of holes through localized states in SiO_2 bulk

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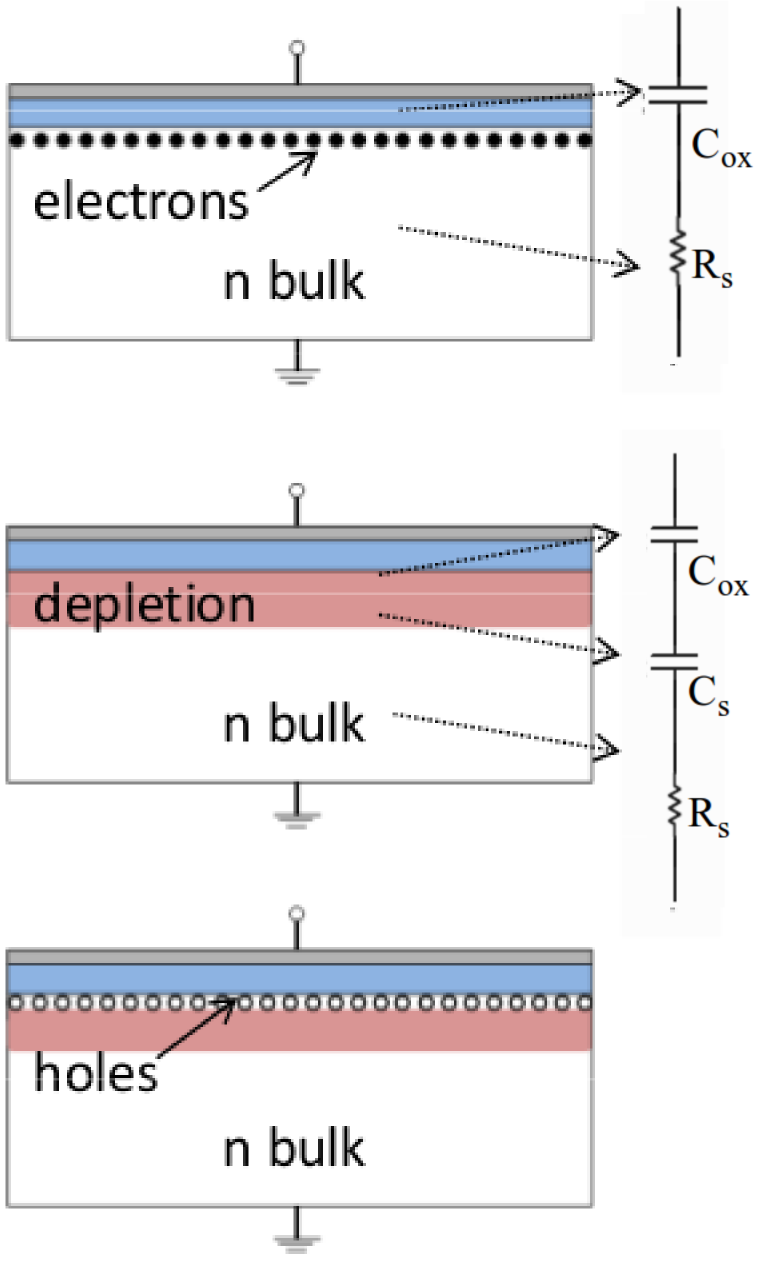
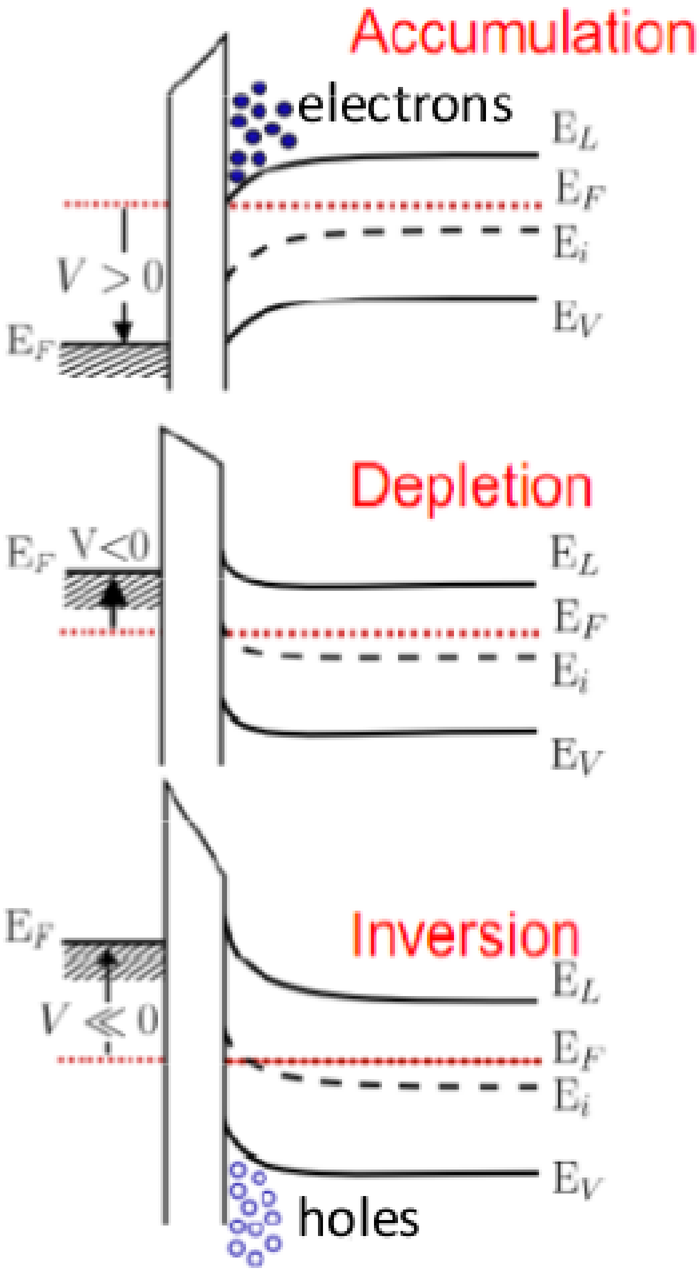
* from T.P. Ma and Paul V. Dressendorfer, "Ionizing Radiation Effects in MOS Devices and Circuits", WILEY 1989.

Introduction to the principles of MOS capacitor

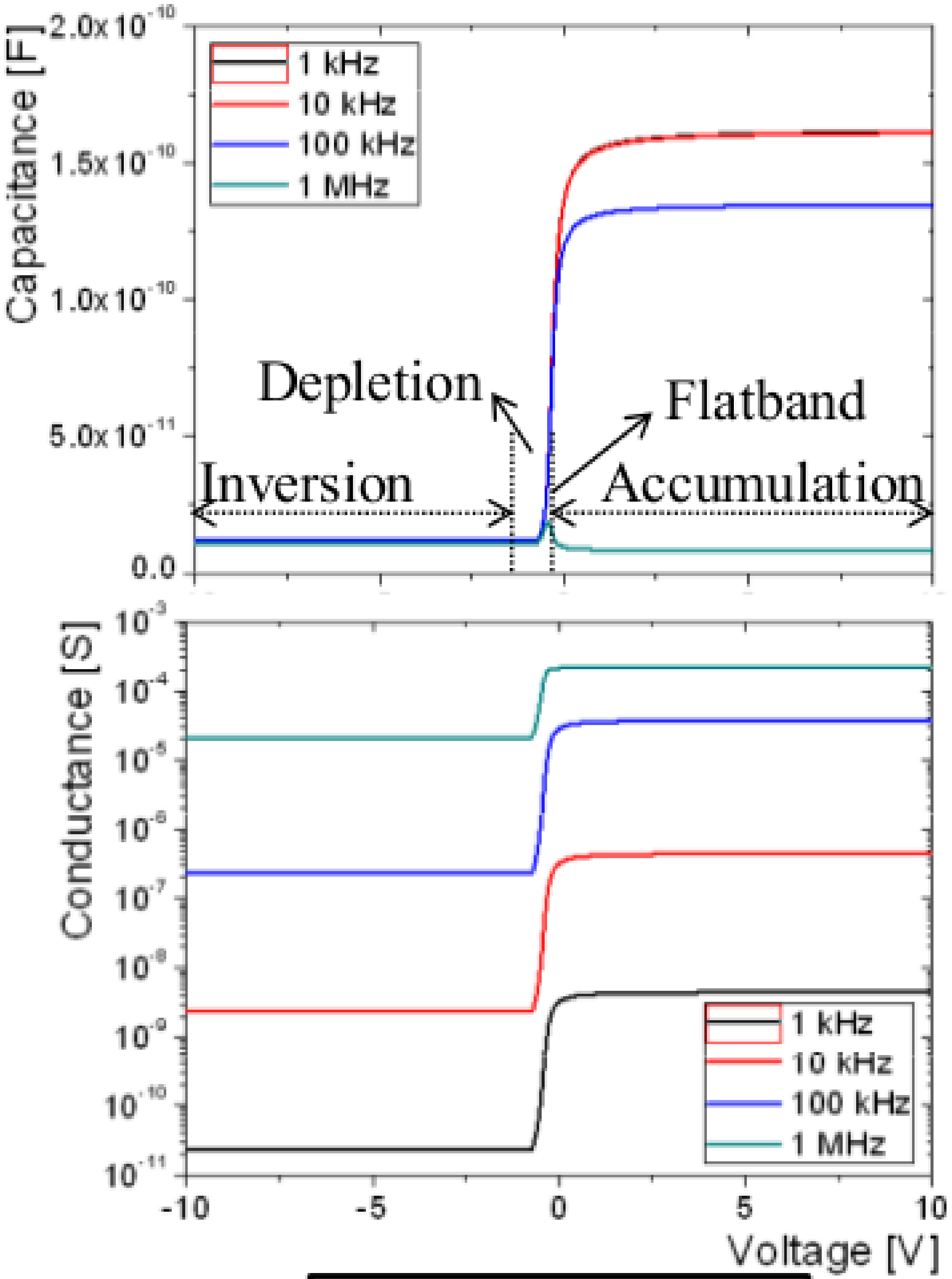
- **Ideal C/G-V curves (no bulk, interface traps or fixed oxide charges):**



MOS capacitor



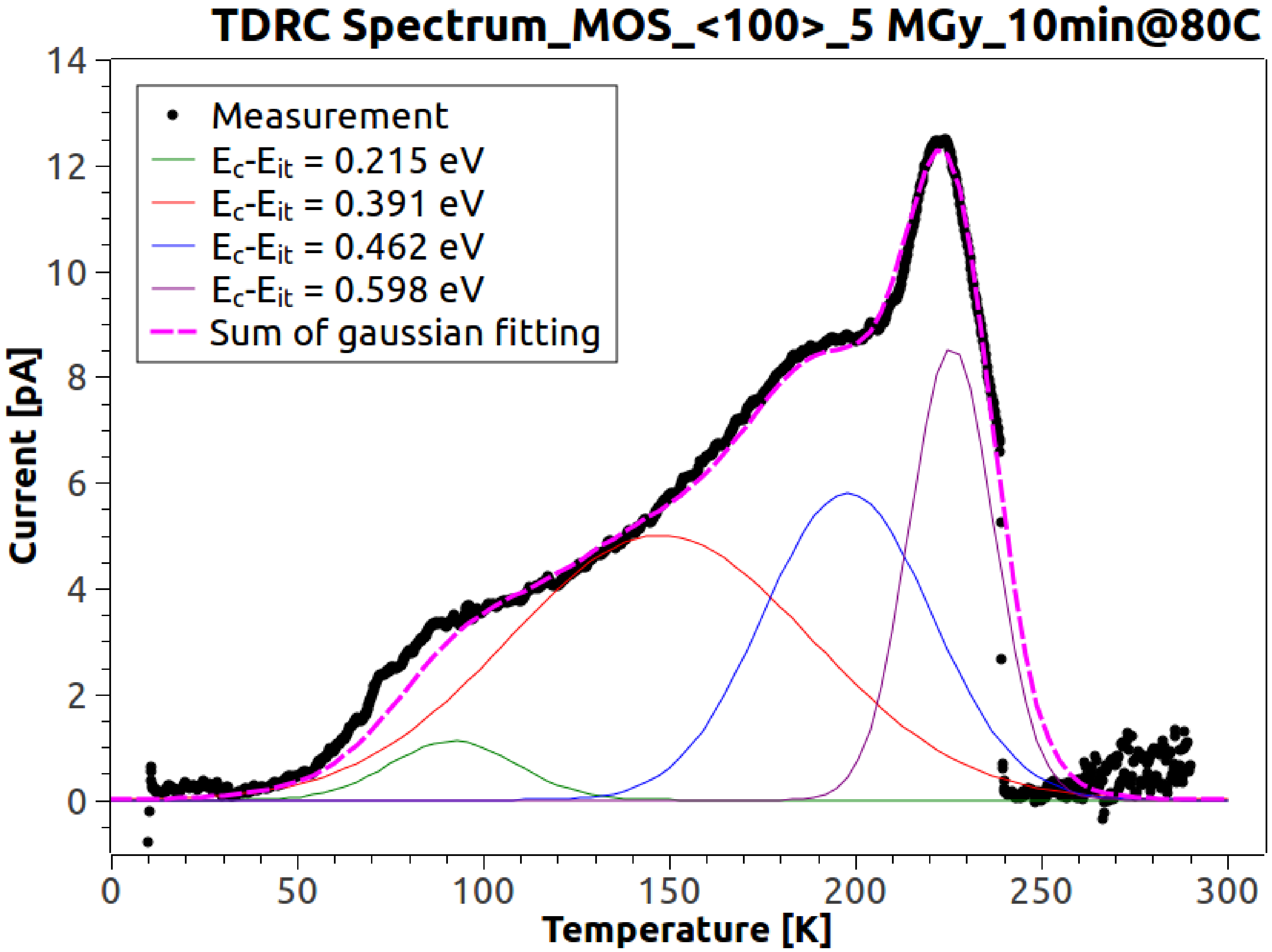
Energy band diagram



Ideal CV/GV curves

Measurement techniques: TDRC

- **TDRC (Thermally Dielectric Relaxation Current technique):**
  (TSC technique for bulk damage)



Procedures:

(1) Bias the MOS capacitor into strong accumulation → fill interface traps with electrons;

(2) Cool down the device to 10 K → freeze traps;

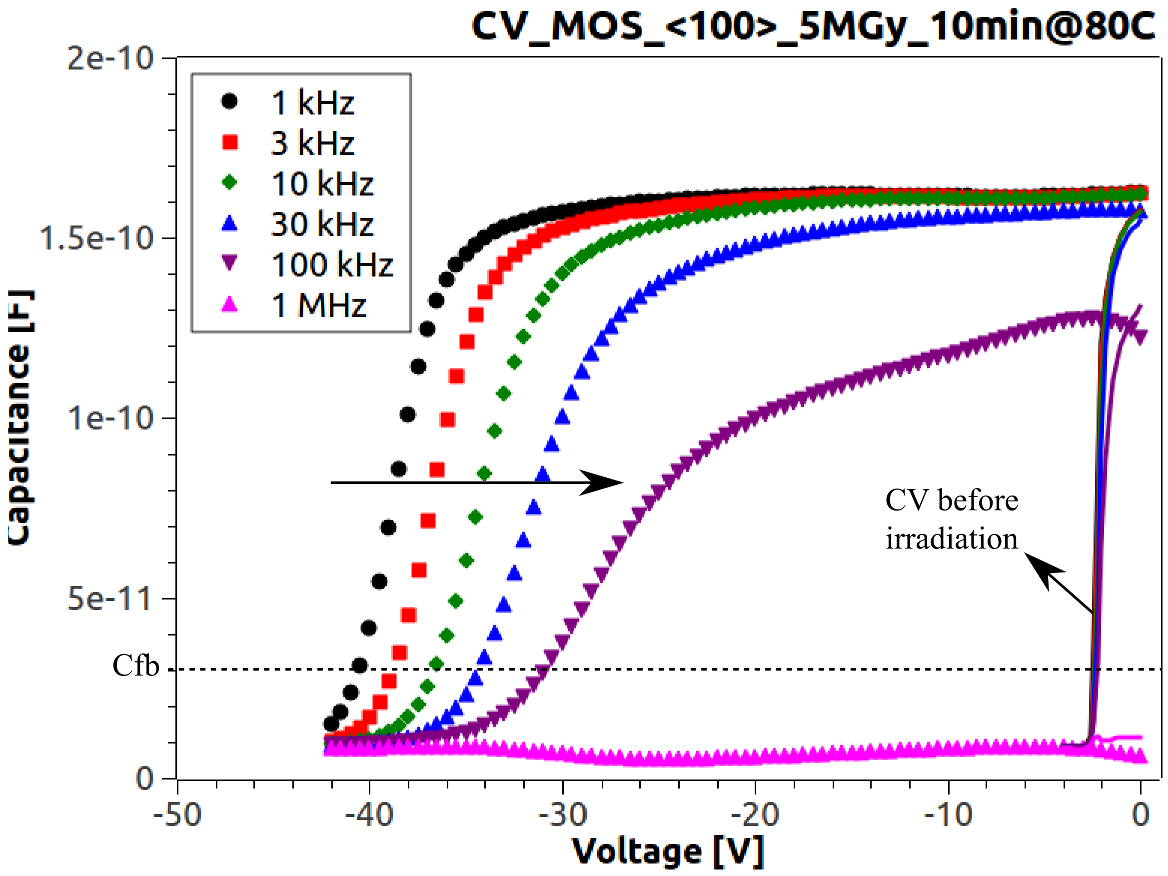
(3) Reverse* the bias and heating up the device till 290 K → trapped charges at Si-SiO_2 interface get released.

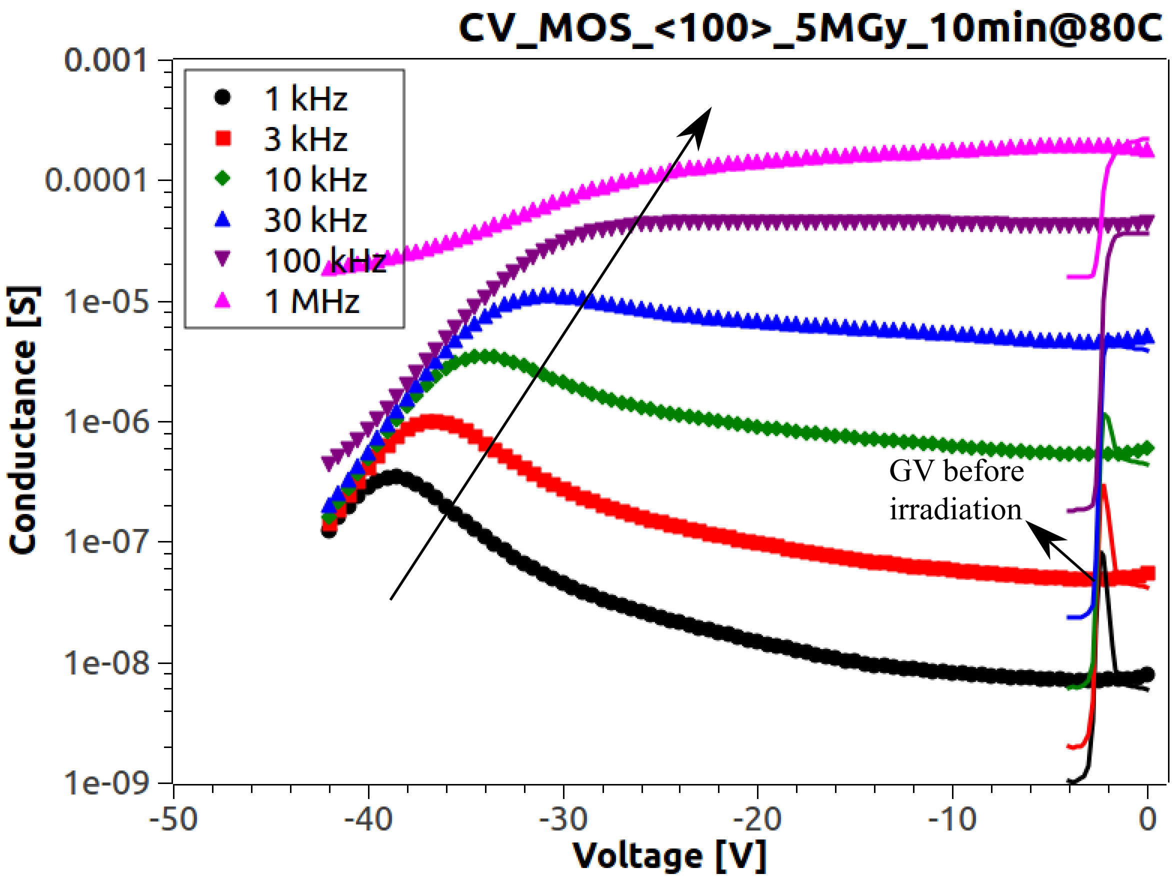
* Reverse bias should not put MOS capacitor into strong inversion (avoid border trap injection)

- Temperature [K] → Ec-Eit [eV]
  TDRC current [pA] → Dit [$cm^{-2}eV^{-1}$] $\xrightarrow{\text{integration of Dit}}$ Nit
- 3 dominant traps and 1 subordinate trap were used to describe the measured TDRC spectrum

Measurement techniques: C/G-V

· C/G-V (Capacitance-Voltage & Conductance-Voltage):





· Shift of flatband voltage ← fixed oxide charges + interface traps
· Frequency shift of C/G-V curves ← interface traps
· Increase of conductance in depletion ← interface traps

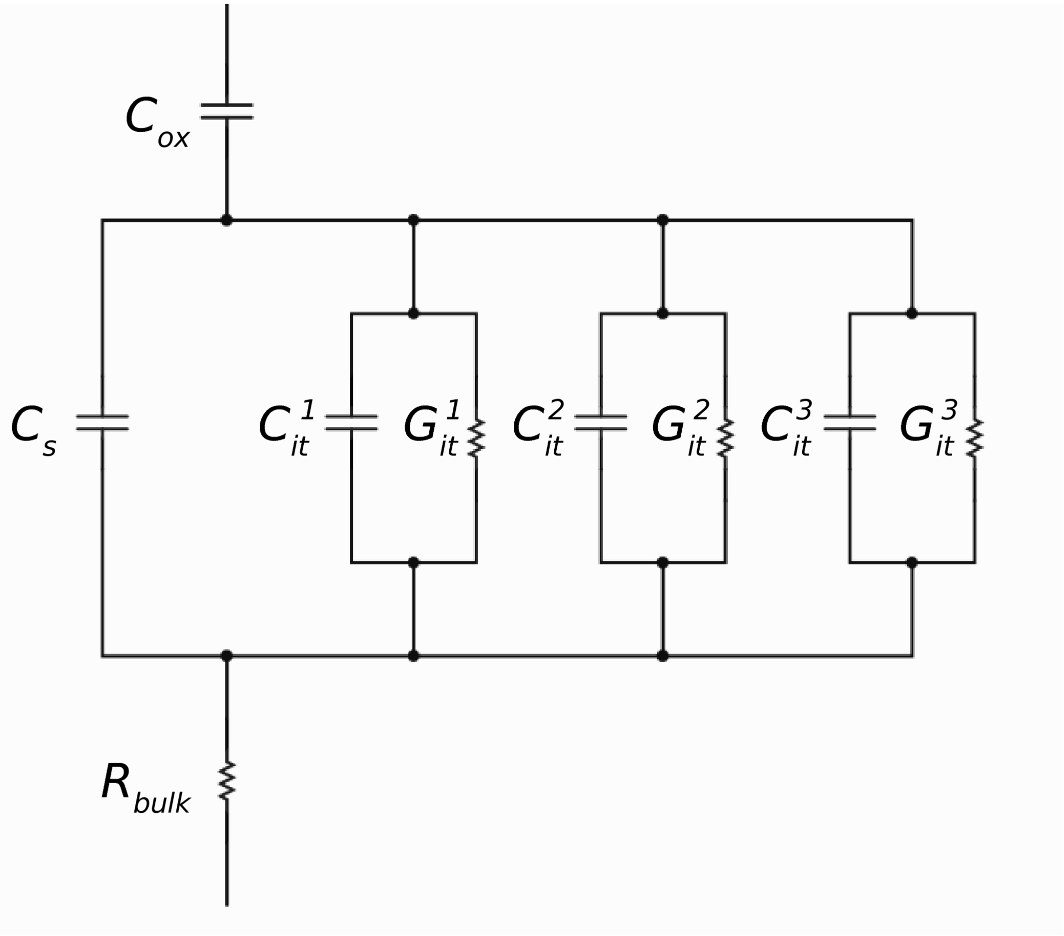
· Flatband capacitance C_{fb} after irradiation shows strong frequency dependence! It is difficult to determine fixed oxide charge density directly from the shift of flatband voltage.

Determination of the concentration of defects

· Simplified trap-included model for MOS capacitors:

- C_{ox}: oxide capacitance, ~ A_{gate}/d_{ox}.
- C_s (V_s): space-charge capacitance, is doping dependent.
  higher N_d → higher C_s
- C_{it} (V_s, $D_{it}(E_{it})$,f): interface trap capacitance
  G_{it} (V_s, $D_{it}(E_{it})$,f): interface trap conductance
  higher D_{it} → higher C_{it} & G_{it}
  higher f → lower C_{it} & G_{it}
- R_{bulk}: series resistance from bulk doping, ~ $1/N_d$.
- Relation between V_g and band bending V_s:

$$V_g\left(V_s\right) = V_s + \varphi_{ms} \boxed{- \frac{q_0 N_{ox} A}{C_{ox}}} - \frac{Q_{si}\left(V_s\right)}{C_{ox}} - \frac{Q_{it}\left(V_s\right)}{C_{ox}}$$

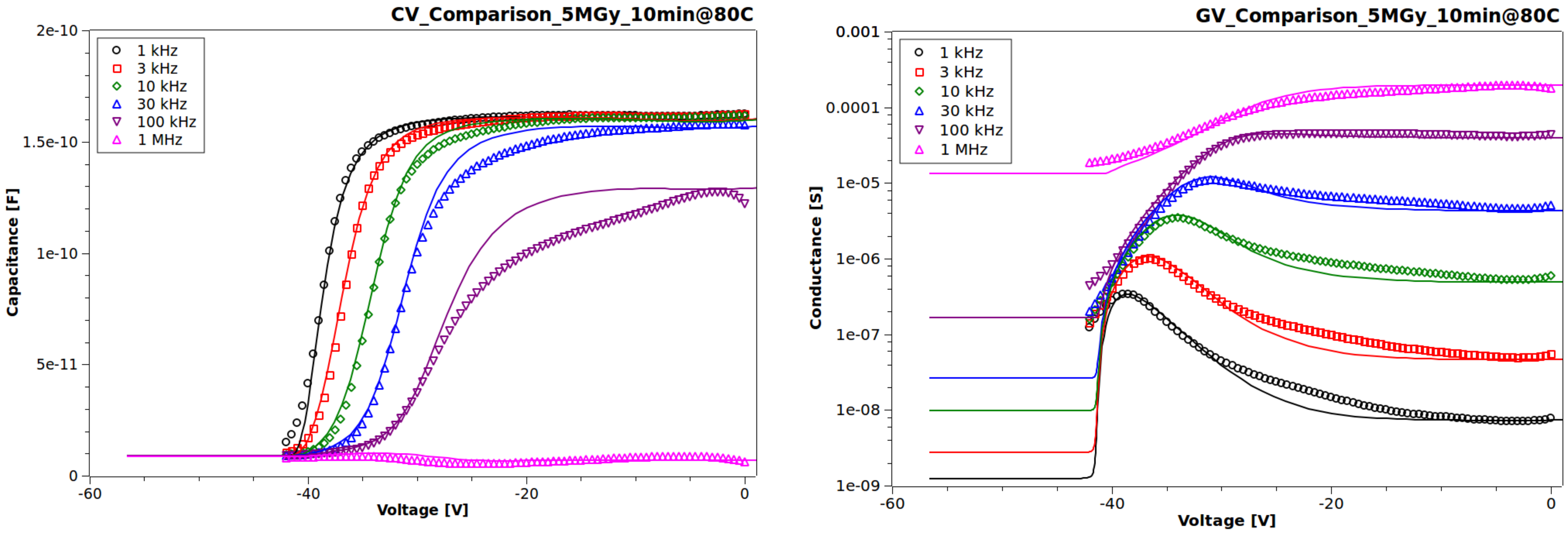


From the model, it can be concluded that:

1) interface traps contribute to C_{it} and G_{it} (change slope & cause frequency shift of measured C/G-V curves), and shift the curves.
2) fixed oxide charges only shift the entire C/G-V curves to lower voltage.

Determination of the concentration of defects

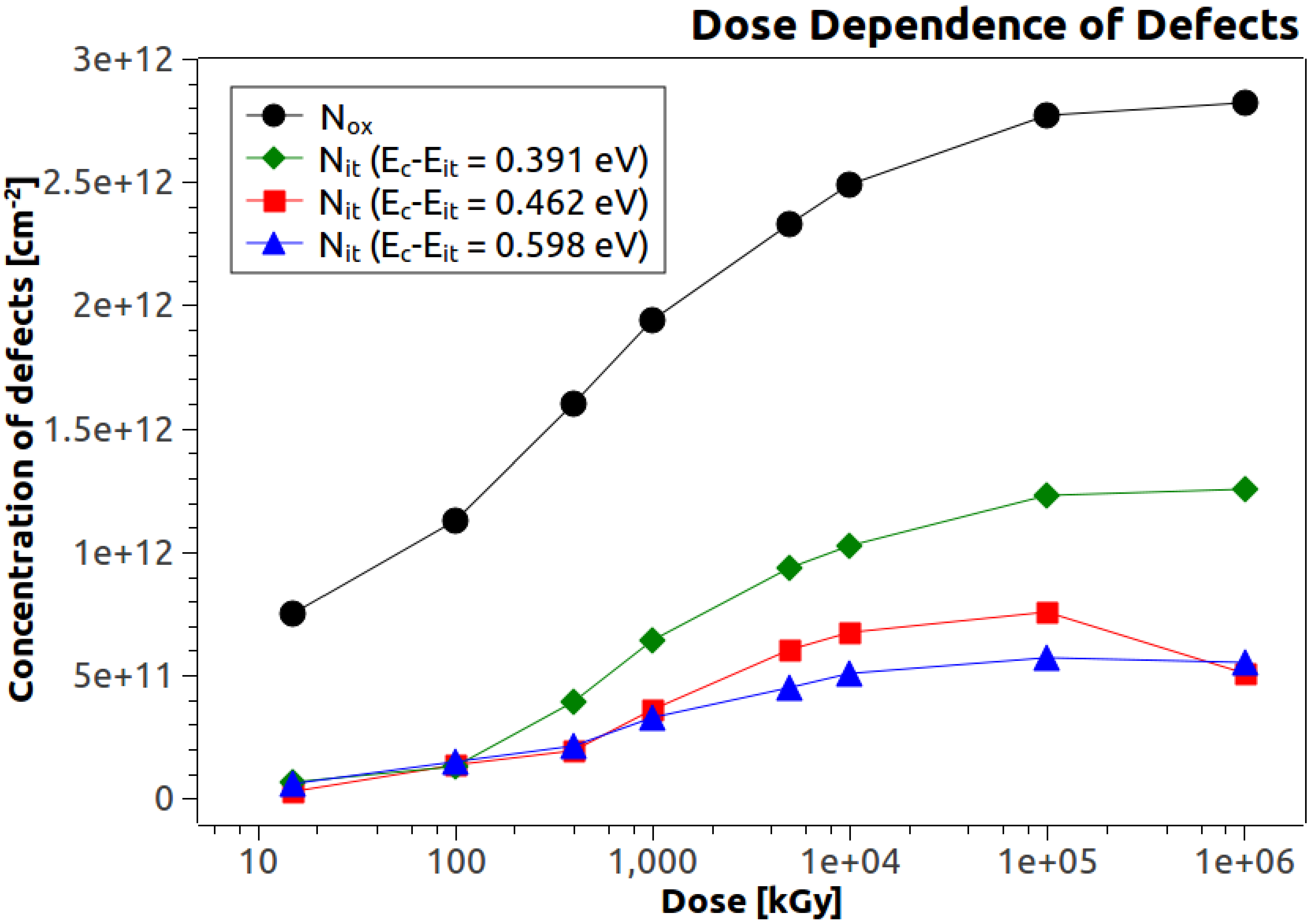
- **Model calculation to reproduce measured C/G-V curves:**
  - TDRC spectrum as an input for D_{it} in the program, all interface traps were assumed to be acceptor like.
  - Capture cross sections for the interface traps were evaluated by measuring TDRC spectrum with different heating rates:
    $\sigma (E_c\text{-}E_{it}=0.391\text{eV})=1.2\times10^{-15}\ \text{cm}^2$, $\sigma (E_c\text{-}E_{it}=0.598\ \text{eV}) =6\times10^{-16}\ \text{cm}^2$, $\sigma (E_c\text{-}E_{it}=0.462\ \text{eV}) =2.5\times10^{-17}\ \text{cm}^2$
  - C/G-V curves were calculated and compared to measurements



- Fixed charge density was determined when model calculation reproduce measurement curves!

Results: dose dependence of defects

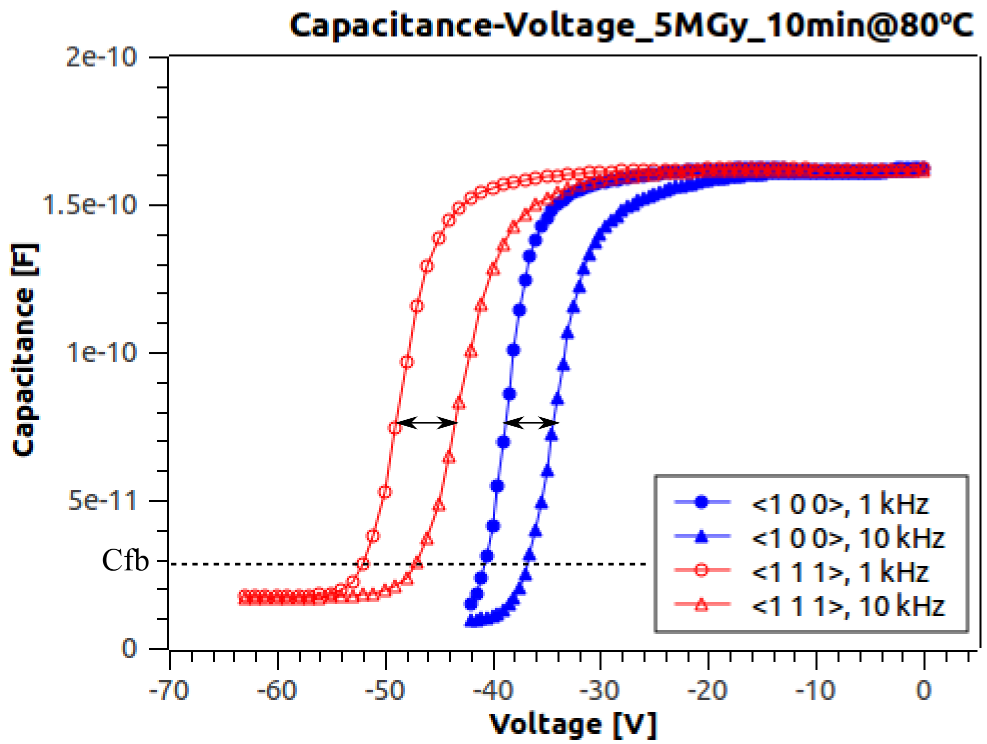
- **Dose dependence of a MOS capacitor with <100> orientation:**

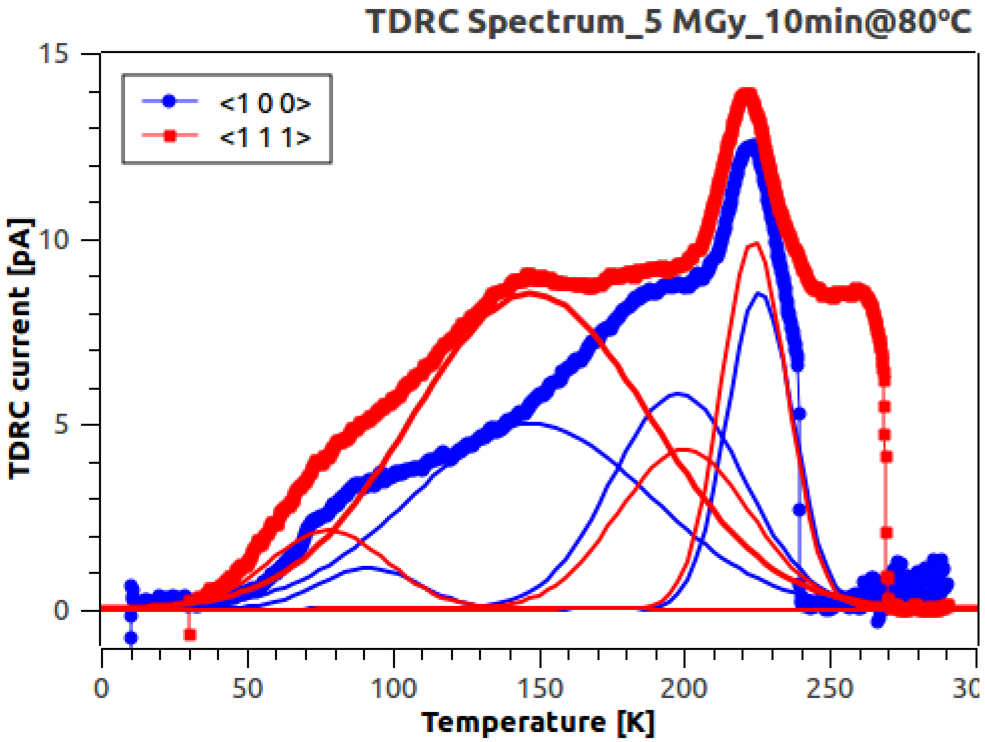


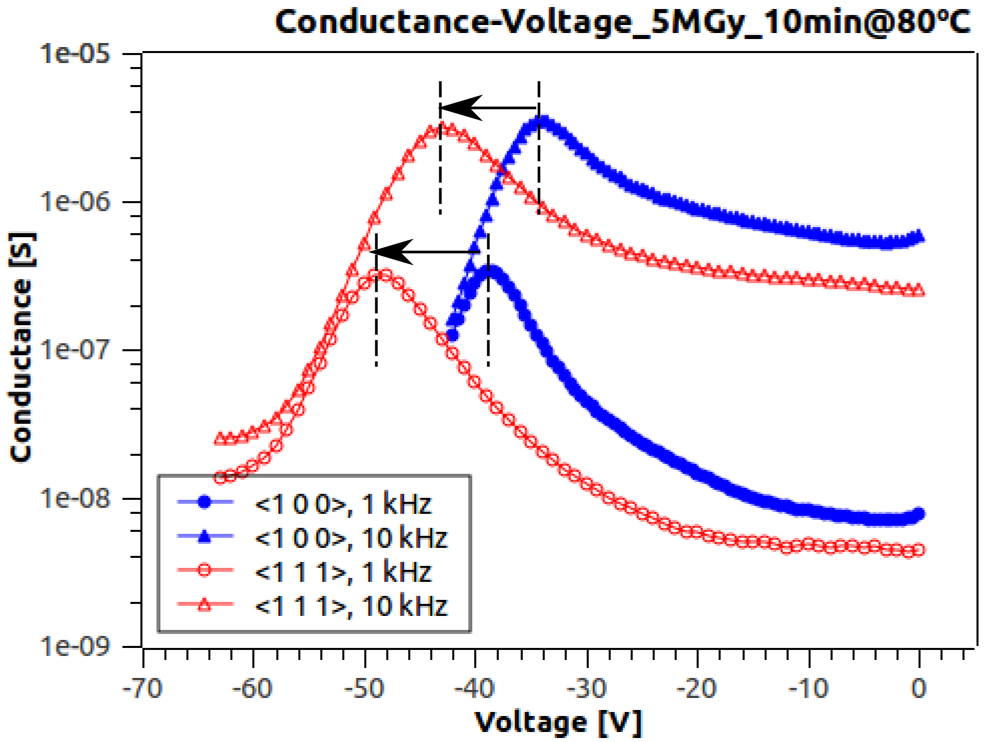
- Measurements were done after 10min@80C annealing to stablize properties of sensors.
- N_{ox} and N_{it} saturate at a dose value in between 10 MGy and 100 MGy.
- Saturation value of N_{ox} is 2.8×10^{12} cm^{-2}.

Results: orientation dependence

- **<1 0 0> vs. <1 1 1>: results for 5 MGy after 10min@80 ºC annealing.**
  - From TDRC spectrum, density of interface traps close to conductance band from <1 1 1> is larger than that from <1 0 0>: $N_{it}^{<111>} > N_{it}^{<100>}$.
  - The capacitor with orientation <1 1 1> shows larger frequency shift → confirms the increase of shallow traps.
  - Shift of C/G-V curves → indication of increase of fixed oxide charges? (Yes if traps are acceptor-like, BUT the types of interface traps can not be determined from C/G-V and TDRC measurements)

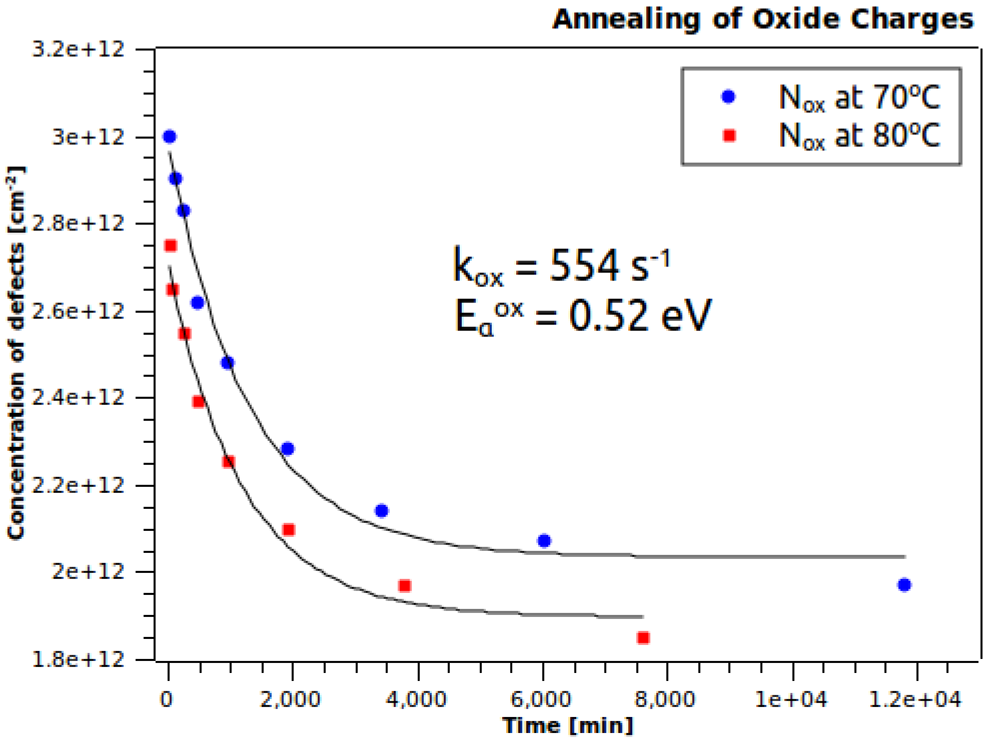


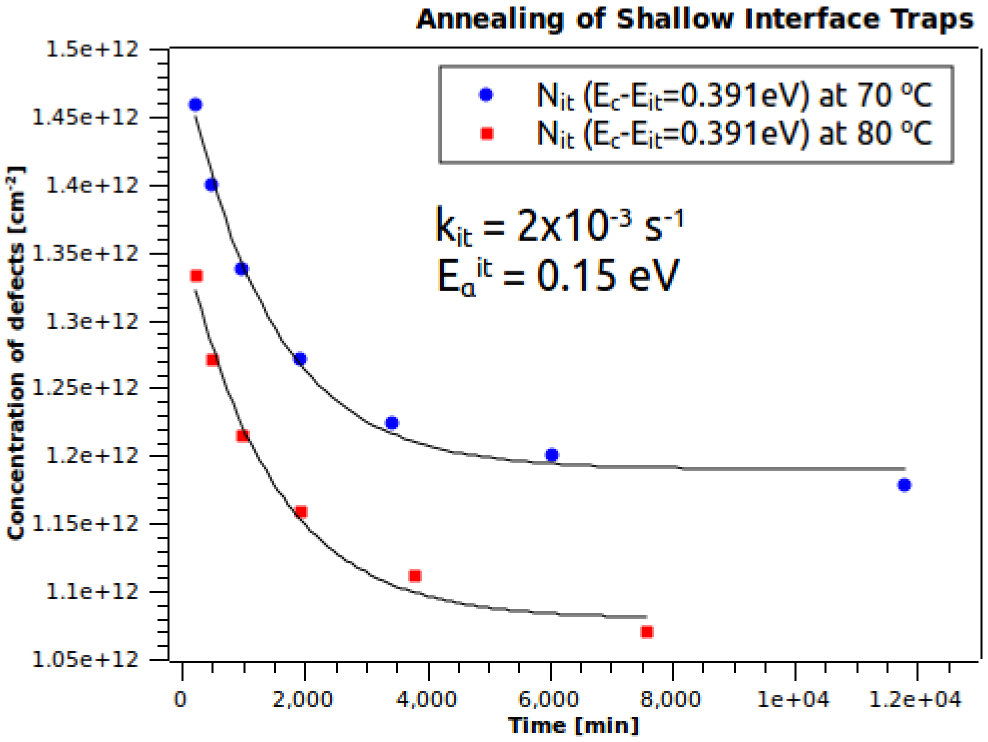




Results: annealing kinetics of defects

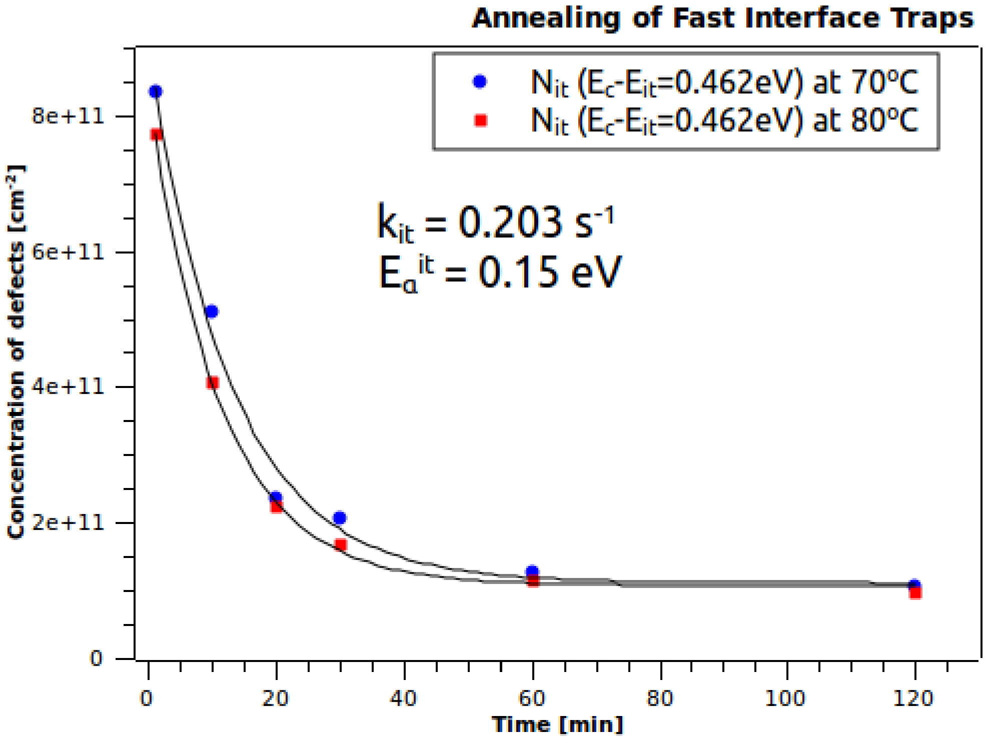
- **Annealing study for a MOS capacitor <1 1 1> after 5 MGy irradiation:**

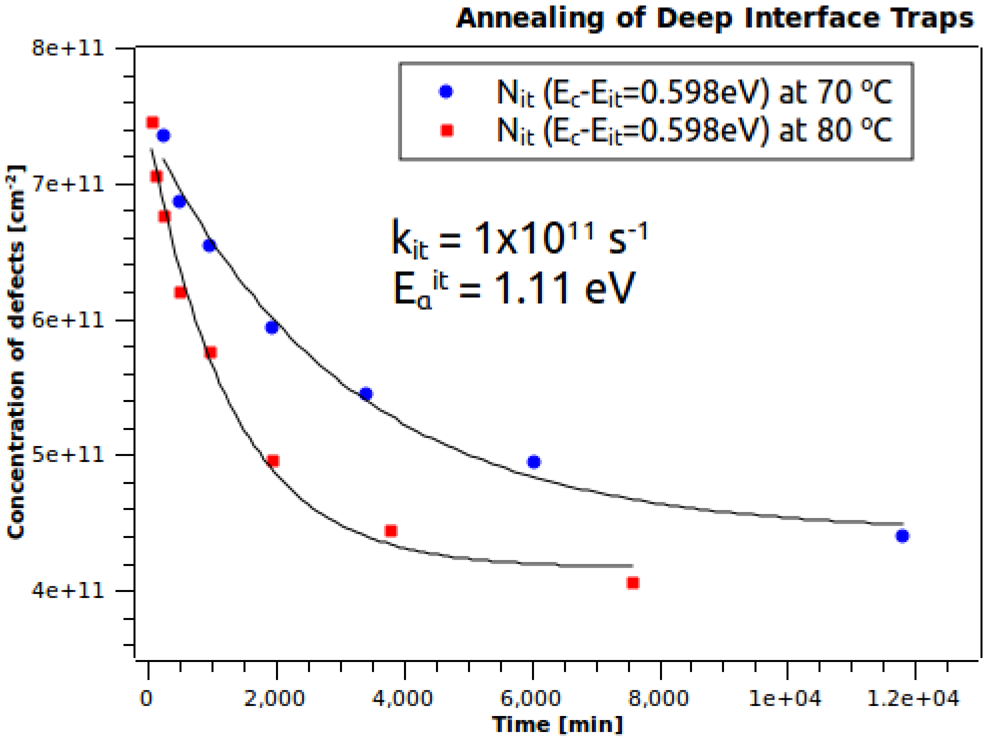




τ at 80°C:

N_{ox} : 13 hours
$N_{it}^{0.391eV}$: 19 hours
$N_{it}^{0.462eV}$: 11 min
$N_{it}^{0.598eV}$: 19 hours





- Short time annealing at higher temperature is needed to stablize performance of the sensor (remove the effects due to fast annealing of interface traps at 0.462 eV).

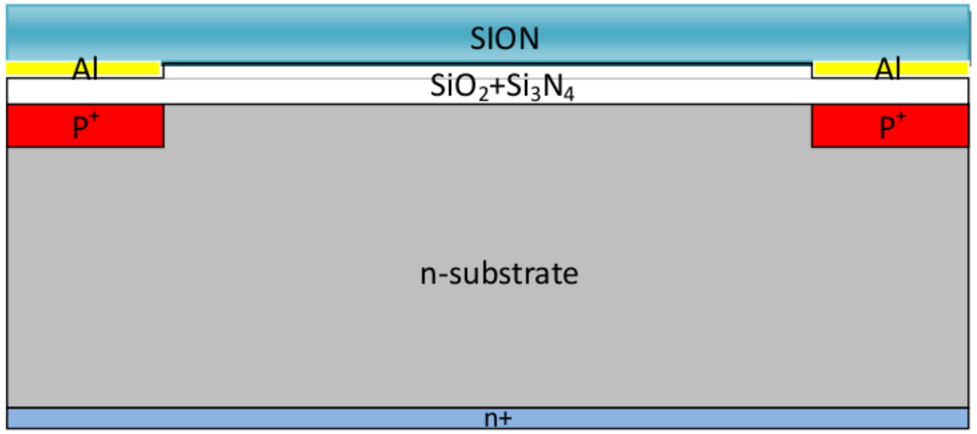
Influence in electric performance of segmented sensors

· CiS p-on-n microstrip sensors (Capacitance-Voltage behavior):

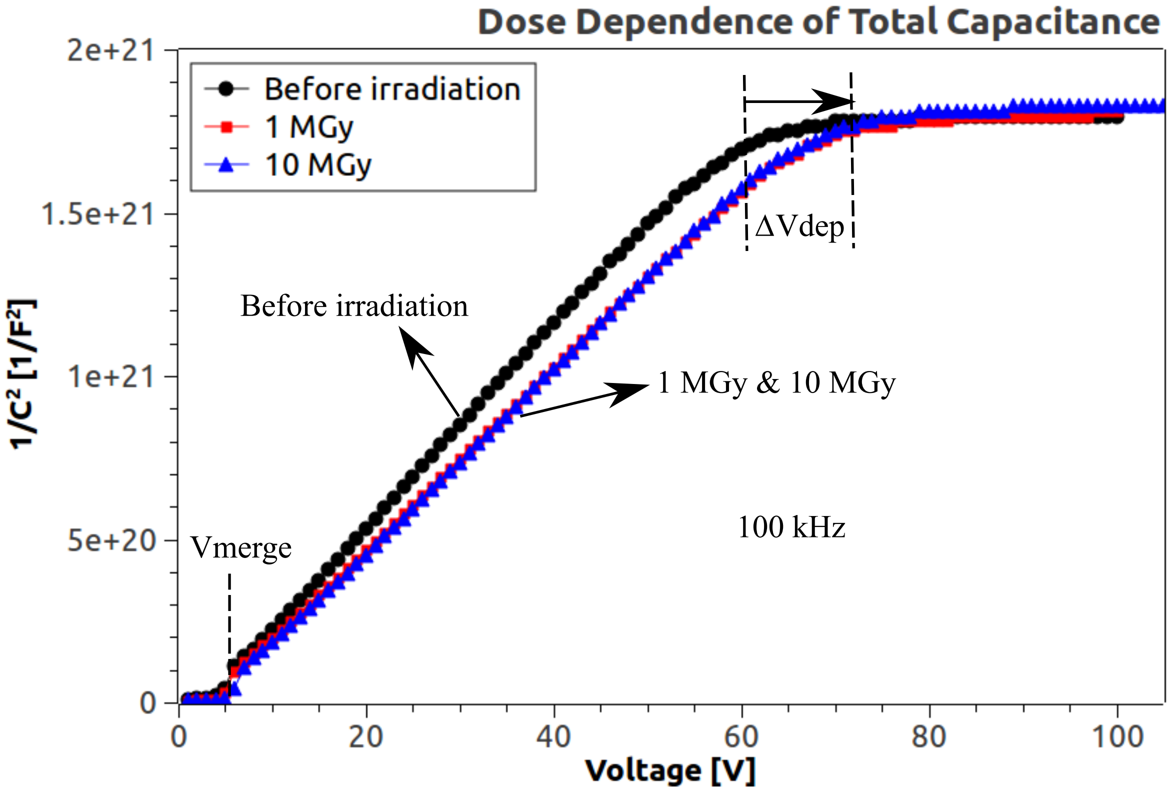
· Sensor's thickness: 285 μm · Orientation: <100>

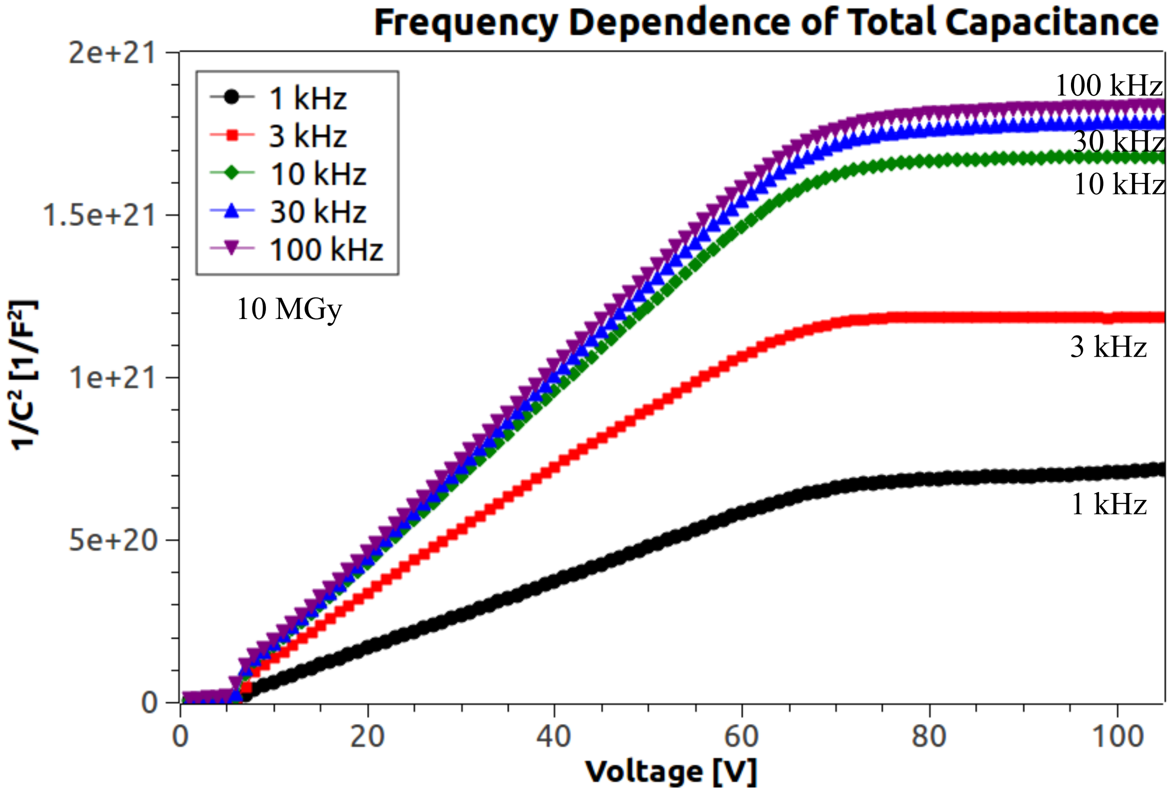
· Pitch: 80 μm · Gap: 62 μm

· Oxide: 200 nm/300 nm SiO_2 + 50 nm Si3N4



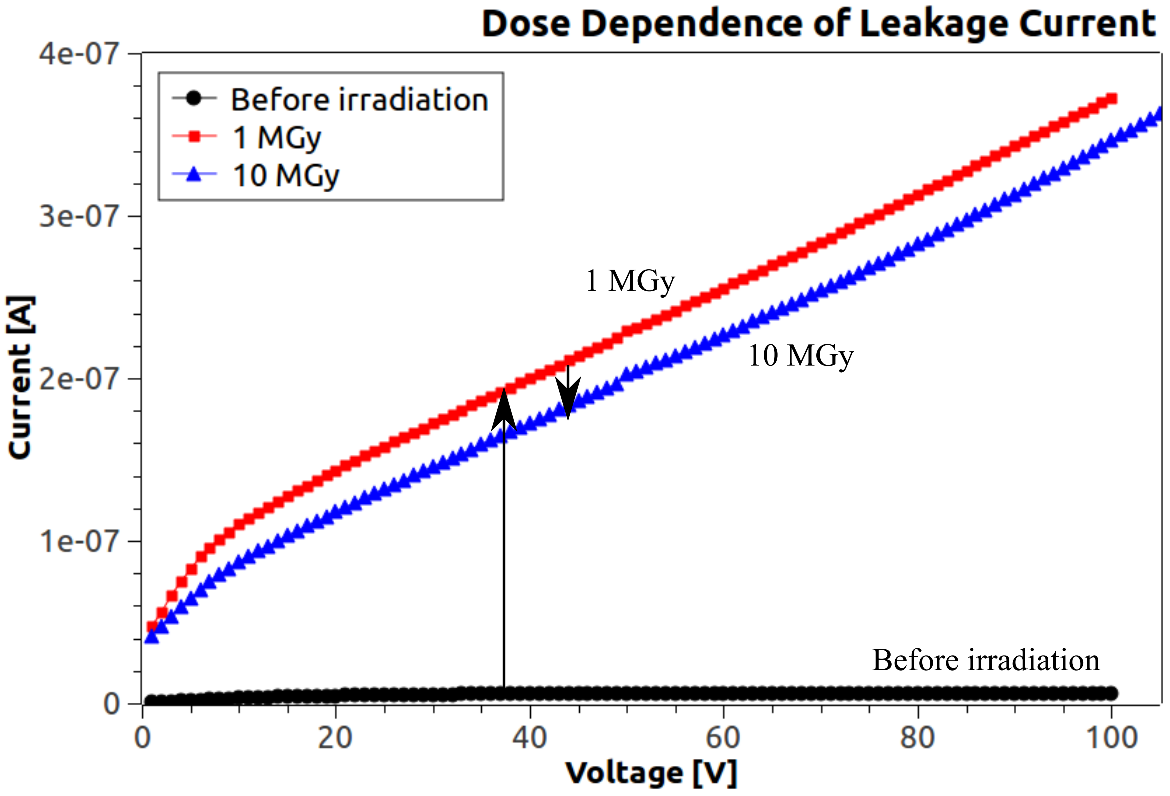
- At ~ 6 V, space charge region below each strip merges into together.
- Due to the presense of surface charges at the Si-SiO_2 interface, full depletion voltage V_{dep} increases about 10 V after irradiaitons (not due to change of doping).
- From simulation, it was observed that increase of full depletion voltage ΔV_{dep} saturates at a value of fixed oxide charge density ~ 3-5×10^{11} cm^{-2}.
- Interface traps are responsible for the frequency dependence of total capacitance.

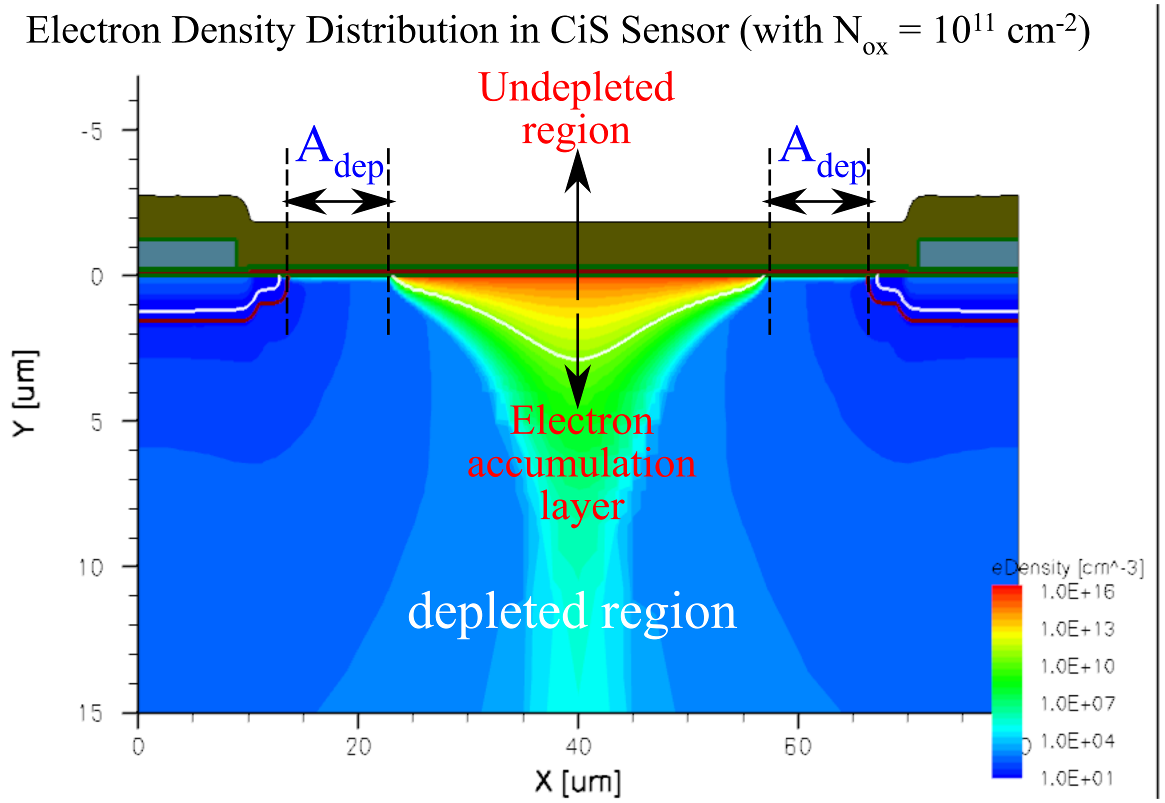




Influence in electric performance of segmented sensors

- **CiS p-on-n microstrip sensors (Current-Votlage behavior):**
  - $I_{leakage} = I_{bulk} + I_{surface}$;
  - I_{bulk} dependes on depleted volume of silicon sensor and life time of charge carriers in bulk;
  - $I_{surface}$ is propotional to interface trap density N_{it} × depleted area A_{dep} at the Si-SiO$_2$ interface.





- Increase of $I_{leakage}$ after irradiations ← interface trap density N_{it};
- "Linear" increase of $I_{leakage}$ with bias voltage ← depleted area A_{dep} at the Si-SiO$_2$ interface;
- Decrease of $I_{leakage}$ with irradiation doses
  ← increasing positive charges at the interface surpress the depleted area A_{dep};

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* A value of 8 µA/cm2 from irradiated microstrip sensor compatible with previous measurements on gated diode.

Summary

- N_{ox} and N_{it} were determined as function of dose: all defects density saturates at ~ 10-100 MGy.

- Annealing studies were performed at 70 ^{O}C and 80 ^{O}C; frequency factors and activation energies of different defects were derived.

- Comparison between two irradiated MOS capacitors with different orientations was made. The densities of interface traps close to conductance band show significant difference.

- Irradiations for $p^{+}n$ microstrip sensors and $n^{+}n$ pixel sensors were done; electric properties were characterized for different doses and understood by the study from MOS.

Thanks for your attention!

Backup

Determination of the concentration of defects

Simplified trap-included model for MOS capacitors:

- C_{ox}: oxide capacitance

$$C_{ox} = \epsilon_{SiO_2}\epsilon_0 \frac{S}{t_{ox}}$$

- C_s: space-charge capacitance

$$C_s\left(V_s\right) = \begin{cases} \frac{C_{FBS}\cdot\frac{V_s}{|V_s|}\cdot\left[\exp\left(\frac{q_0V_s}{k_0T}\right)-1\right]}{\sqrt{2\left[-\frac{q_0V_s}{k_0T}-1+\exp\left(\frac{q_0V_s}{k_0T}\right)\right]}} & \frac{q_0V_s}{k_0T} > v_m \\ \frac{C_{FBS}\cdot\frac{v_m}{|v_m|}\cdot[\exp(v_m)-1]}{\sqrt{2[-v_m-1+\exp(v_m)]}} & \frac{q_0V_s}{k_0T} \leq v_m \end{cases}$$

- C_{it}: interface trap capacitance

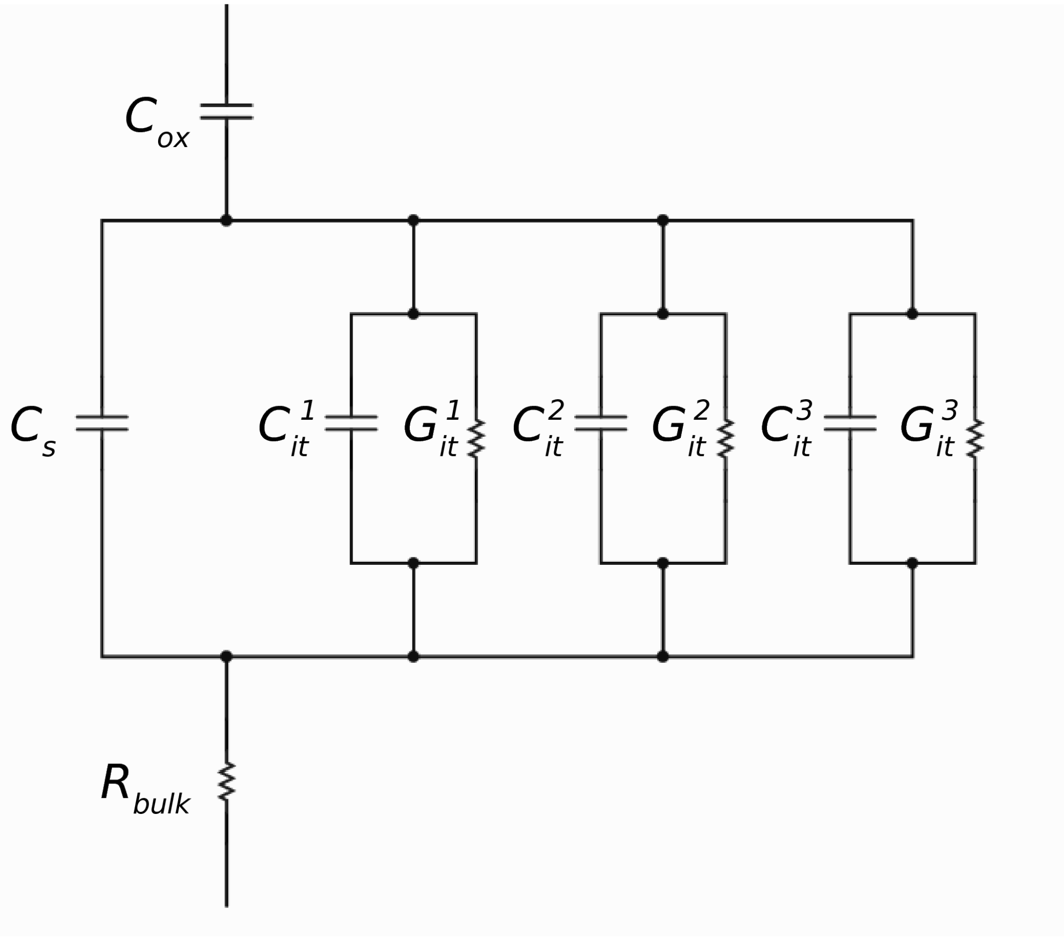
$$C_{it}^{p}\left(V_s, f\right) = \frac{q_0^2 S}{k_0T}\int_{E_v}^{E_c} D_{it}\left(E_{it}\right)\cdot\frac{\exp\left(\frac{-(E_c-E_{it})-q_0V_s-E_F}{k_0T}\right)}{\left[1+\exp\left(\frac{-(E_c-E_{it})-q_0V_s-E_F}{k_0T}\right)\right]^2}$$

$$\times\frac{dE_{it}}{1+\frac{\omega^2}{C_0^2}\frac{1}{\left[\exp\left(\frac{q_0V_s}{k_0T}\right)+\exp\left(\frac{-(E_c-E_{it})-E_F}{k_0T}\right)\right]^2}}$$

- G_{it}: interface trap conductance

$$G_{it}^{p}\left(V_s, f\right) = \frac{\omega^2 q_0^2 S}{k_0T}\int_{E_v}^{E_c} D_{it}\left(E_{it}\right)\cdot\frac{\exp\left(\frac{-(E_c-E_{it})-q_0V_s-E_F}{k_0T}\right)}{\left[1+\exp\left(\frac{-(E_c-E_{it})-q_0V_s-E_F}{k_0T}\right)\right]^2}$$

$$\times\frac{\frac{1}{C_0}\cdot\frac{1}{\left[\exp\left(\frac{q_0V_s}{k_0T}\right)+\exp\left(\frac{-(E_c-E_{it})-E_F}{k_0T}\right)\right]}}{1+\frac{\omega^2}{C_0^2}\frac{1}{\left[\exp\left(\frac{q_0V_s}{k_0T}\right)+\exp\left(\frac{-(E_c-E_{it})-E_F}{k_0T}\right)\right]^2}}\cdot dE_{it}$$



- R_{bulk}: series resistance from bulk doping

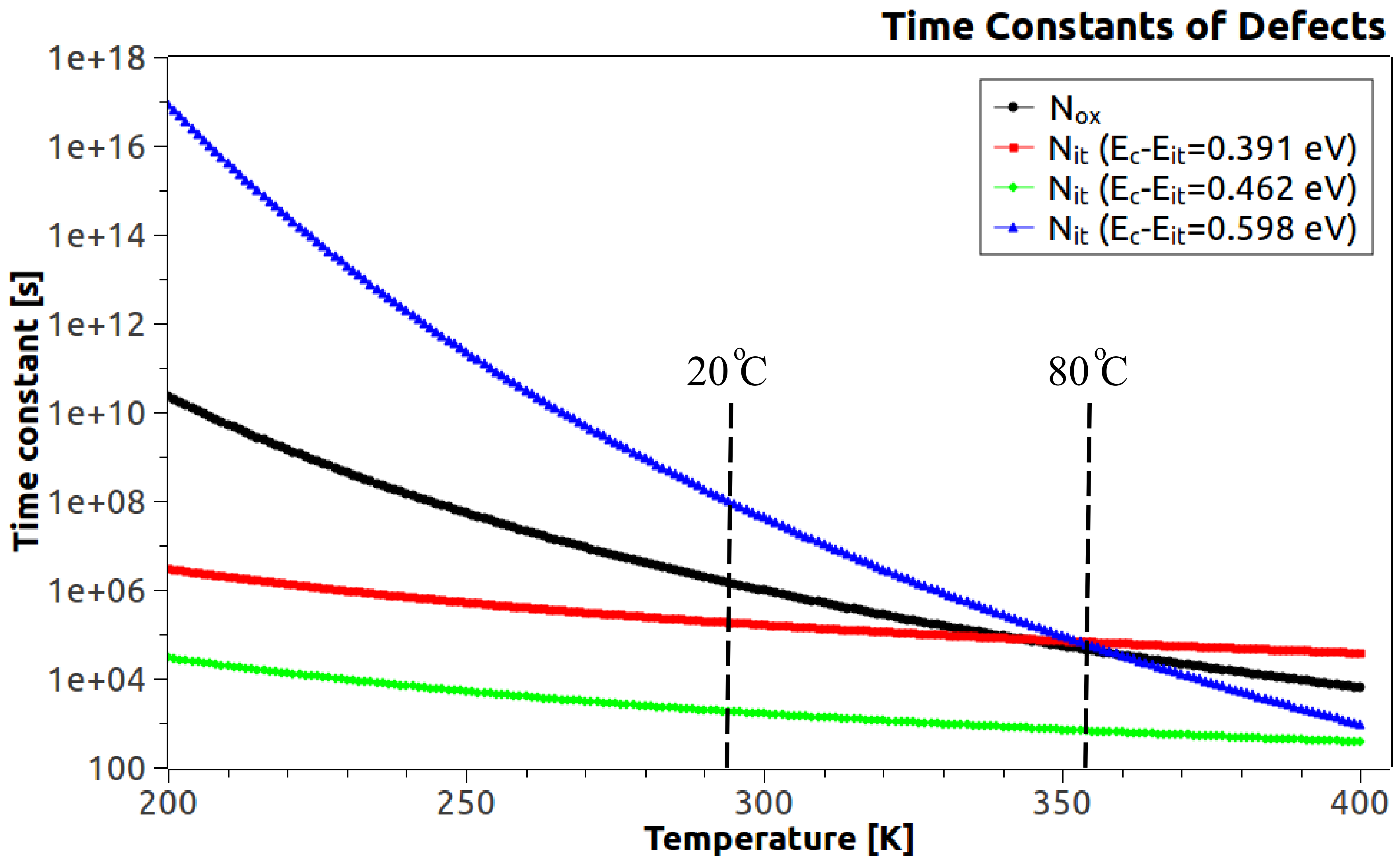
$$R_{bulk}\left(V_s\right) = \frac{1}{q_0\mu_n N_d}\cdot\frac{d_{si}}{S}$$

- Relation between V_g and band bending V_s:

$$V_g\left(V_s\right) = V_s + \varphi_{ms} - \frac{q_0 N_{ox} S}{C_{ox}} - \frac{Q_{si}\left(V_s\right)}{C_{ox}} - \frac{Q_{it}\left(V_s\right)}{C_{ox}}$$

Results: annealing kinetics of defects

- **Annealing time constants for different defects:**



τ at 20°C:

N_{ox} : 18 days
N_{it} [0.391 eV]: 53 hours
N_{it} [0.462 eV]: 31 min
N_{it} [0.598 eV]: 1378 days

τ at 80°C:

N_{ox} : 13 hours
N_{it} [0.391 eV]: 19 hours
N_{it} [0.462 eV]: 11 min
N_{it} [0.598 eV]: 19 hours

- The interface trap at 0.462 eV can be annealed out quickly at room temperature.
- The interface traps at 0.391 eV and 0.598 eV, and fixed oxide charges are very stable at room temperature.
- Short time annealing at higher temperature is needed to stablize sensros' performance (remove the effects due to fast annealing of the interface traps at 0.462 eV).

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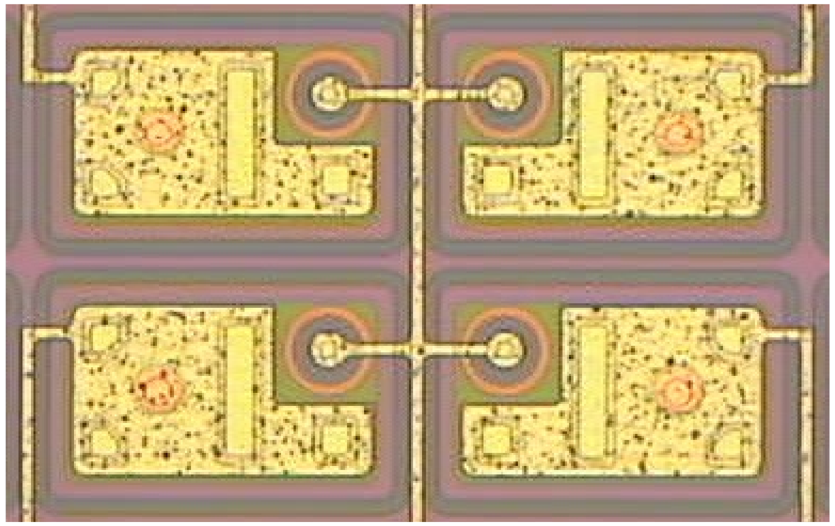
* results with large uncertainties

Influence in electric performance of segmented sensors

- **CMS n-on-n test pixel sensors (Current/Capacitance-Votlage behavior):**

· Sensor's thickness: ~300 µm · Orientation: <111>
· Pixel: 100 µm × 150 µm · Resistivity: 4 kΩ·cm



· Jump of capacitance around V_{dep} is due to the isolation between pixel sensors on the same test field.

· Due to the compensation of p-spray to surface charges, full depletion voltage V_{dep} did not increase with irradiaitons.

· Similar behavior of leakage current was observed for n^+ on n sensors:
1) $V_{bias} < V_{dep}$, p+ side traps contribute to $I_{leakage}$
2) $V_{bias} > V_{dep}$, both p+ and n+ side traps contribute