



Lab measurements and testbeam results of irradiated n^+ -in-n planar pixel sensors for IBL and beyond

18th RD50 Workshop

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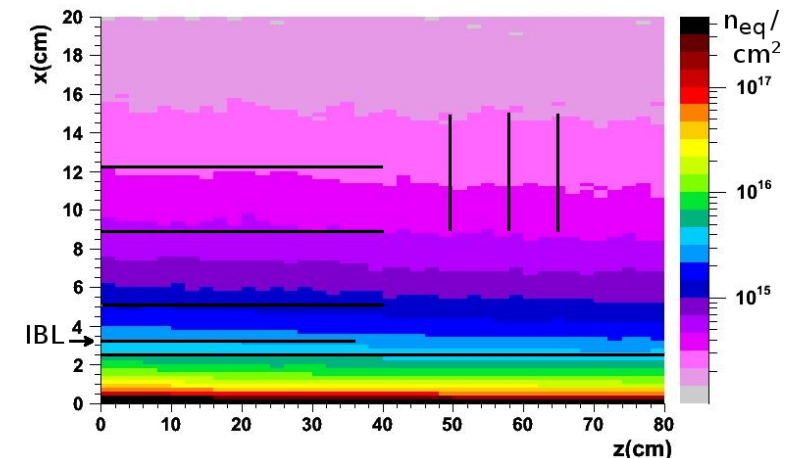
GEFÖRDERT VOM



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für Bildung
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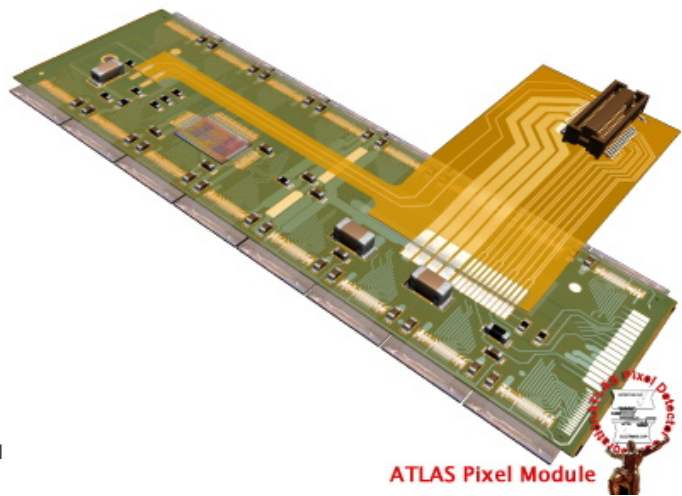
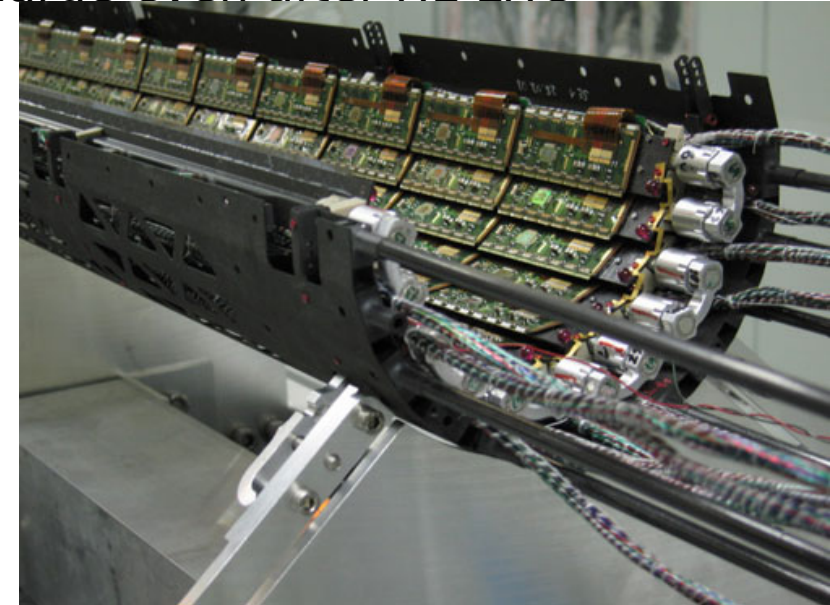
Why planar Pixel R&D – Upgrade Plans for LHC

- Two phased upgrade plan on the path to sLHC:
 - Phase 1: $5 \cdot 10^{15} n_{eq}/\text{cm}^2 \rightarrow \text{IBL}$
 - Phase 2: $2 \cdot 10^{16} n_{eq}/\text{cm}^2 \rightarrow \text{sLHC}$
- Current (n⁺-in-n) pixel detector has been shown to be rad hard up to $1 \cdot 10^{15} n_{eq}/\text{cm}^2$
- Planar n⁺-in-n technology is proven and reliable
- Results gained with strip sensors show promising results with regard to collected charge (charge amplification!)
- First results with real pixel taken this year confirm the capability and rad-hardness of planar sensors



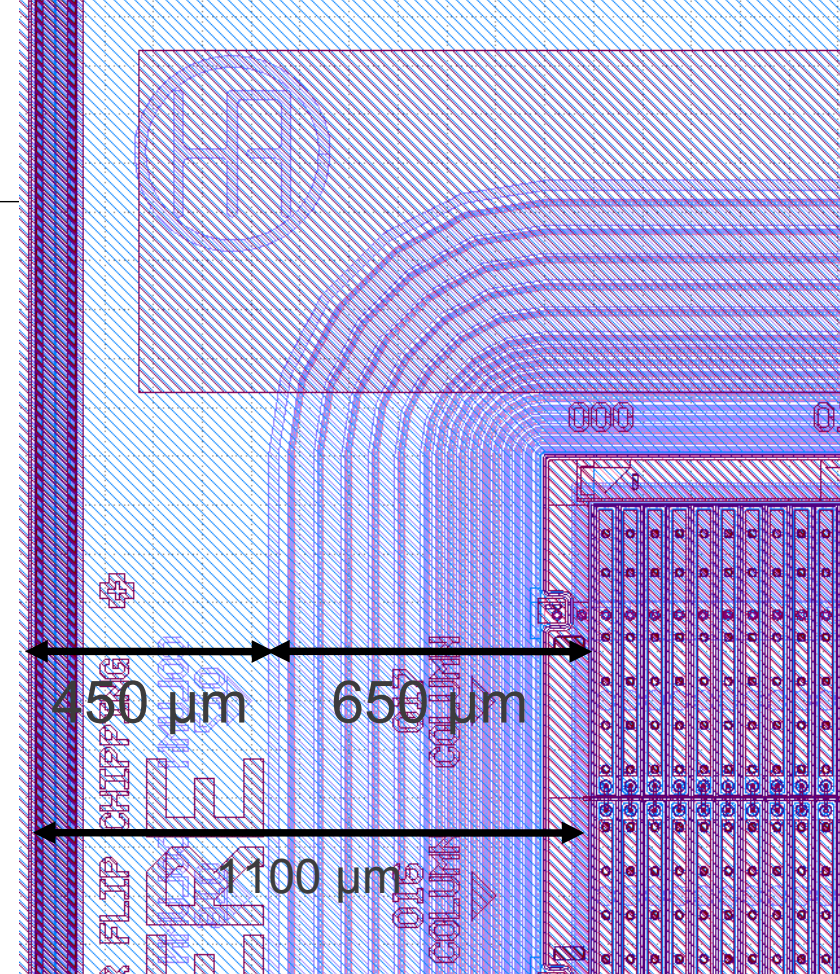
Planar Sensors: Basic Information

- The current ATLAS Pixel detector is based on planar sensors
- Planar sensors were already shown to yield charge even after HL-LHC fluences of $2 \cdot 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$
- IBL specifications to qualify:
 - Power dissipation $< 200 \text{ mW}/\text{cm}^2$
 - Leakage current $< 100 \text{ nA}/\text{pixel}$
 - Operation temperature -15°C on sensor
 - Inactive edges $< 450 \mu\text{m}$
 - Thickness between 150 and $250 \mu\text{m}$
 - Sufficient hit efficiency
 - after a benchmark fluence of $5 \cdot 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$
 - at a maximum bias voltage of 1 kV

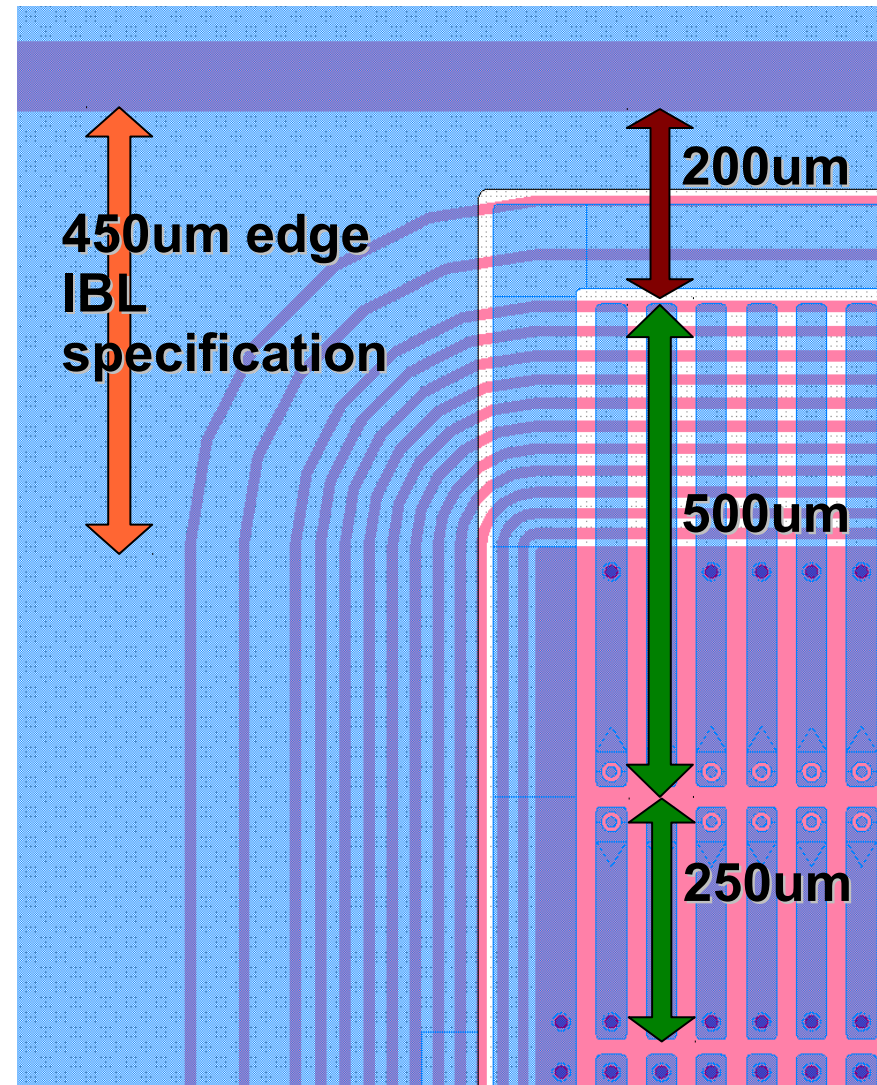
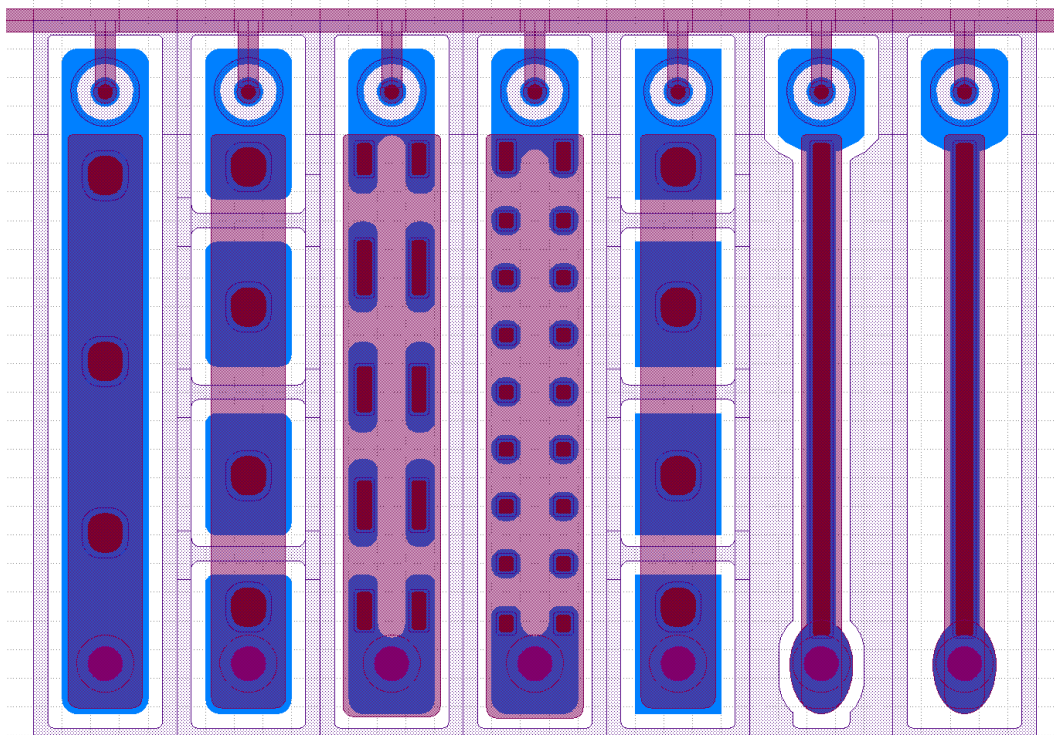
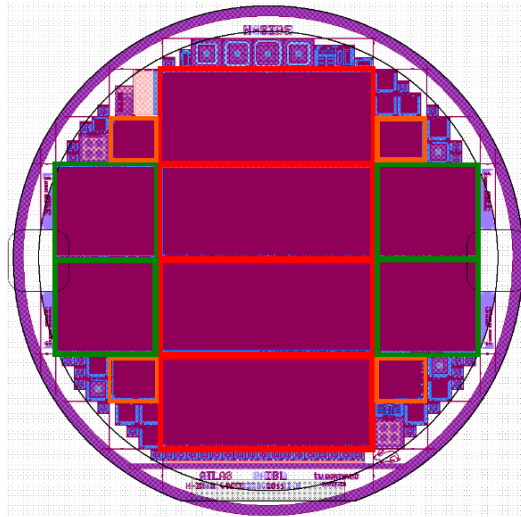


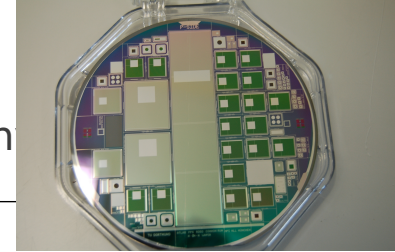
Initial point and progress

- Standard SingleChip Sensors taken from ATLAS Pixel production wafers
- n⁺-in-n design produced by CIS
- 16 guard rings with overhanging metal
- 250µm thick DOFZ bulk
- 400µm by 50µm pixel cells
- 2880 pixel cells!
- New production in 2009:
 - MCz and FZ in 285µm
 - Joint RD50 and PPS production
- New Production in 2010:
 - PPS production with structures contributed by several RD50 member institutes
 - varied bulk thicknesses (150µm - 285µm)
- several special layouts (e.g. w/o bias grid) and FE-I4 compatible sensors on all production wafer
- IBL pre-production 2011



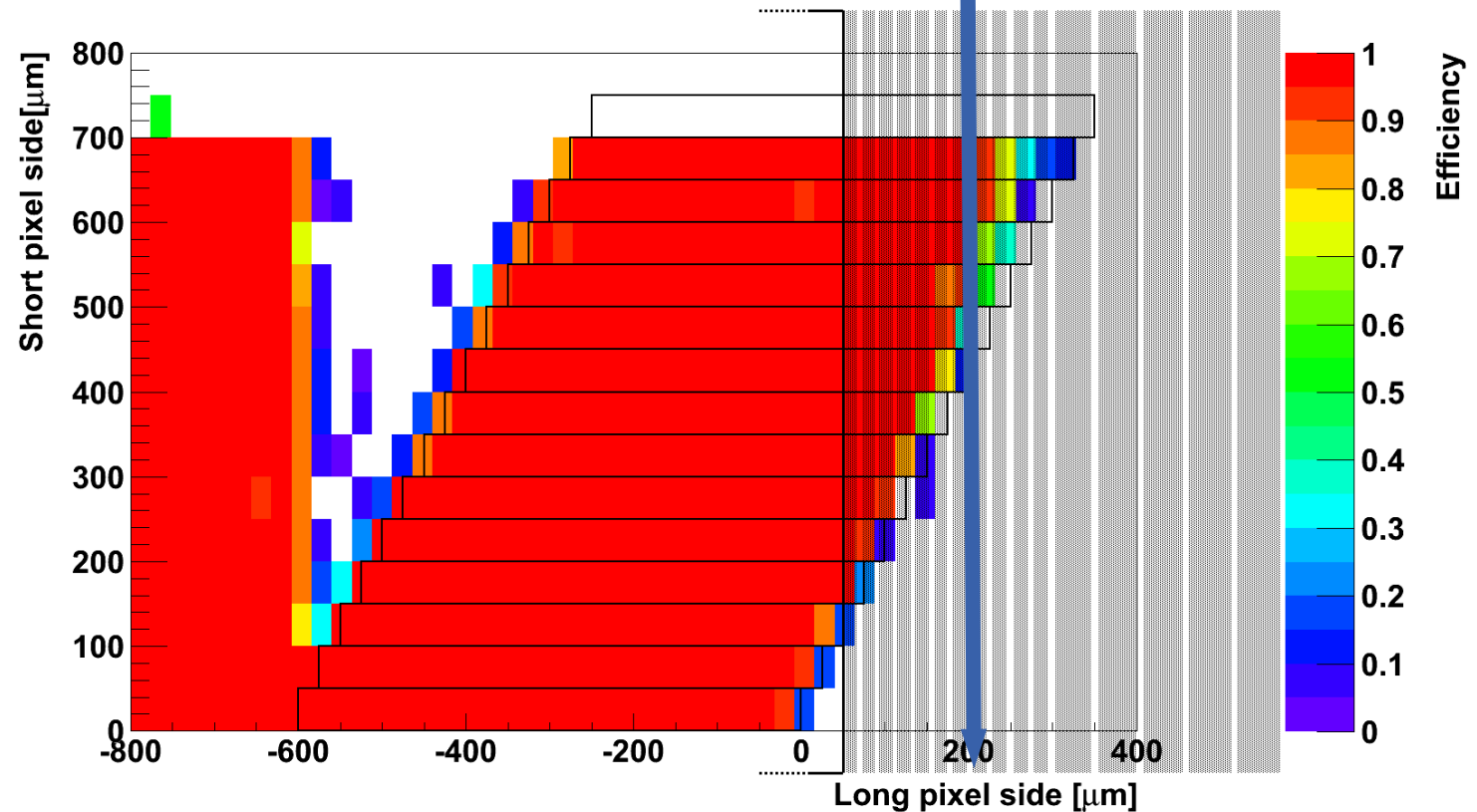
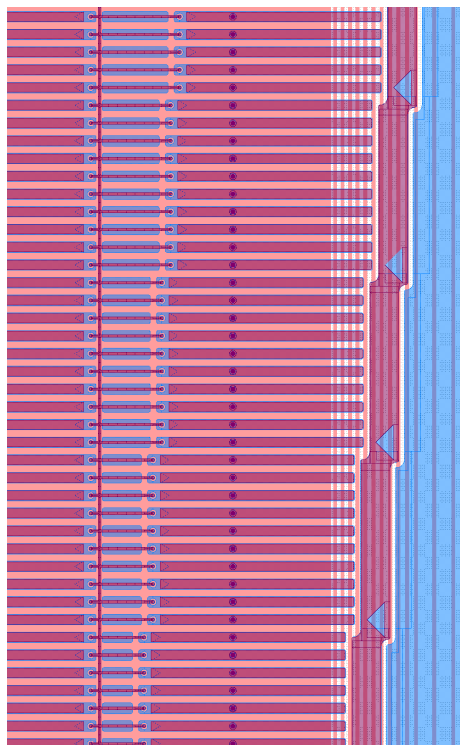
New layouts





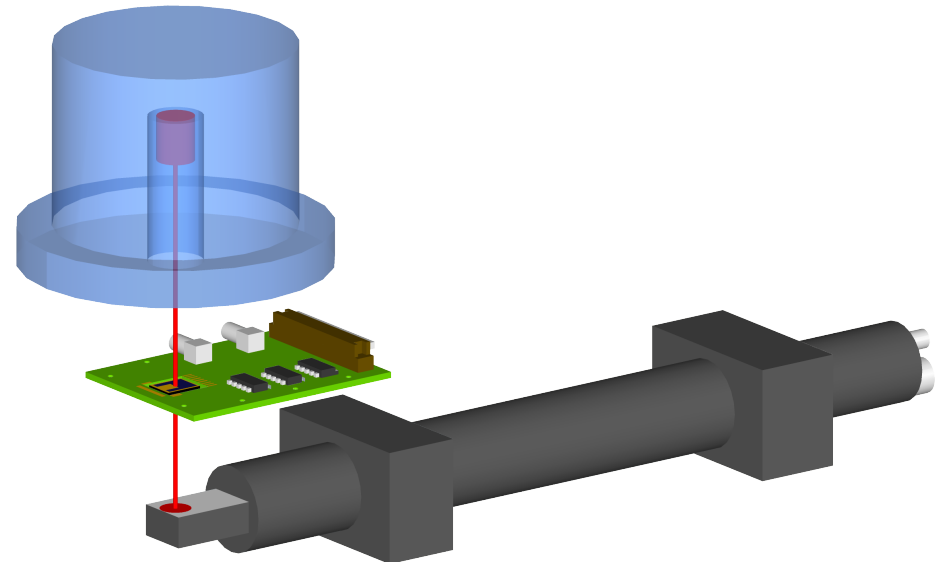
Slim-edge: testbeam results available up to now

- dedicated test structure ('pixel shifted stepwise') confirms that charge is collected opposite of the guard rings
- estimated region of high (>99%) efficiency before irradiation: up to ~200 μm from the HV implant (i.e. ~250 μm inefficient edge)
- looks promising (strongly supported by simulation results at LAL by M. Benoit)



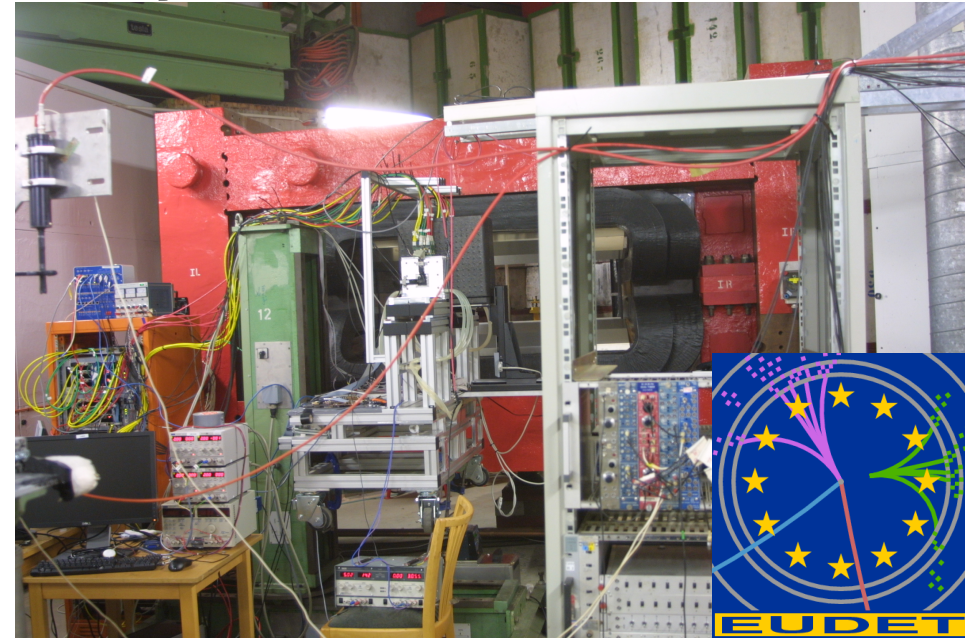
Experimental Methods: electrons

- ^{90}Sr beta electrons:
 - Charge Collection Efficiency measured with a Sr-90 source (landau expected)
 - Operation temperature below -55°C with dry ice in a insulated box
 - Standard ATLAS TurboDAQ readout (already used during the production process)
 - Two possible triggers:
 - trigger scintillator beneath the sensor, only through-going electrons
 - (internal) hitbus trigger, all electrons
- Advantages:
 - easily accessible
 - study of many parameters possible
- Disadvantages:
 - much scattering
 - “no real MIPs”



The IBL Testbeam in February 2011

- Testbeam data taken in February 2011 at DESY
- Allows to take space resolved data
- Samples were mounted in the DOBOX which uses a lab proven dry ice system capable of cooling heavily irradiated sensors
- New readout system USBpix used for FE-I3 and FE-I4
- Despite still existing trouble with irradiated FE-I3 much more amicable
- 4 GeV electrons

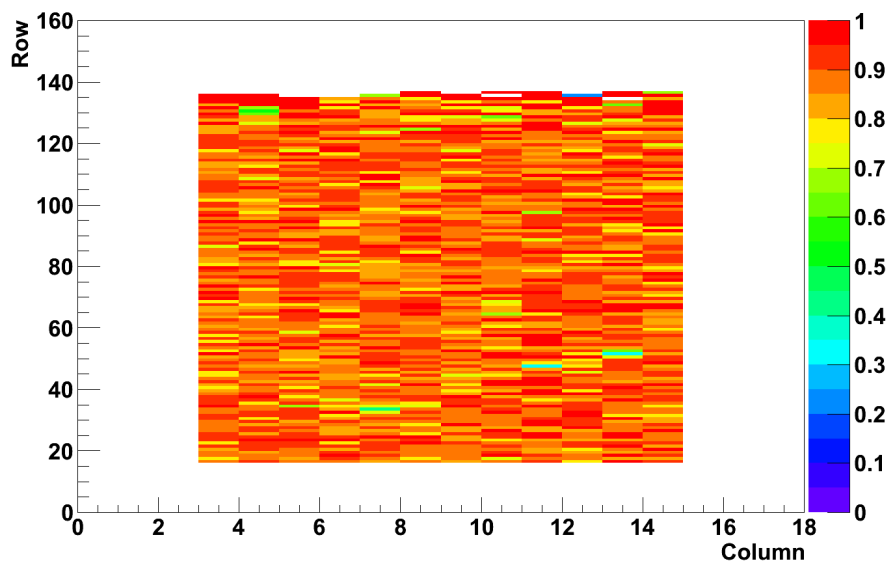


Many thanks to the IBL collaboration and in particular to the IBL Testbeam group and all people involved in the data taking and analysis

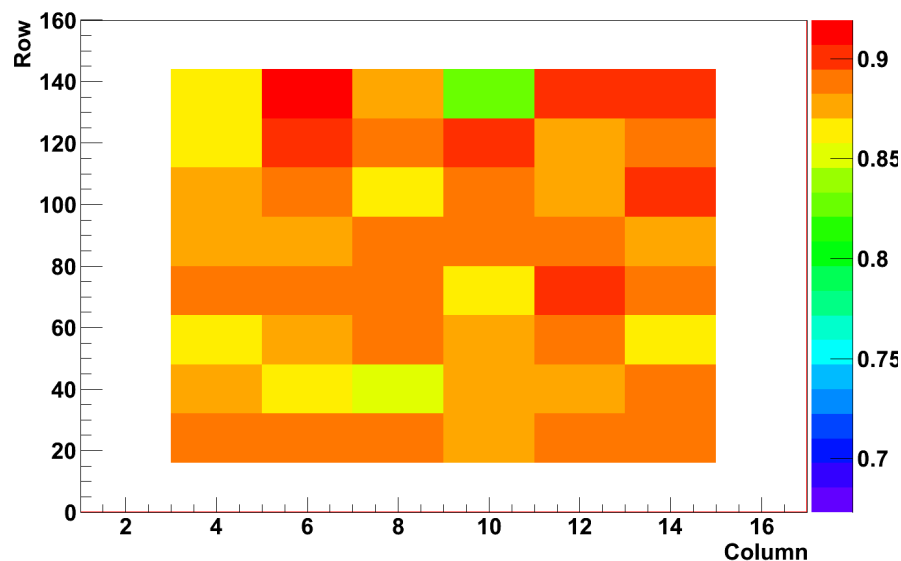
DO13 at 300V

Efficiency: 88.1%±0.1%

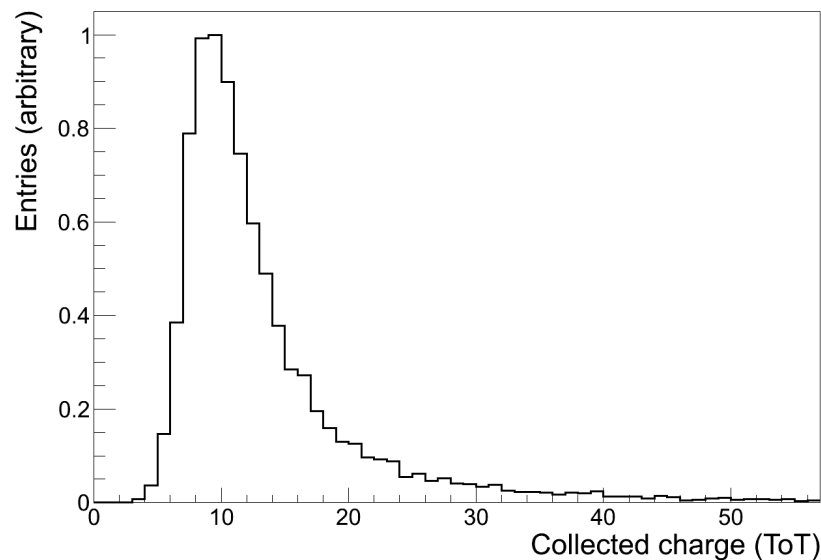
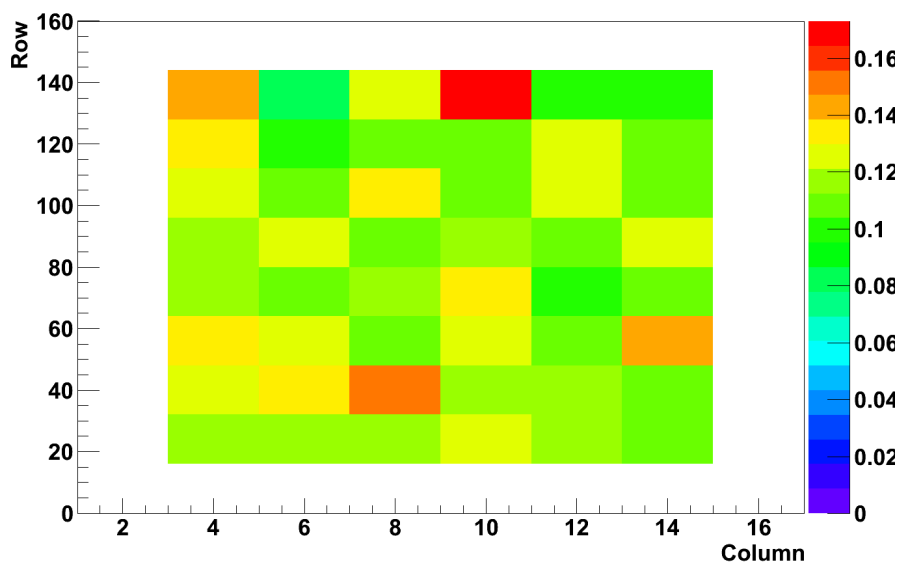
Efficiency Map



Efficiency Map 216



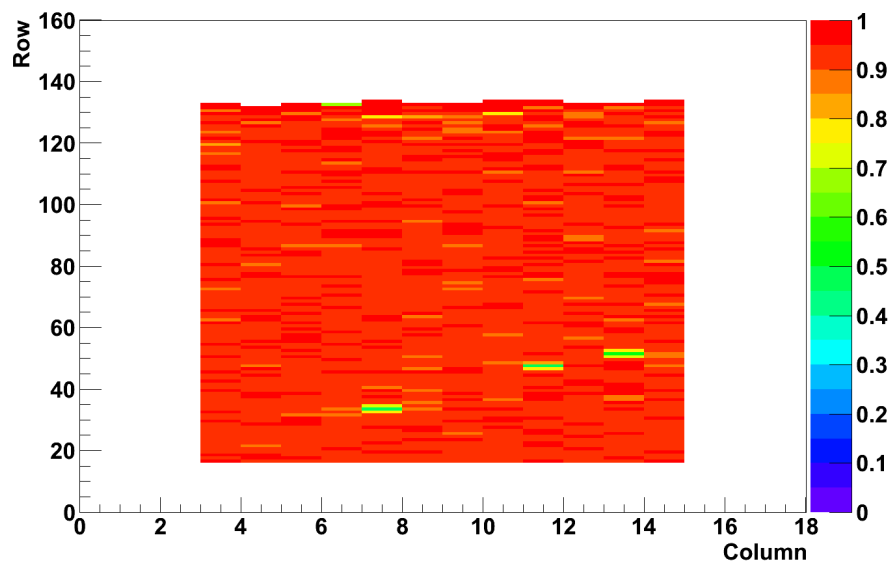
Inefficiency Map 216



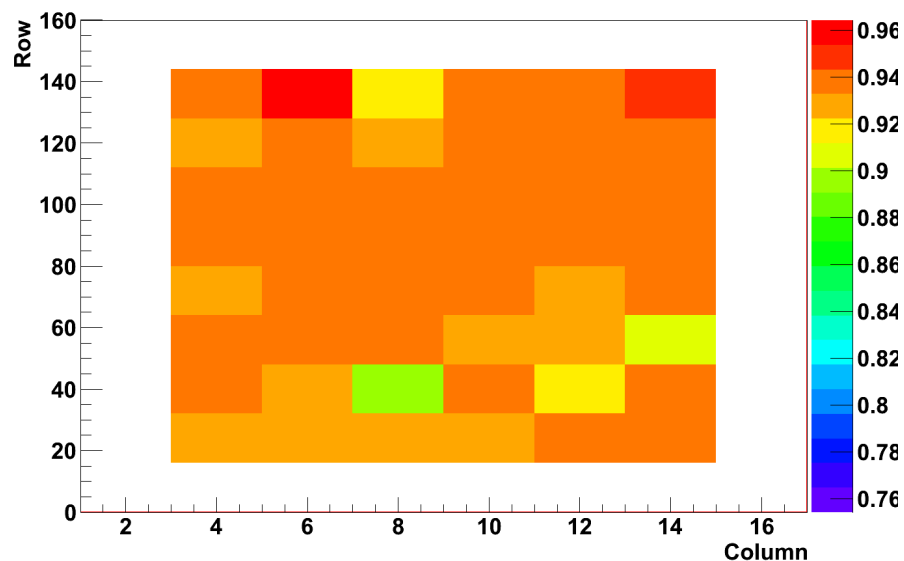
DO13 at 350V

Efficiency: $93.2\% \pm 0.1\%$

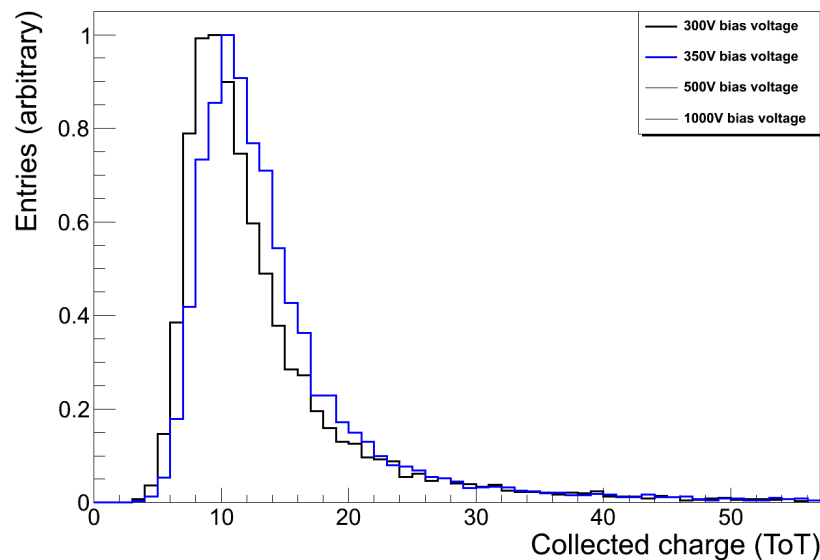
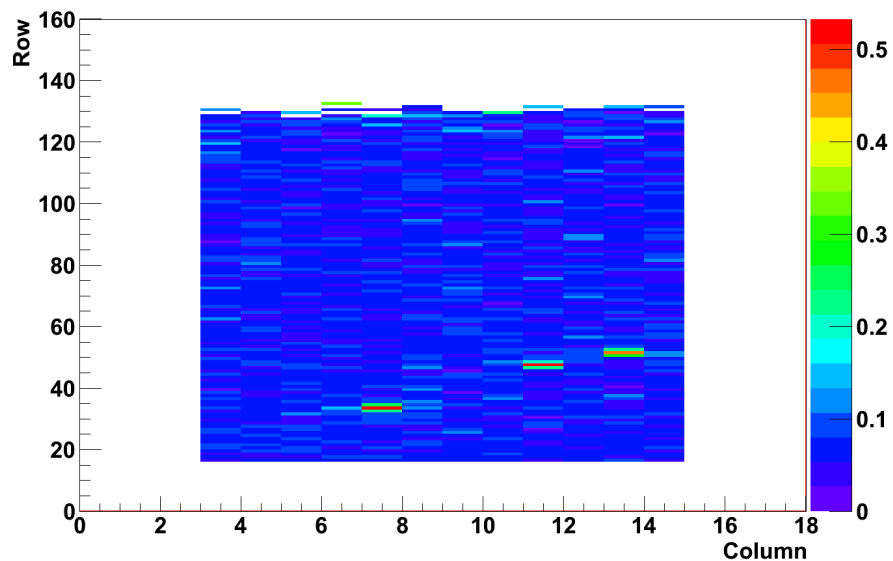
Efficiency Map



Efficiency Map 216



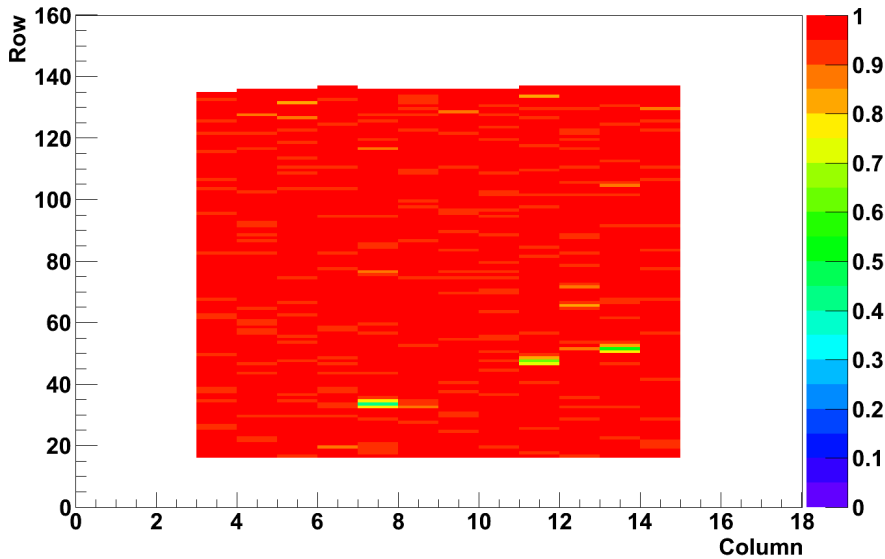
Inefficiency Map



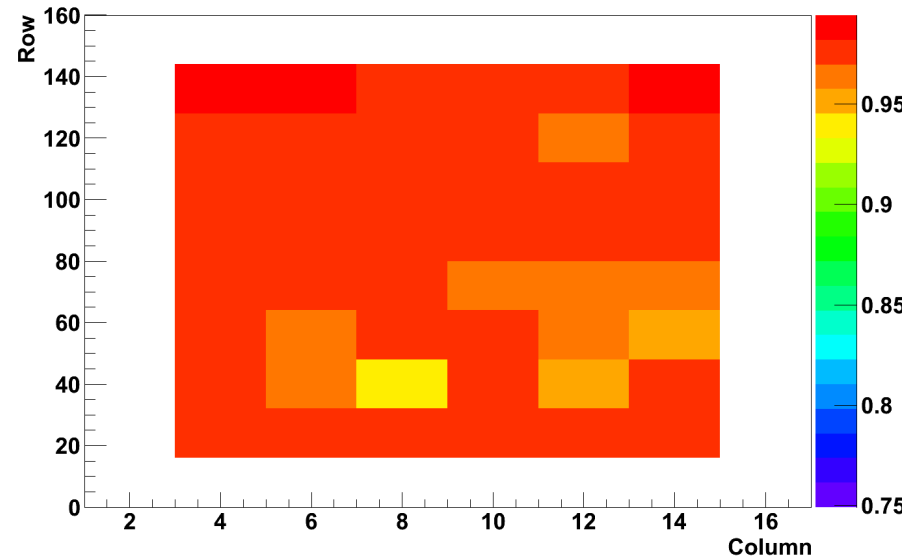
DO13 at 500V

Efficiency: $97.3\% \pm 0.1\%$

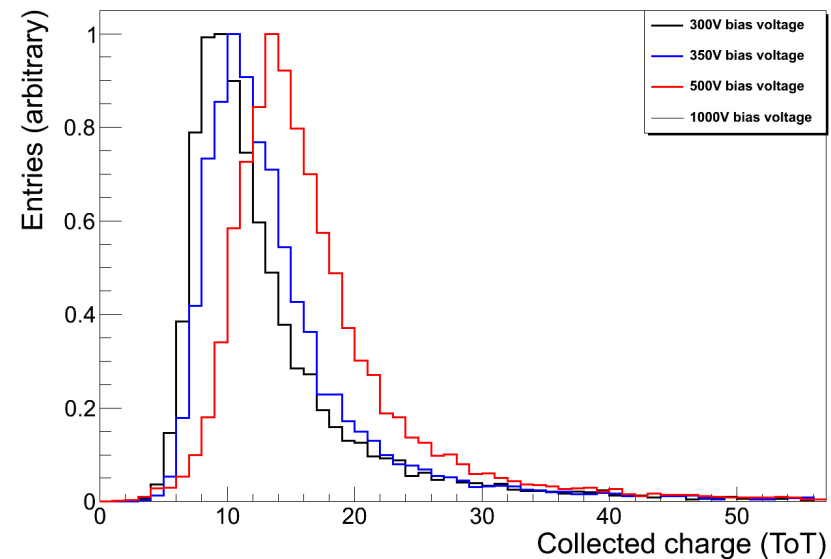
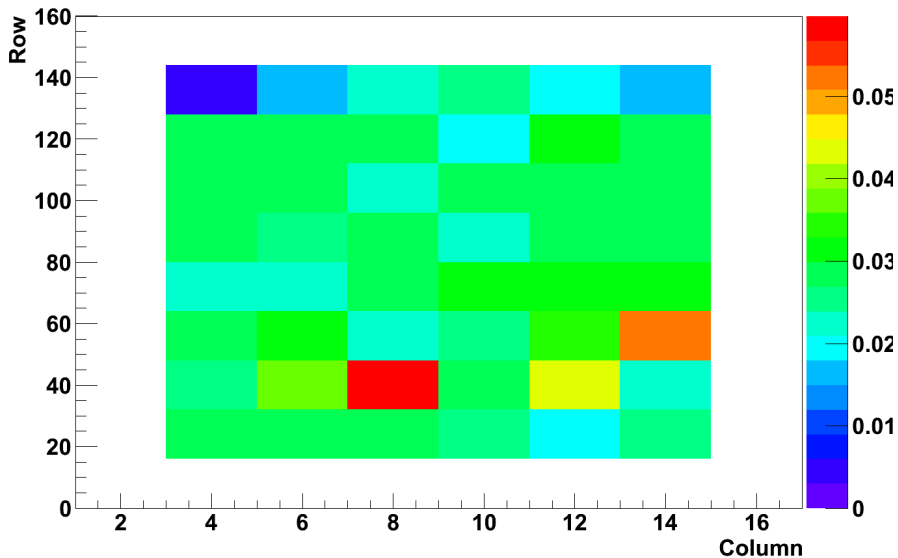
Efficiency Map



Efficiency Map 216



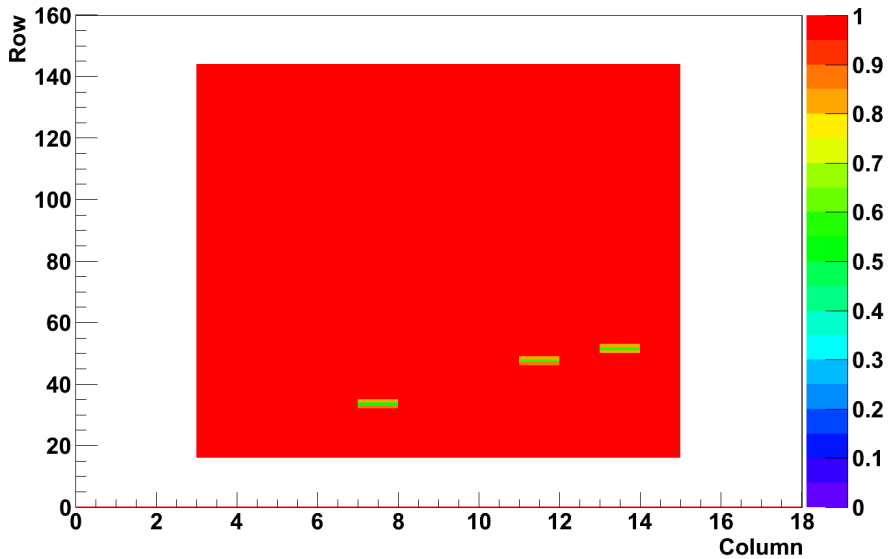
Inefficiency Map 216



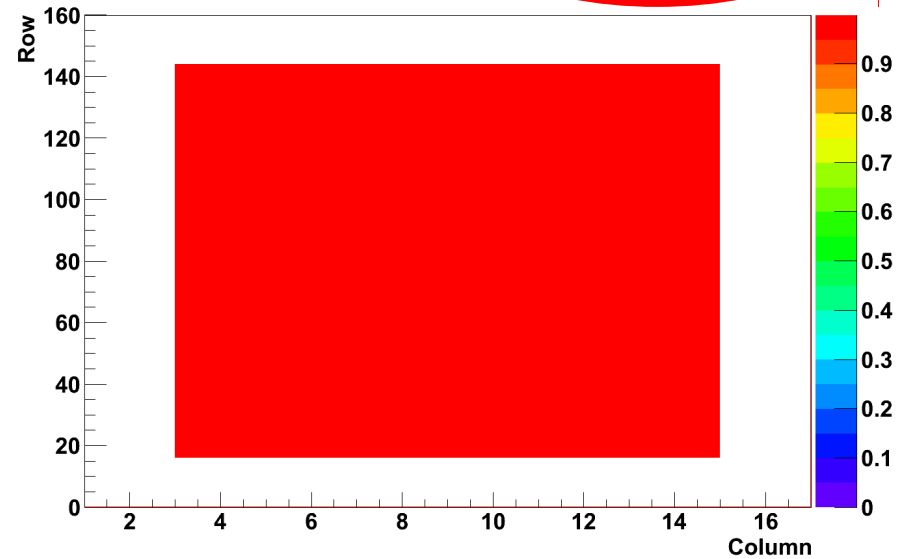
DO13 at 1000V

Efficiency: $99.6\% \pm 0.1\%$

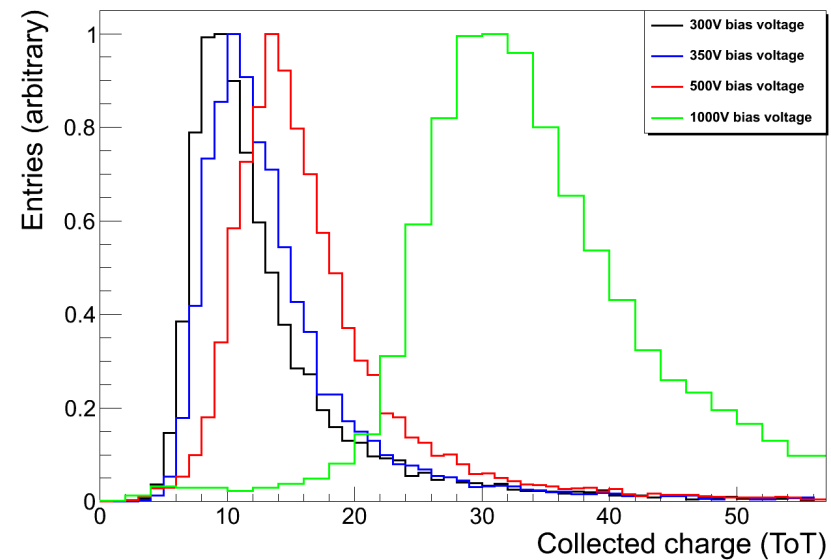
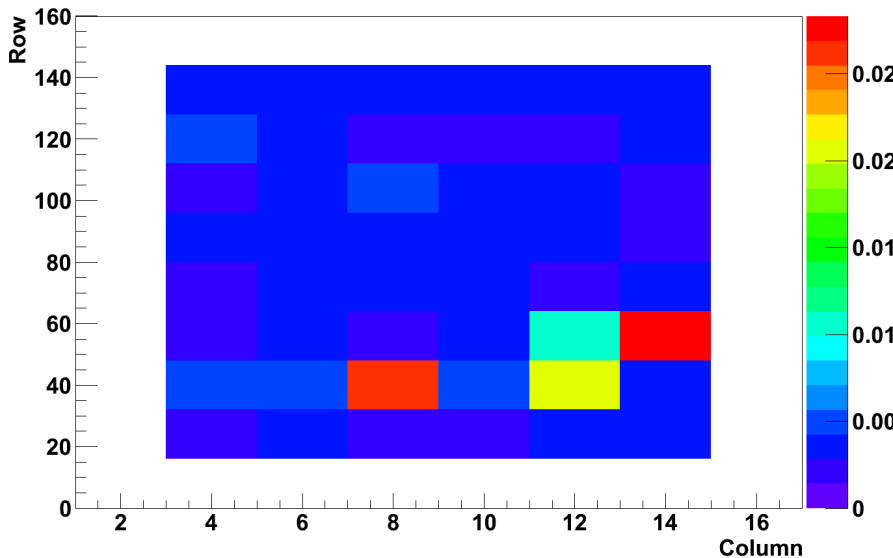
Efficiency Map



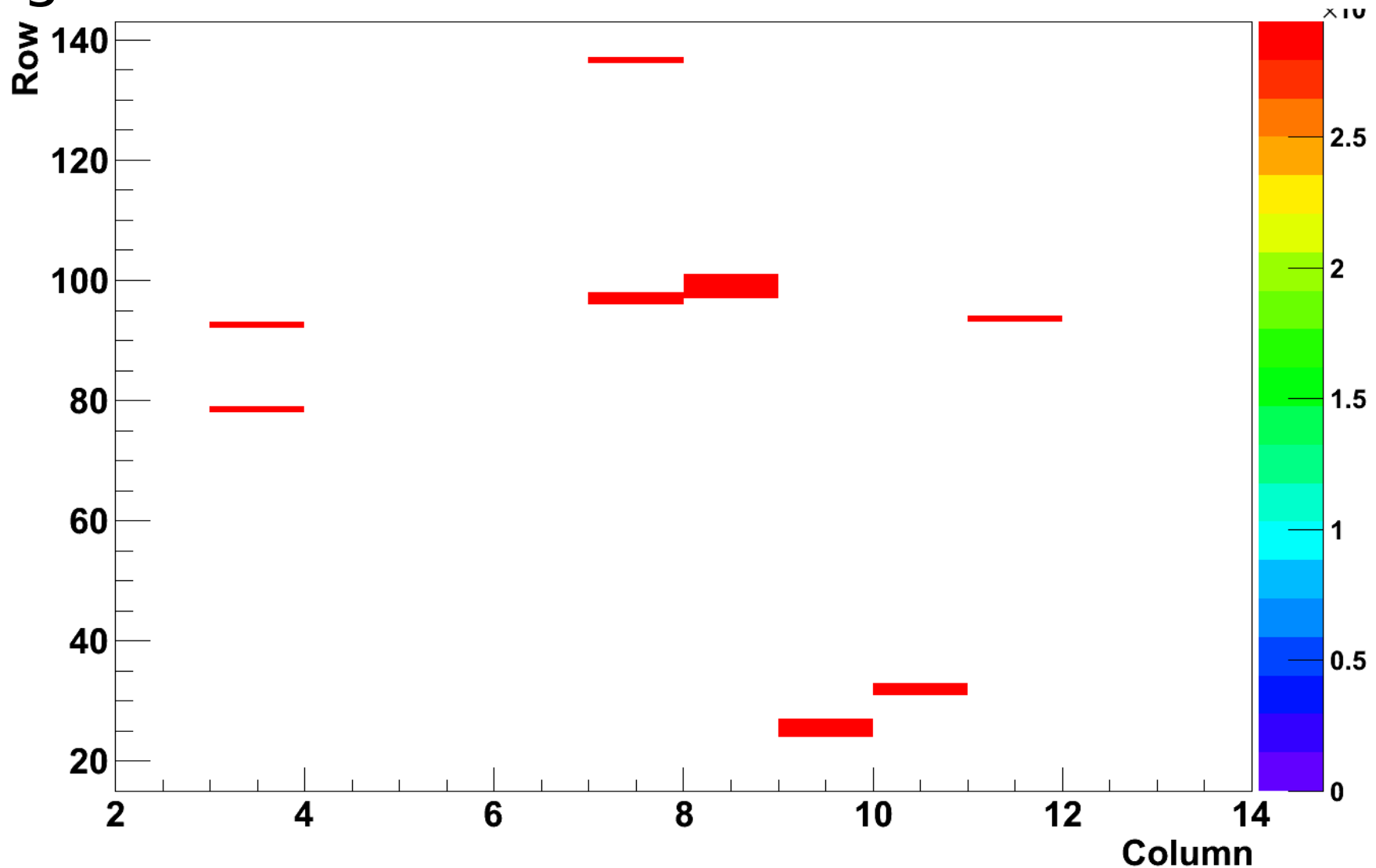
Efficiency Map 216



Inefficiency Map 216

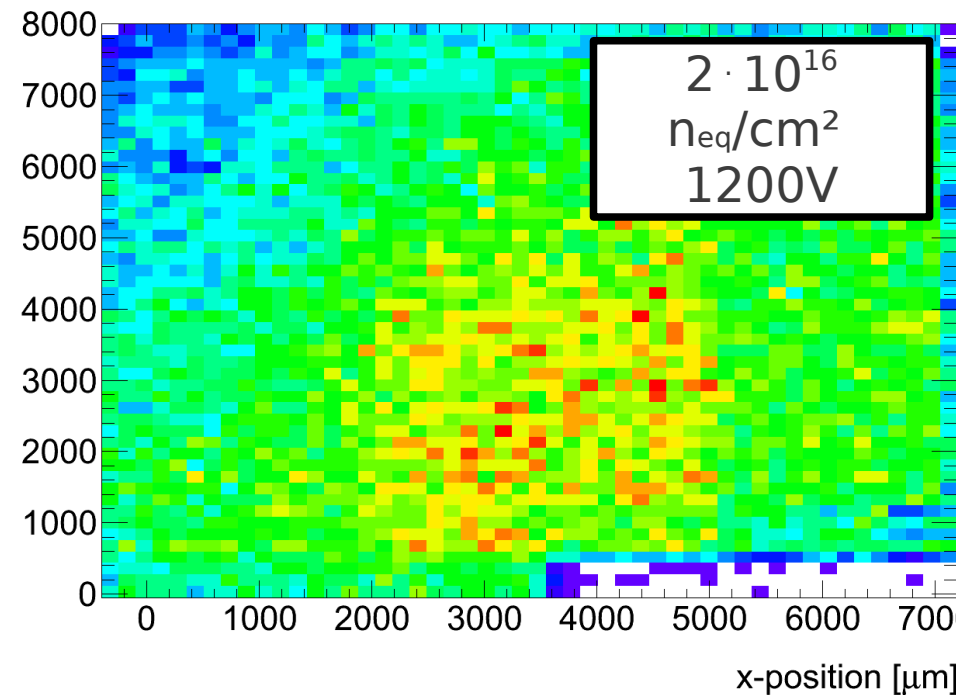
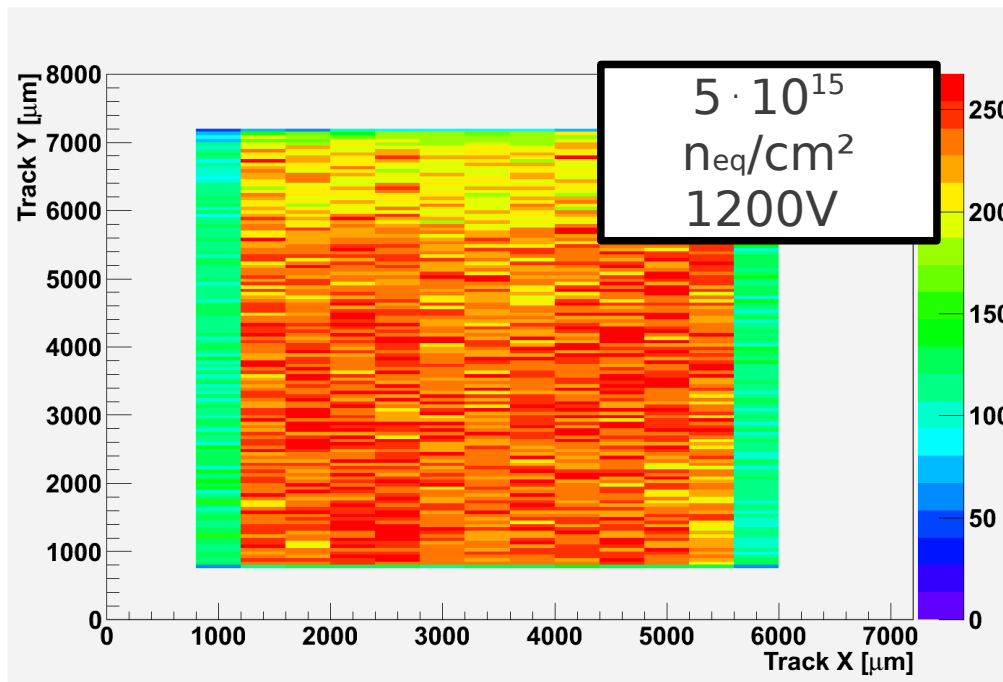
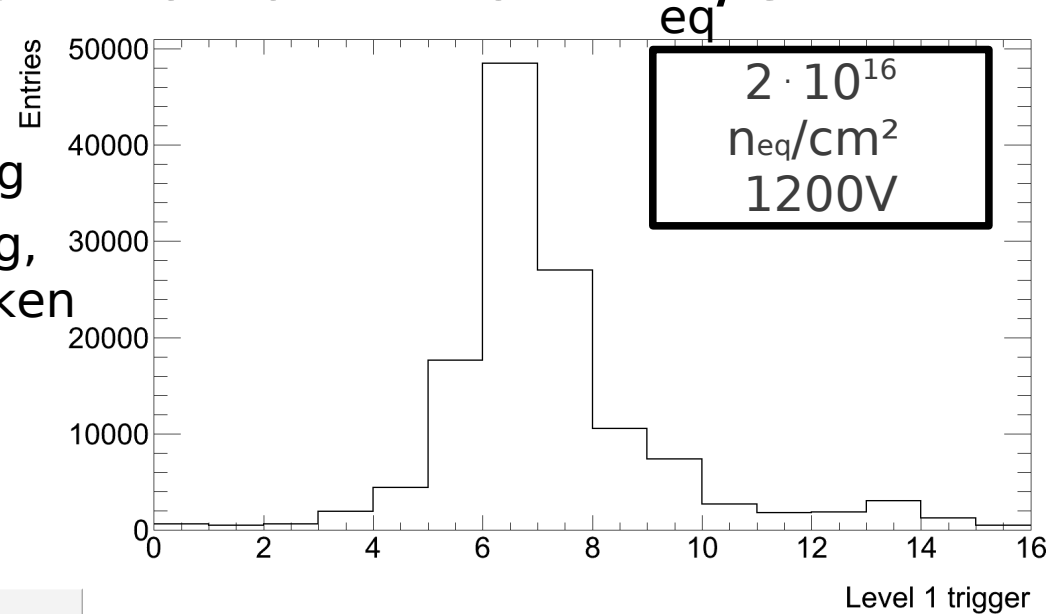


Peek at noise occupancy at 1000V in central region



A challenge: $5 \cdot 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ and $2 \cdot 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$

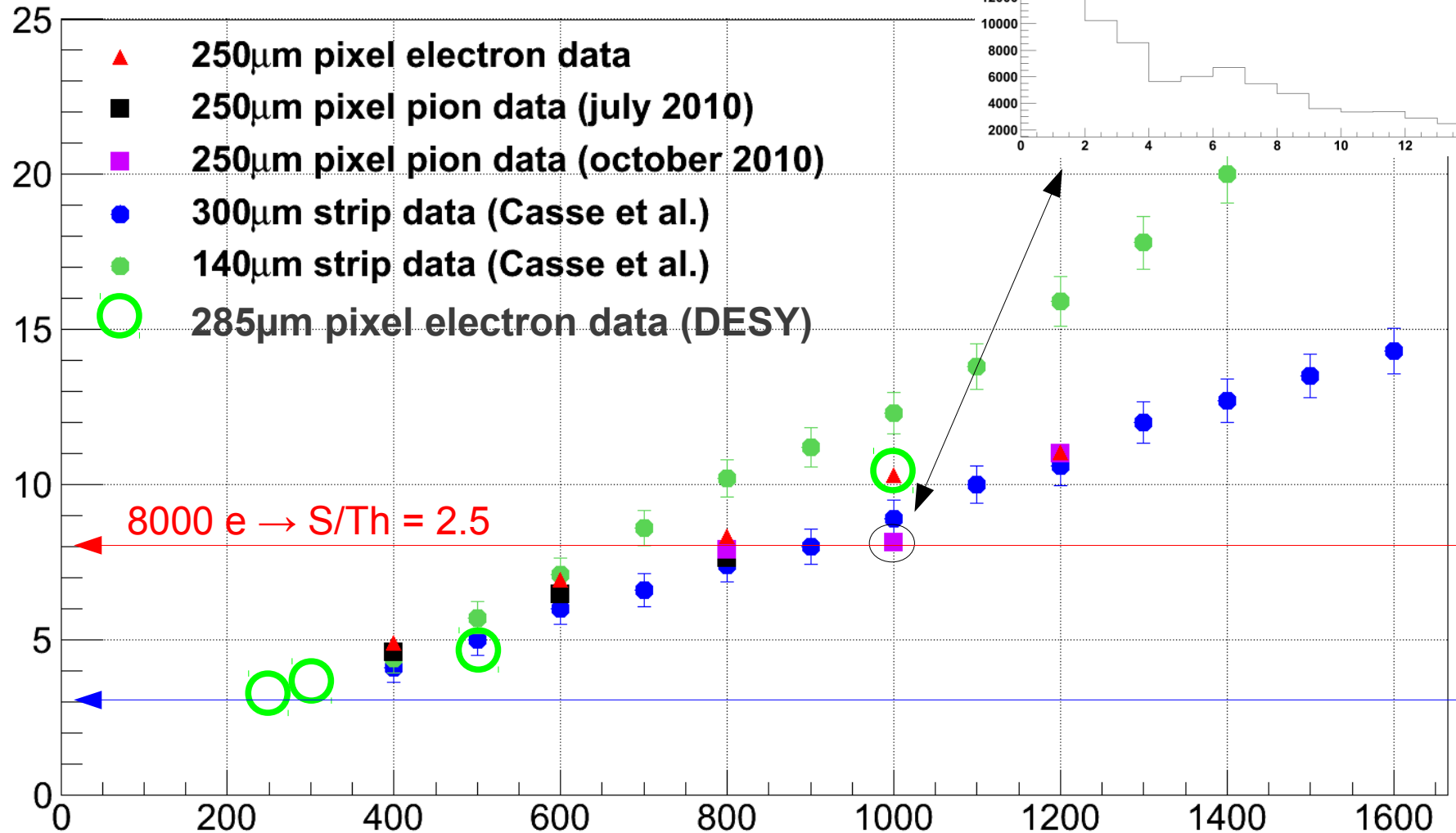
- Operation at below -50°C to exclude self-heating effects
- $2 \cdot 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$ sample always working
- $5 \cdot 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ sample mostly working, data with more such samples was taken and is currently being analysed
- Testbeam hitmaps look good
- Trigger-distribution shows little noise



Charge Collection $5 \cdot 10^{15} n_{eq}/cm^2$ summary

- data quite consistent
- MPV
- 1kV pion data point probably off due to "bad run"

Collected charge [kilo electrons]

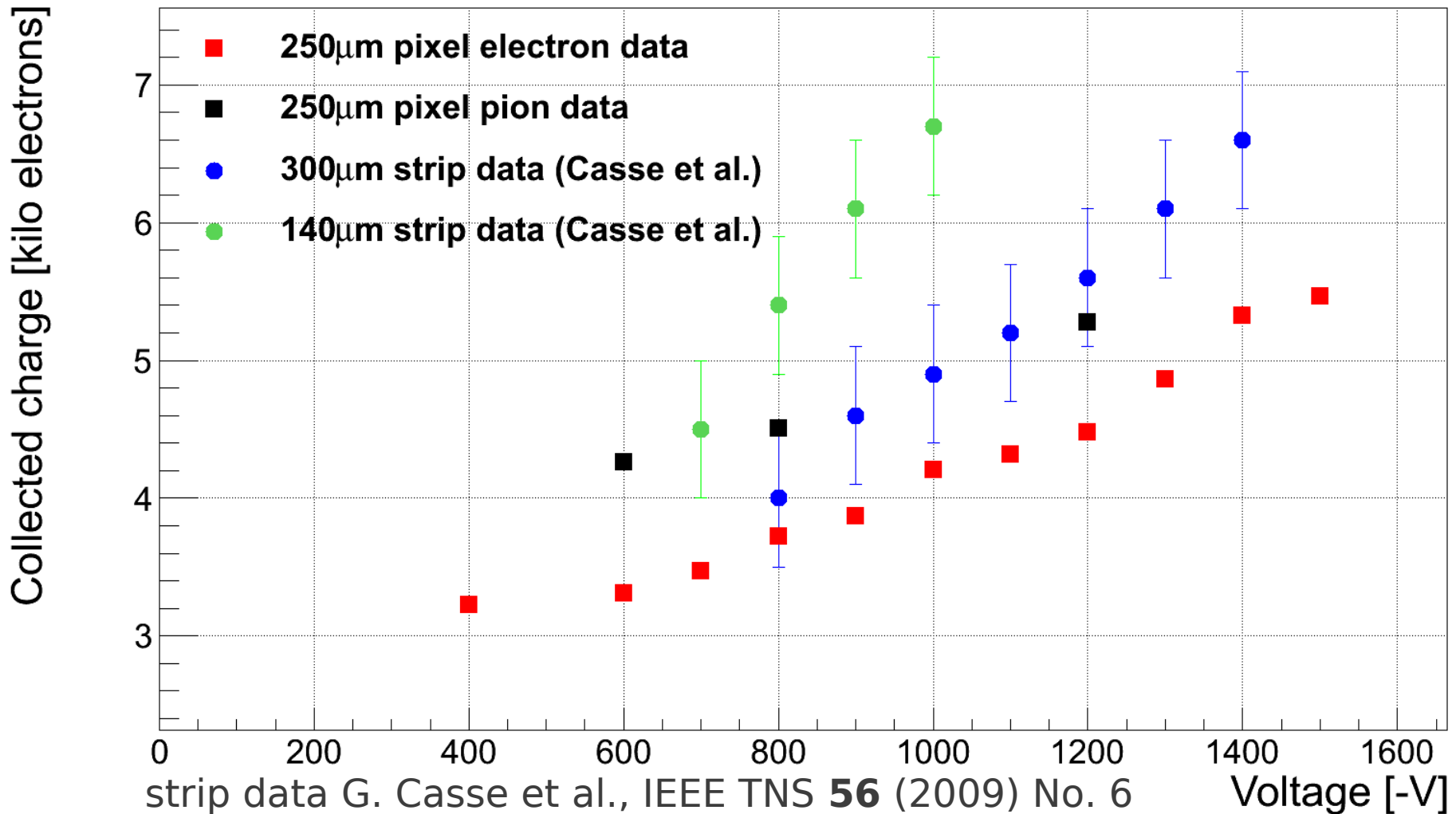


strip data: G. Casse et al., doi:10.1016/j.nima.2010.02.134

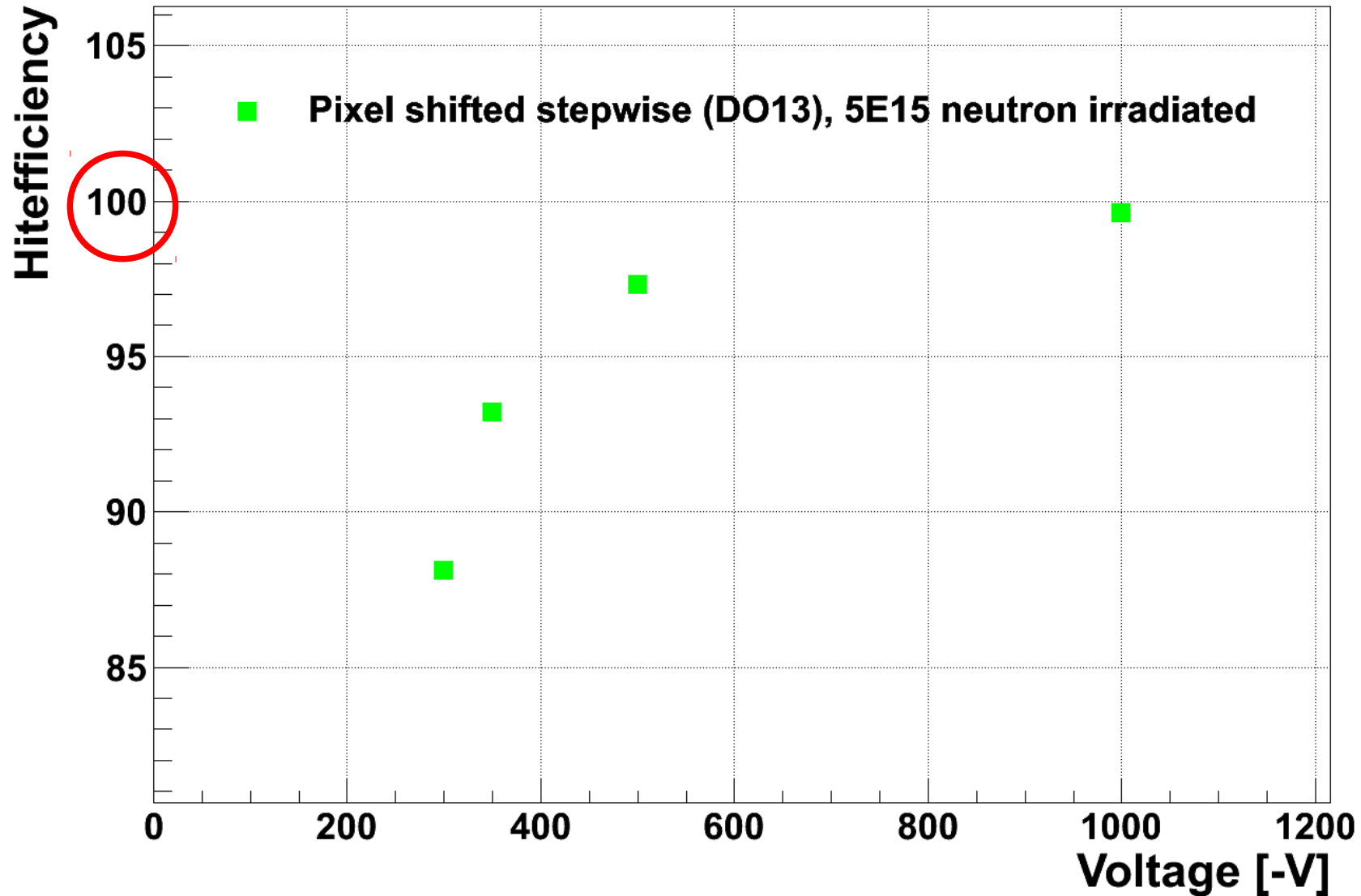
Voltage [-V]

Charge Collection $2 \cdot 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$ summary

- Pixel electron data lower than pion data and lower than strip data
- Might be a charge-sharing effect [doi:10.1016/j.nima.2010.11.186](https://doi.org/10.1016/j.nima.2010.11.186)
- MDV

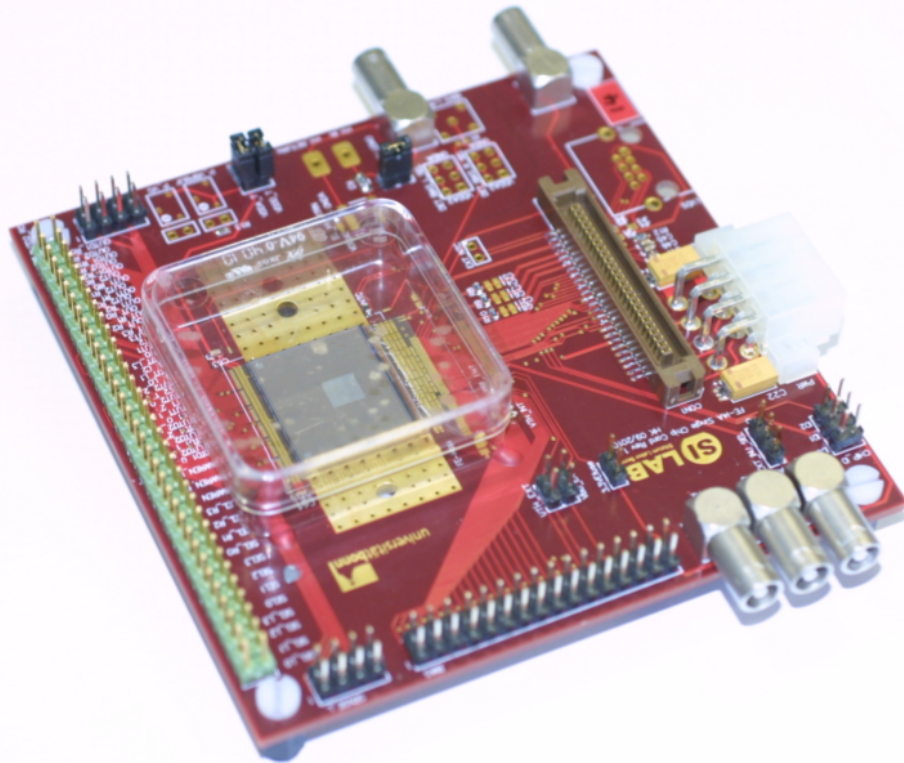


Hitefficiency at $5 \cdot 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ - Overview

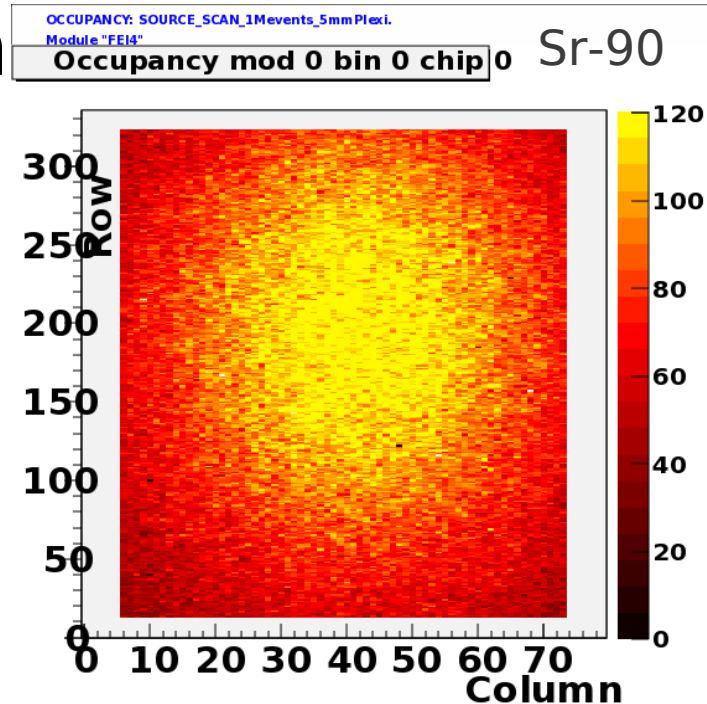


First 250 μm sensor FE-I4 assem

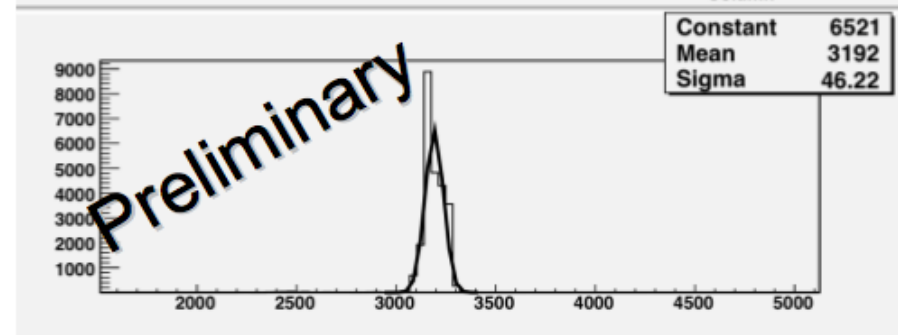
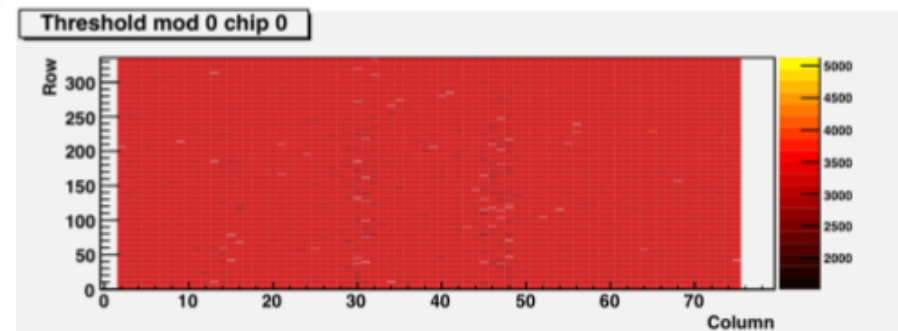
- Thresholds of below 3000 e^- seem possible



J. Jentsch

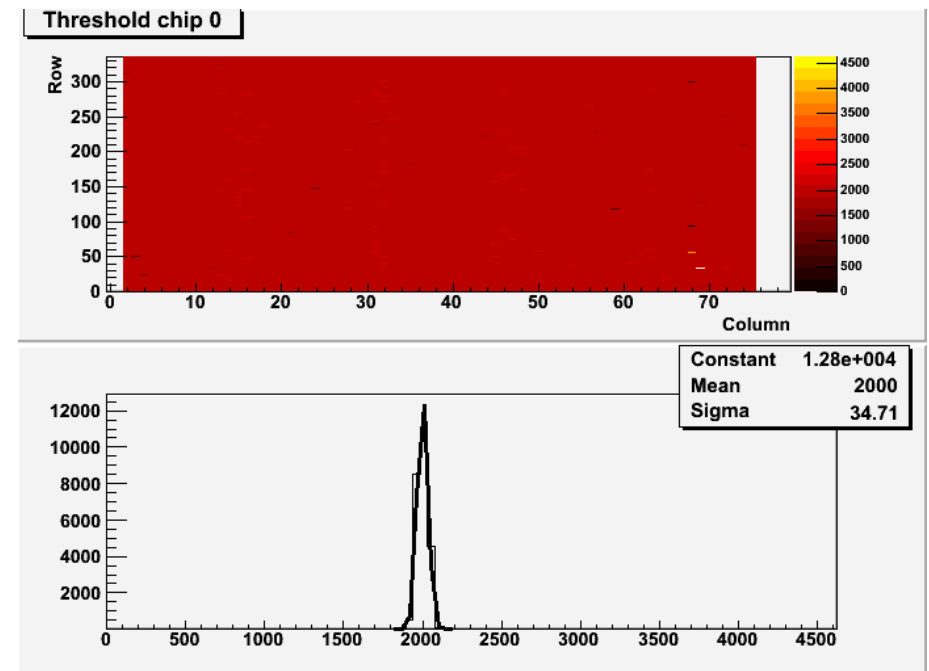
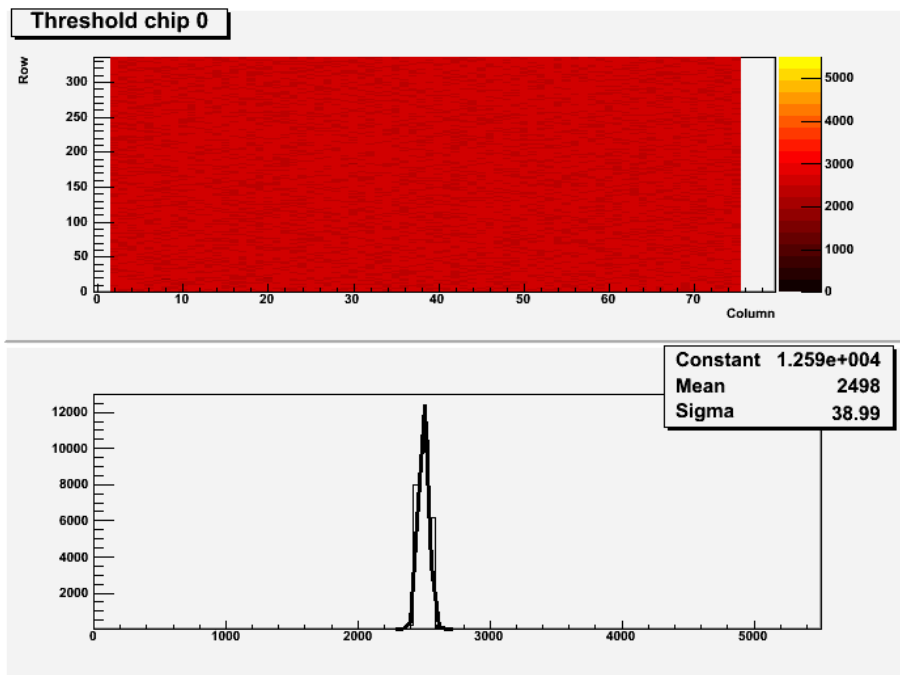


- Testbeam with unirradiated assemblies at DESY in February
- Immediately after irradiation testbeam in April at DESY as well



Tuning of neutron irradiated FE-I4 assemblies

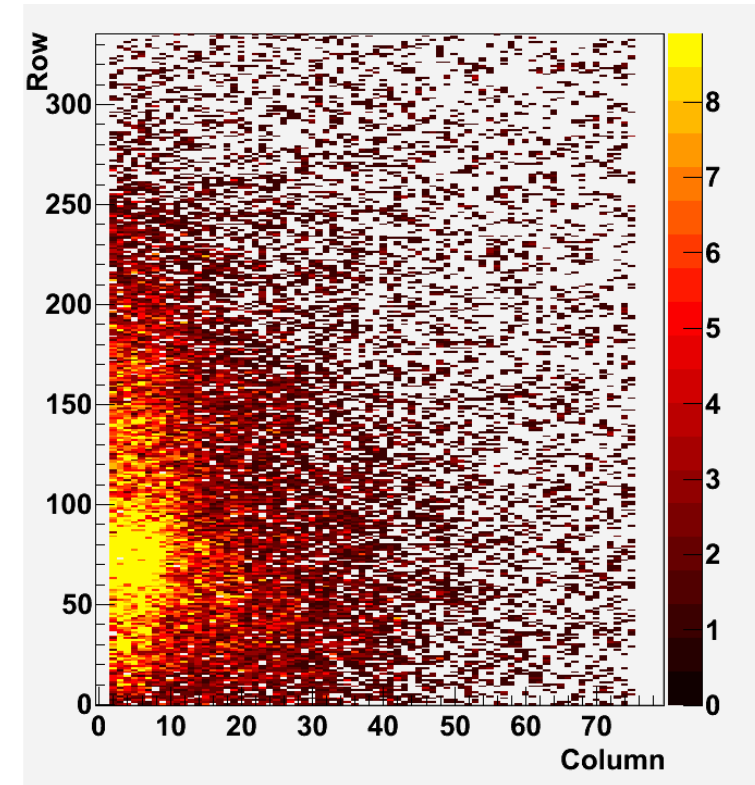
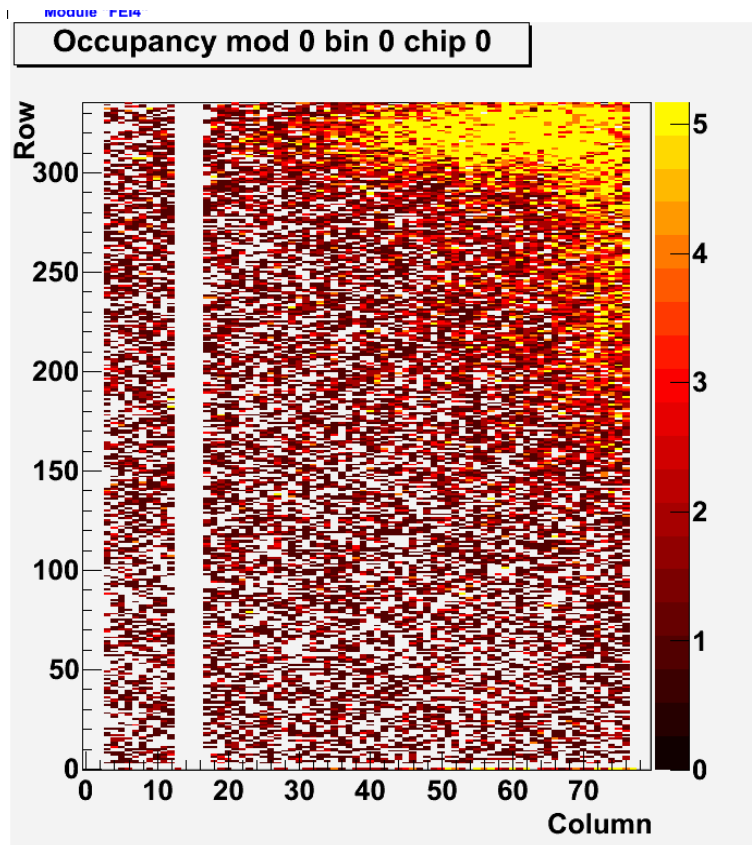
- Tuning seems to be very successful
- Very painless after teething troubles



S. Altenheiner, J. Jentsch

First source scans with neutron irradiated FE-I4 assemblies

- New readout electronic and
- New frontend
- First (neutron) irradiated samples
- Activated (acts as its own source)

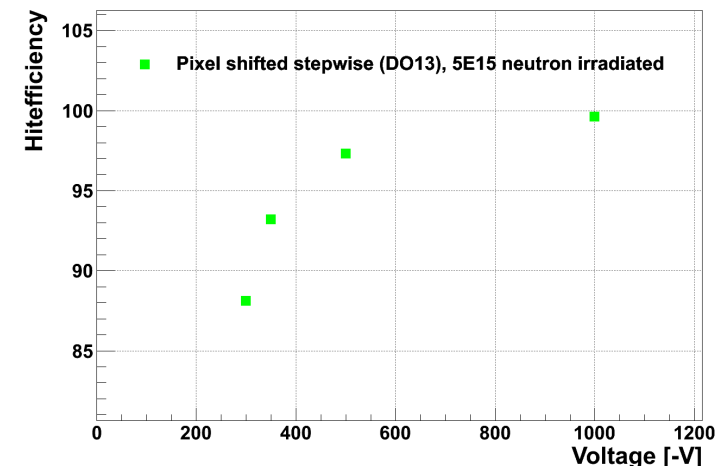


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But nevertheless it works very well!

Conclusions and Outlook

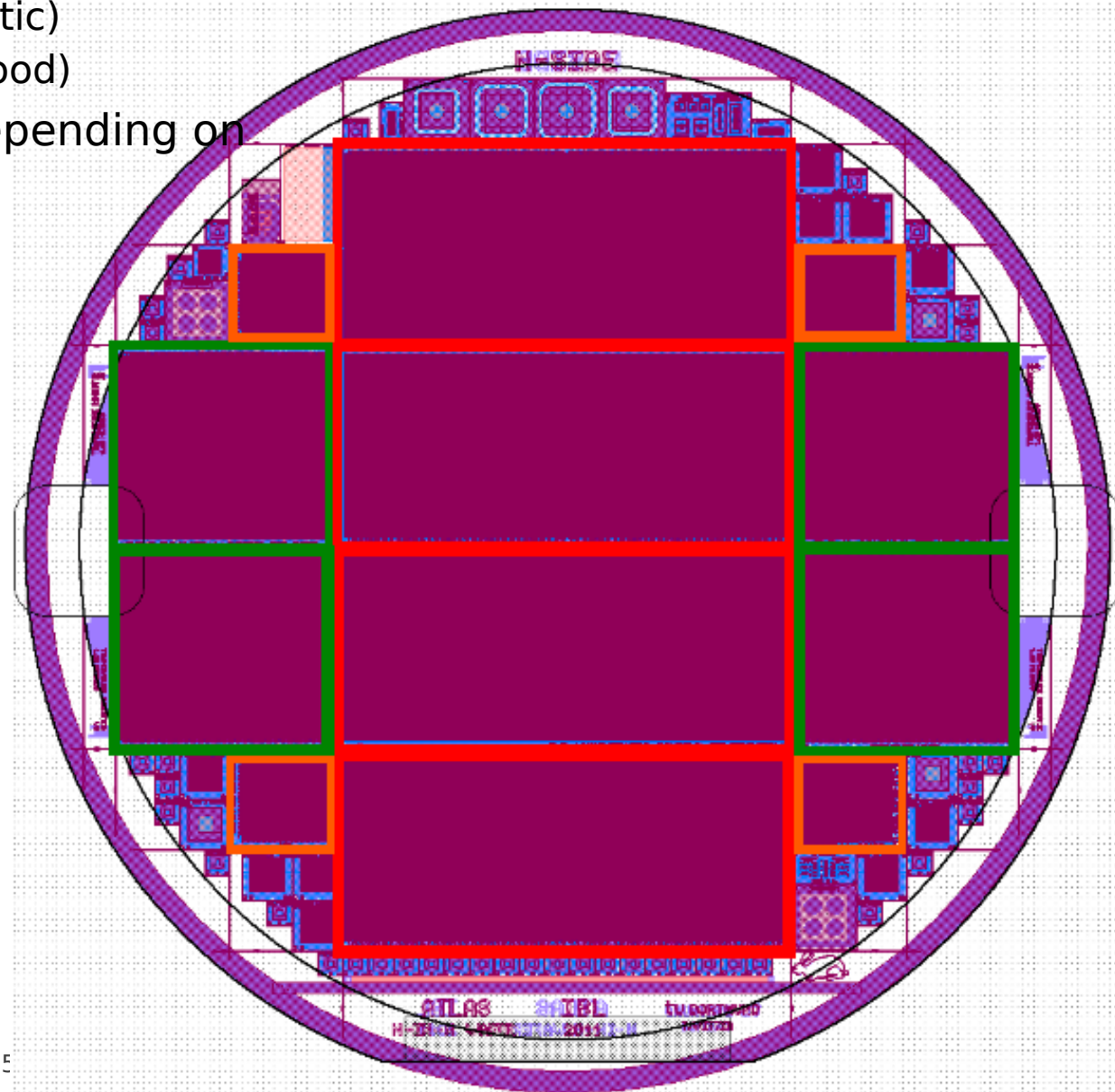
- Lot of progress in the last three years
- Planar pixel sensors still yield charge at 'SLHC innermost layer' conditions
- The n-bulk IBL sensor qualification production was very successful
 - high yield ($\sim 80\%$ for 2-chip modules)
 - slim-edge design ($\sim 200\text{-}250\ \mu\text{m}$ inactive edge) working well
- Planar sensors have been shown to yield more than $10\ \text{ke}^-$ after $5 \cdot 10^{15}\ \text{n}_{\text{eq}}/\text{cm}^2$ at 1 kV
- Hit efficiency with a FE-I3 based readout is at **99.6%** → excellent
- Data with FE-I4 were taken and are currently analyzed
- Operation of irradiated pixel detectors still tricky as FE-I3 not rad-hard enough but new DAQ seems to behave much better under testbeam conditions
- Planar IBL (pre-)production is under way



Backup

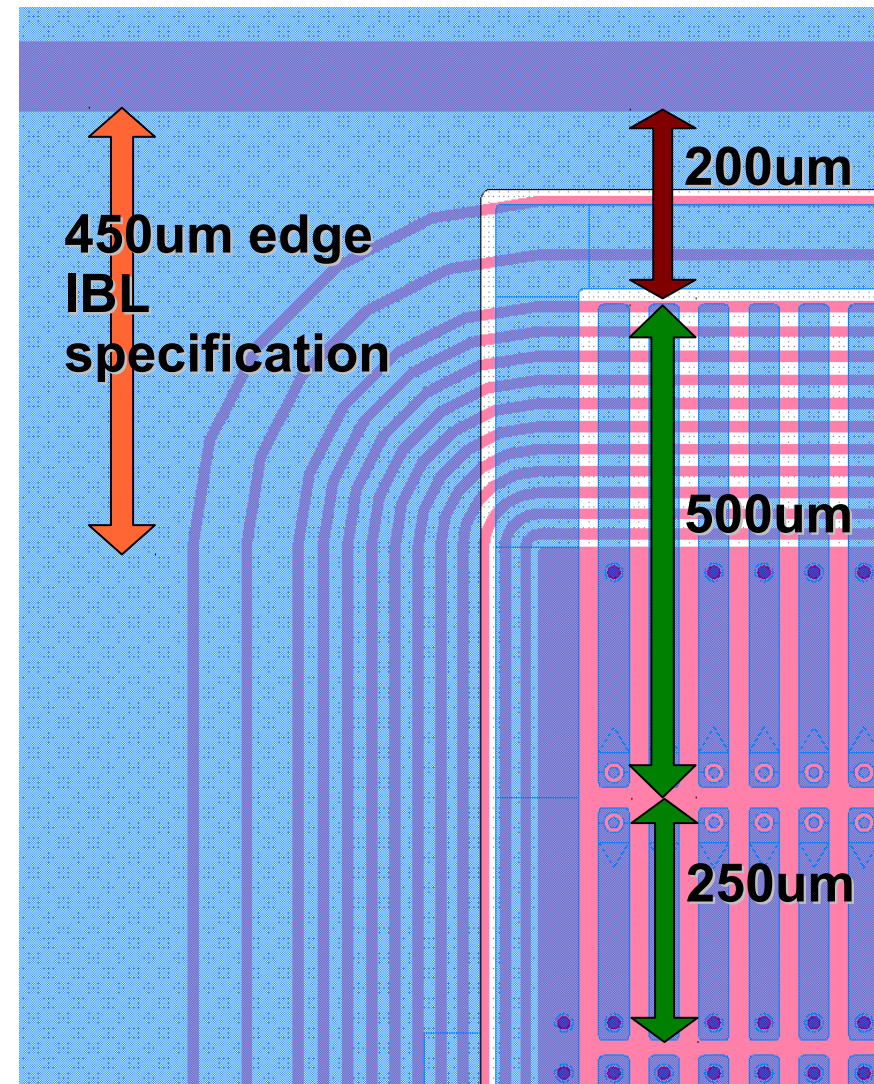
The planar IBL production wafer

- thinning and polishing of raw wafers is outsourced:
 - 250um - 100 wafers (Okmetic)
 - 200um - 50 wafers (Rockwood)
- will decide by mid-march depending on
 - thinning results
 - 200 μm UBM/flipping experience
- 4" n-bulk wafer
 - slim-edge design
 - 4 FE-I4 2x1 MCMs
 - 4 FE-I4 SCs
 - 4 FE-I3 SCs
 - diodes
 - test structures



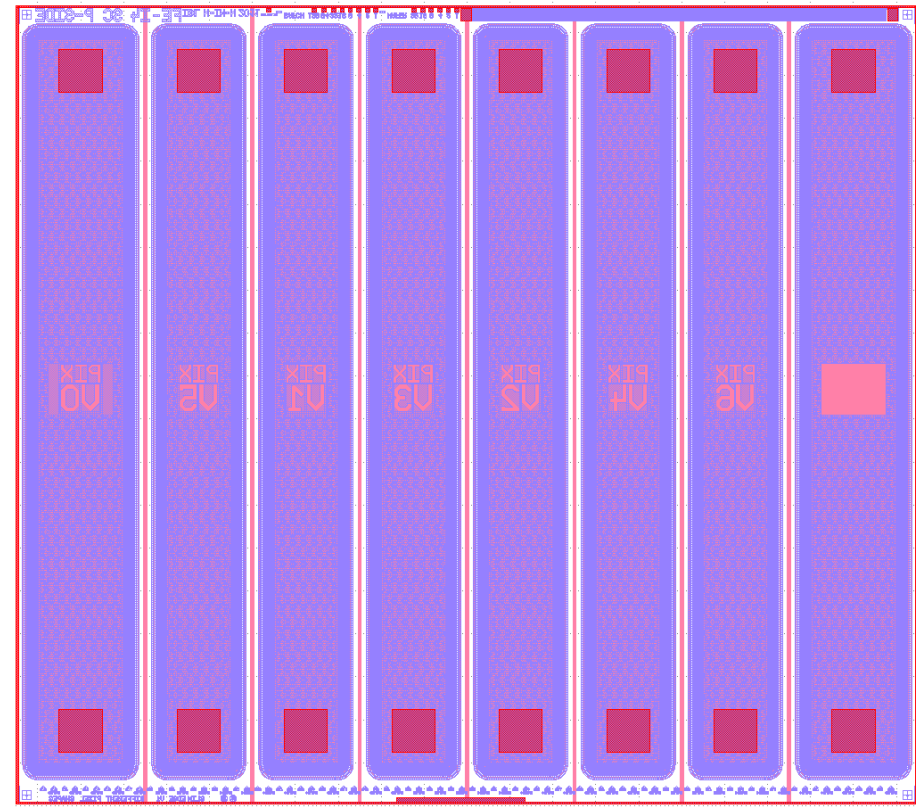
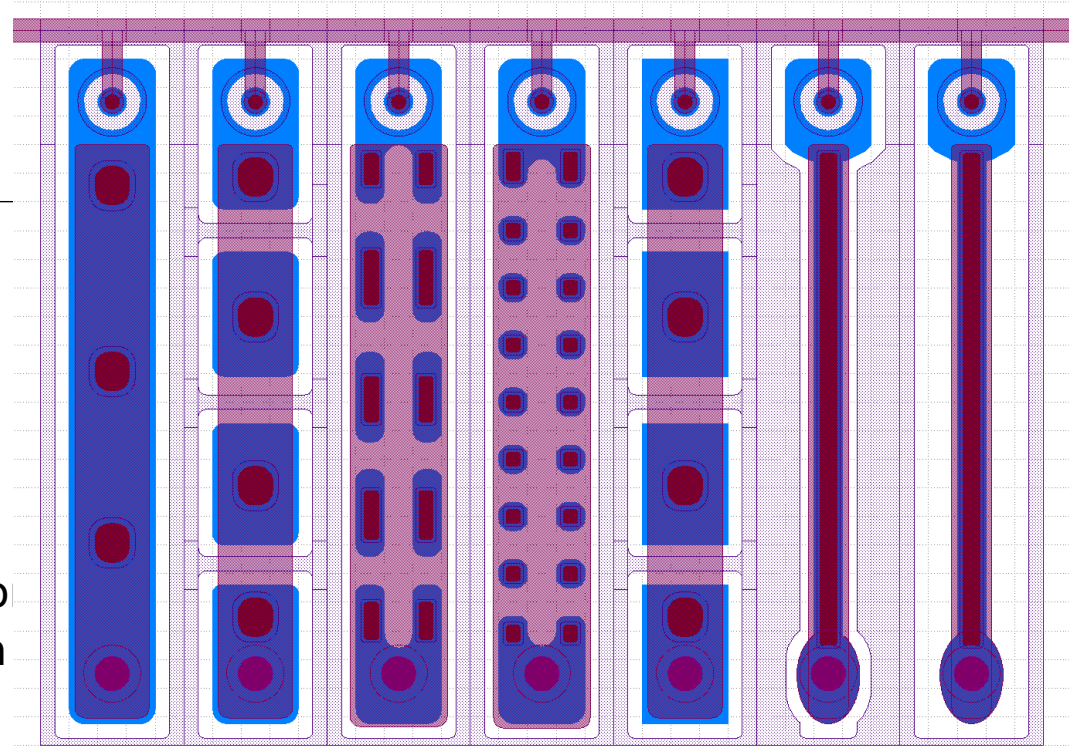
FE-I4 sensor design

- we decided to use the “slim edge” design:
 - with long pixels (500um)
 - 13 guard rings shifted 250um beneath the pixels to reduce the inactive area
 - no disadvantage in comparison to the conservative design
 - only ~200-250um inactive edge expected
- same design for the MCMs and for the SCs
 - for comparability



segmented FE-I4 SC

- on one FE-I4 SC we implemented pixels with different shaped implantations
 - to enforce different field configuratio
 - study of charge amplification at high fluences
- always 5 double columns contain same pixel version
 - every double column will only see one sort of pixels (same capacities)
- The HV-pad is segmented into strips
 - the different pixel versions can be operated seperately
 - possibility to do slim edge studies with two double columns (of each version) opposite of guard rings

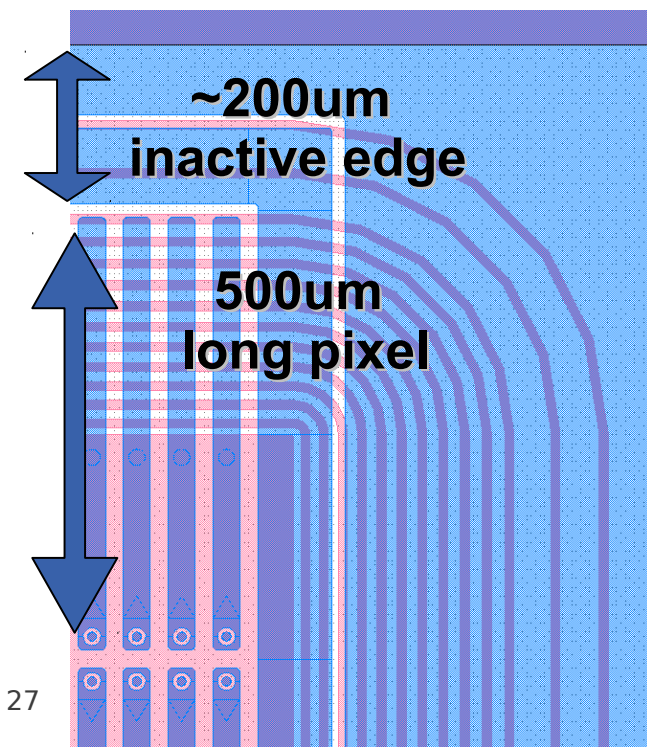
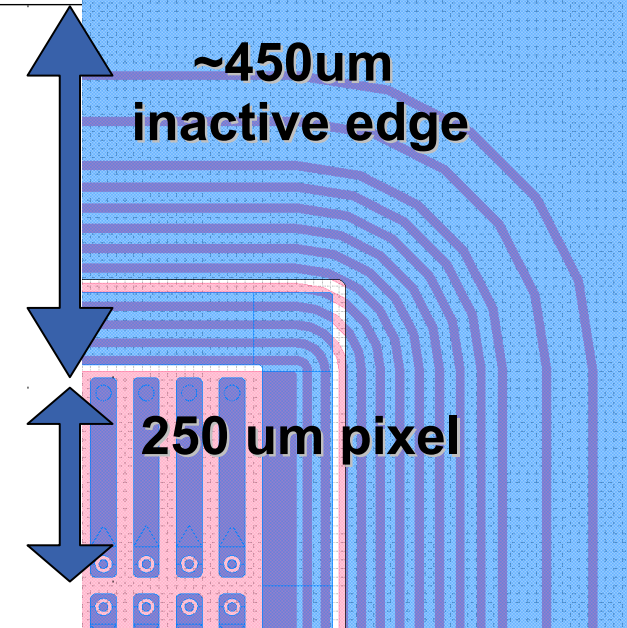


Time schedule

- final design review was held on January 28th
- after final changes the design was submitted to CiS in the begin of February
- 50 wafers will be ordered in March
- time table:
 - Mid-January the wafer-thinning was ordered
 - 4-6 weeks delivery time
 - ~ mid-March: start processing at CiS
 - 16-18 weeks processing time
 - ~ mid-July: wafers delivered from CiS
 - start UBM & dicing at IZM, ~4-6 weeks
 - -> ~ end of August: ~150 2-chip sensors available for flip chipping
- Subsequent order of ~100 wafers could (should?) be placed soon
 - would allow to get ahead of schedule

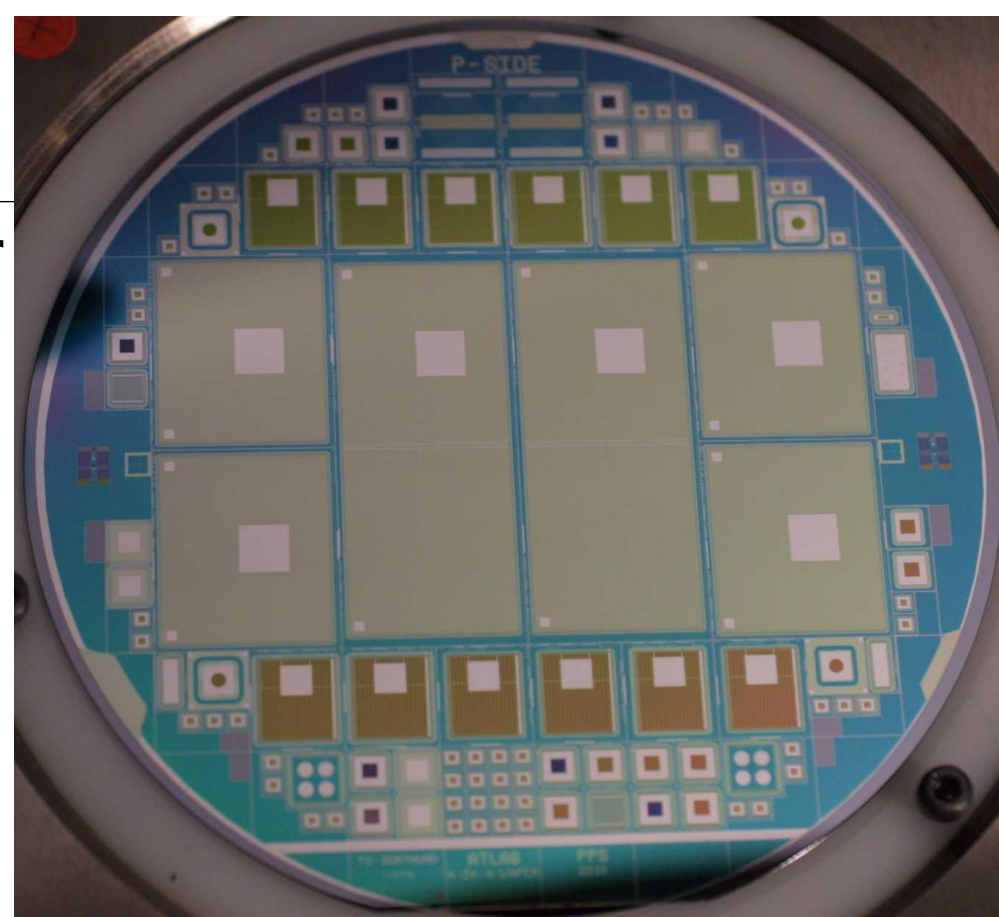
Inactive edge widths

- 2 official n-bulk designs produced:
 - n-in-n: mature technology
 - double sided processing, 4" wafers
 - CiS one of the ATLAS Pixel production vendors
- Conservative design
 - as similar as possible to current ATLAS design
 - ~450 μm inactive edge width
 - electric field at edges homogenous
- Slim edge design
 - guard rings on p-side are shifted beneath the outermost pixels
 - least possible inactive edge (< 200 μm)
 - less homogenous electric field, but charge collection after irradiation dominated by region directly beneath the pixel implant
 - only moderate deterioration expected
- Three parameters:
 - Safety margin (doi:10.1016/j.nima.2010.06.004)
 - Number of guard rings
 - Pixel opposite guard rings



n-bulk qualification wafer

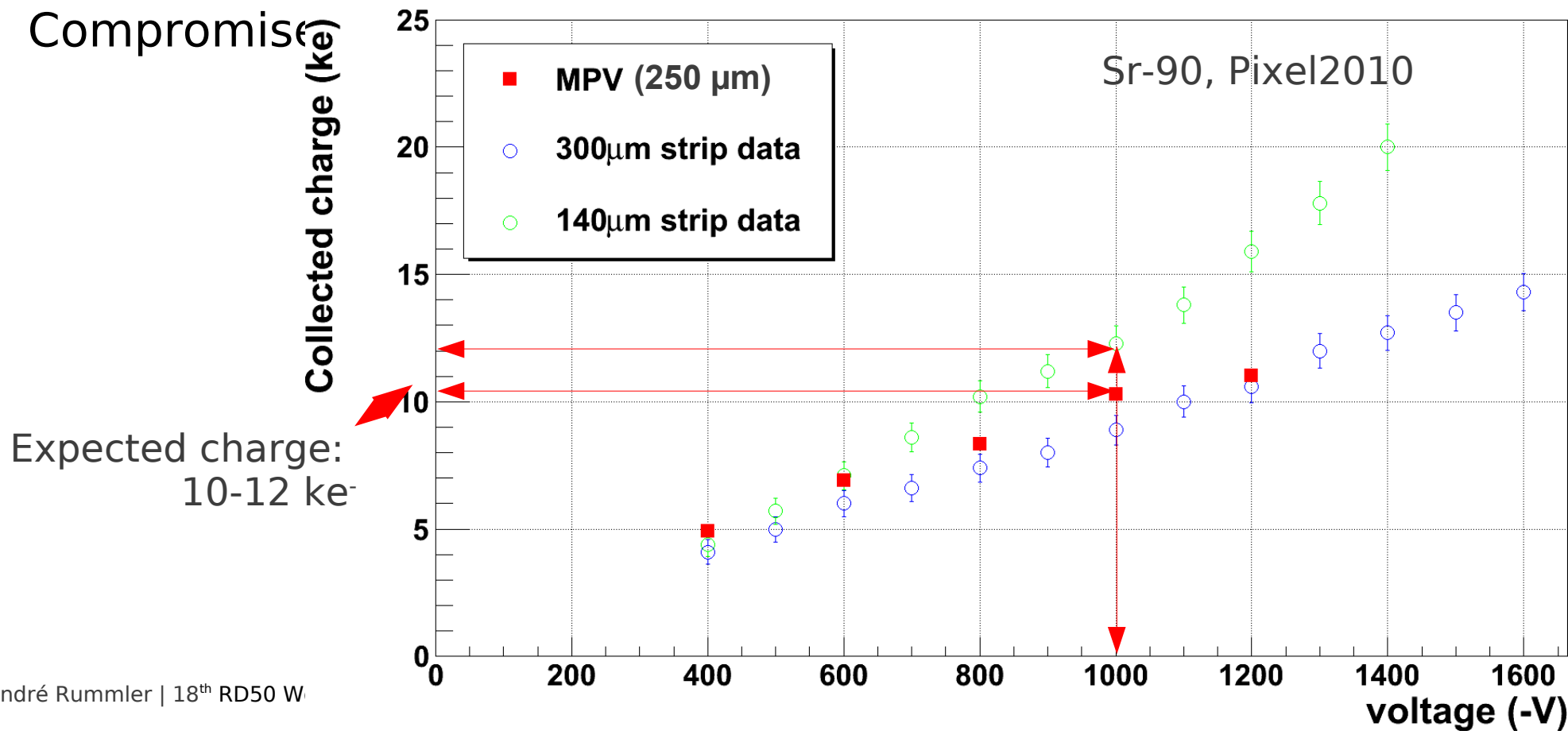
- 6 FE-I4 sensors:
 - conservative (no long pixels, no pixel overlap)
 - slim edge (long pixels (500um), pixels shifted over guard rings)
 - 1 2-chip and 2 1-chip sensors of each design
- 12 FE-I3 SCs
 - various guard ring designs
- diodes, test structures...
- vendor: CiS
- 5 thicknesses:



thickness	wafers ordered	wafers received
250um	12	18
225um	6	11
200um	6	10
175um	6	11
150um	6	8

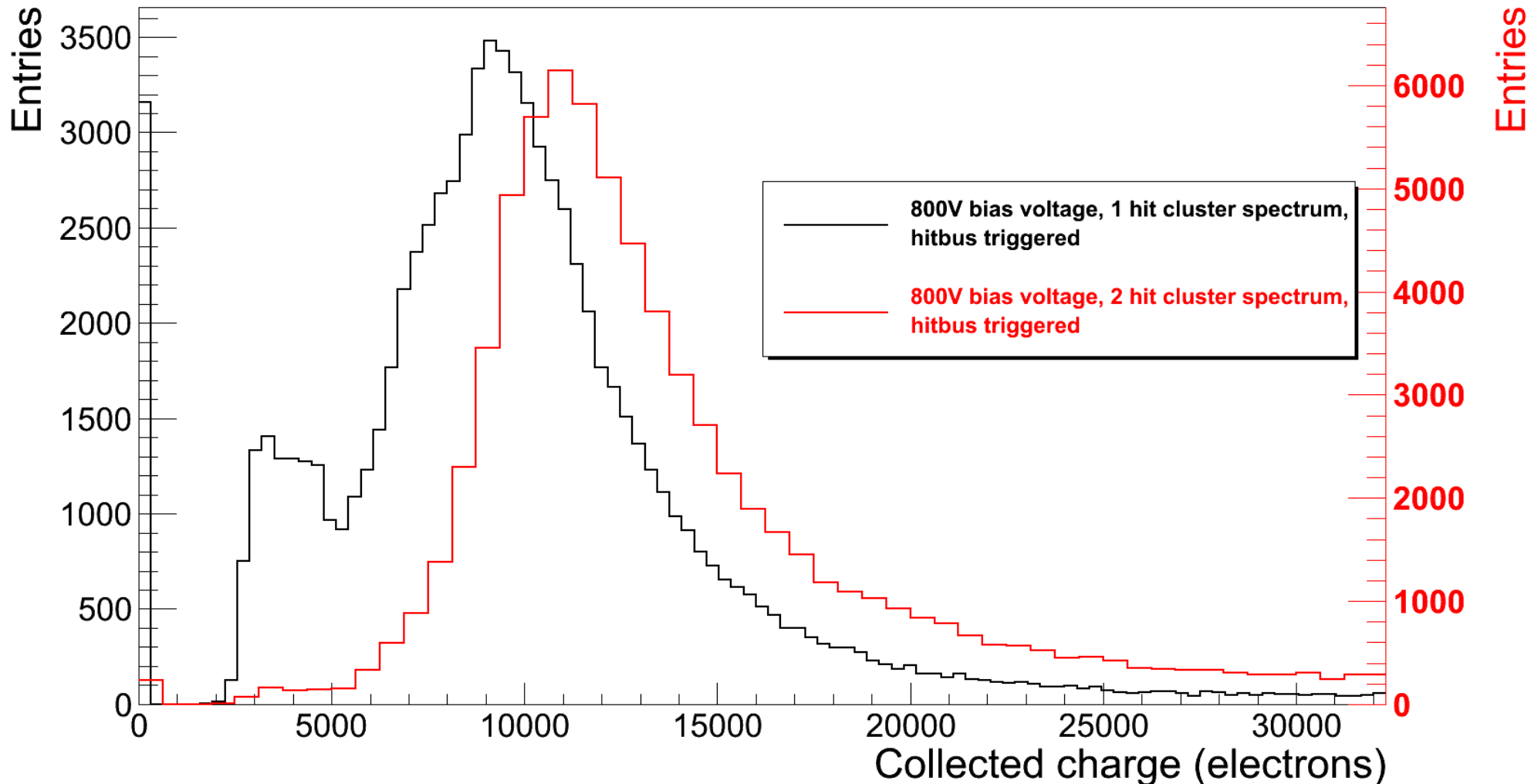
Wafer thickness

- Thinner sensors
 - generate about 1-2 ke⁻ more charge after $5 \cdot 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ at 1 kV
 - have less radiation length
- Baseline: 250 μm (ATLAS production)
- Extreme: 150 μm
- Compromise



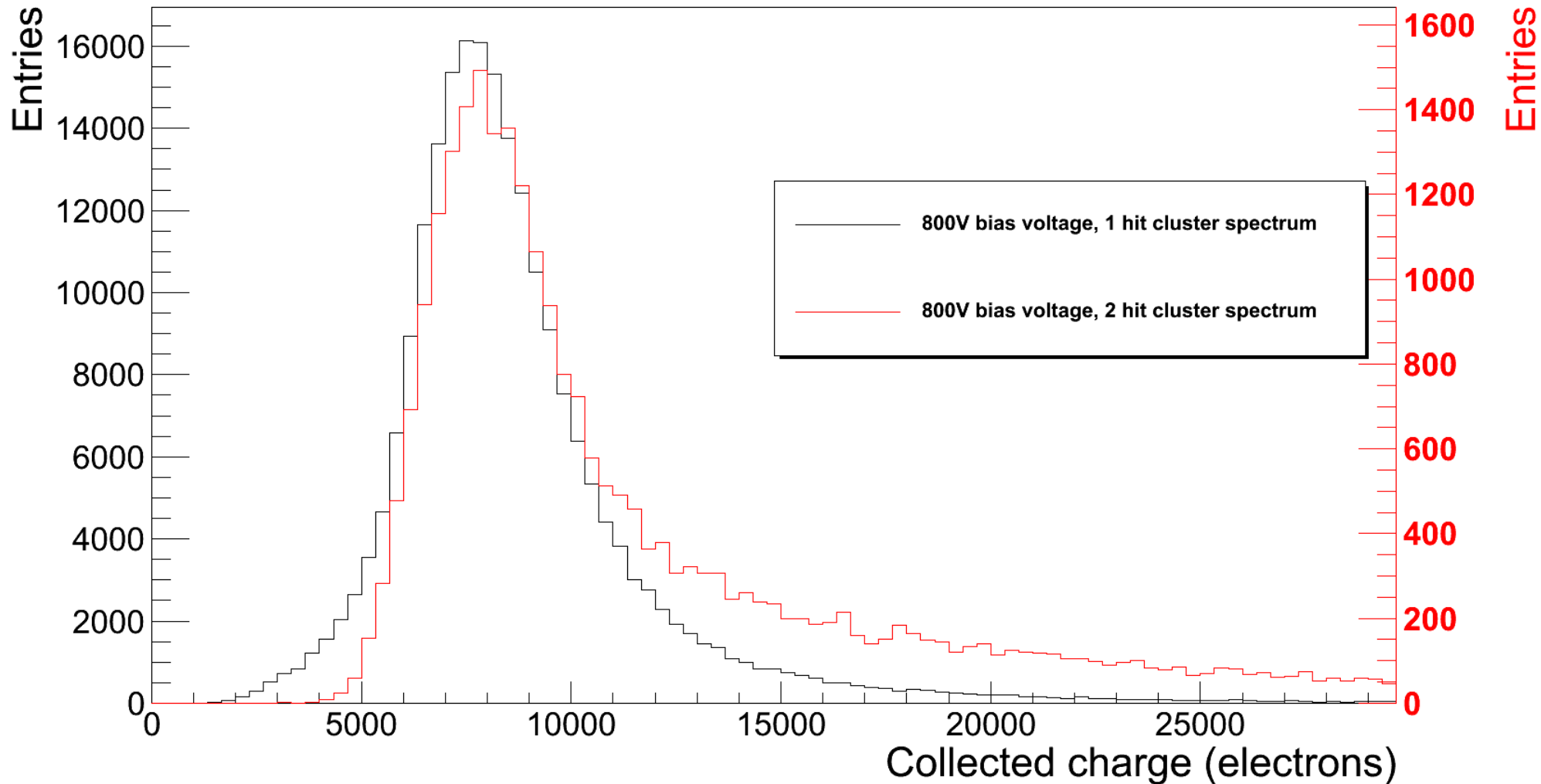
$5 \cdot 10^{15} \text{ n}_{\text{eq}} / \text{cm}^2$ @ 800V, Sr-90 electrons

- Difference between cluster charge of 1-hit and 2-hit clusters:



$5 \cdot 10^{15} n_{eg}/\text{cm}^2 @ 800\text{V}, \text{pions}$

- With pions, this effect is negligible

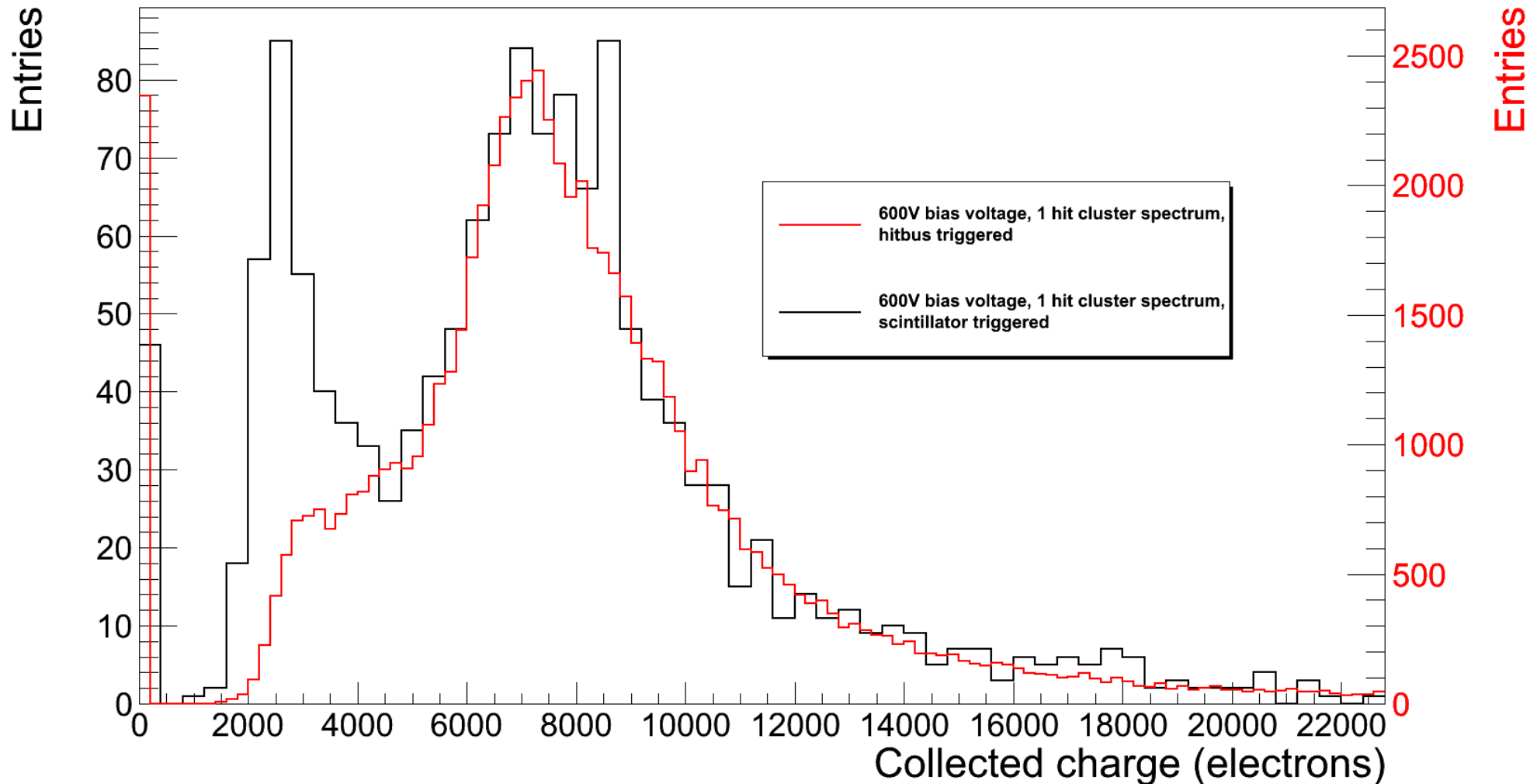


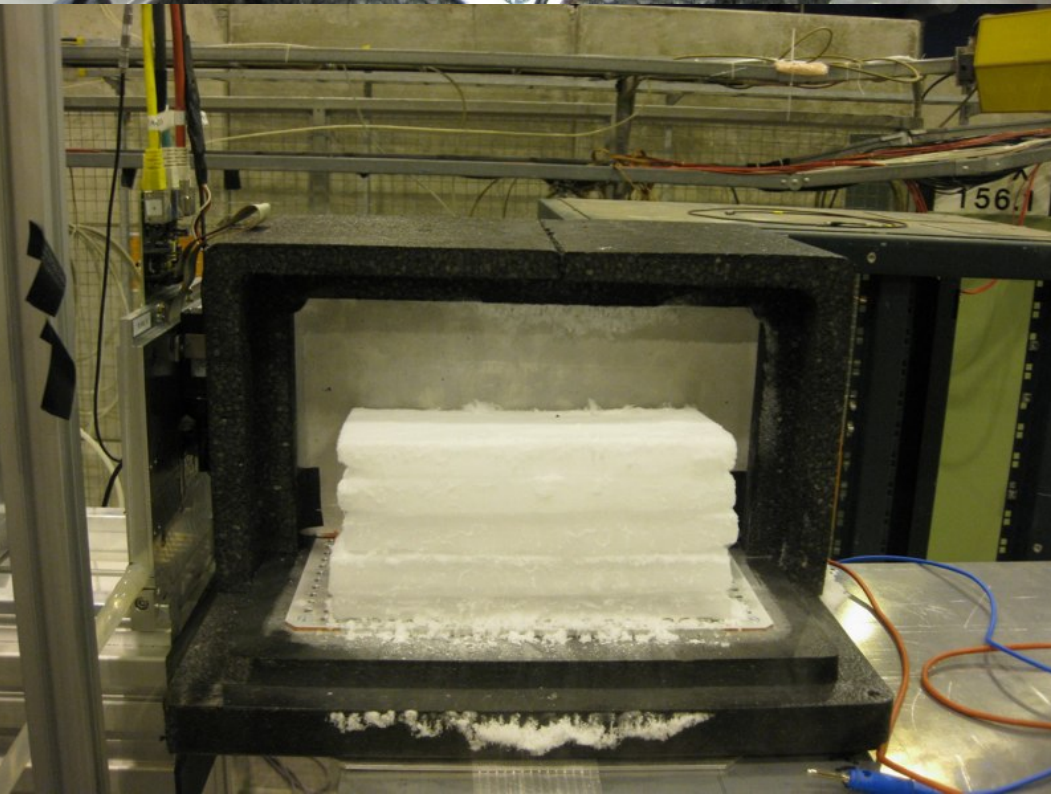
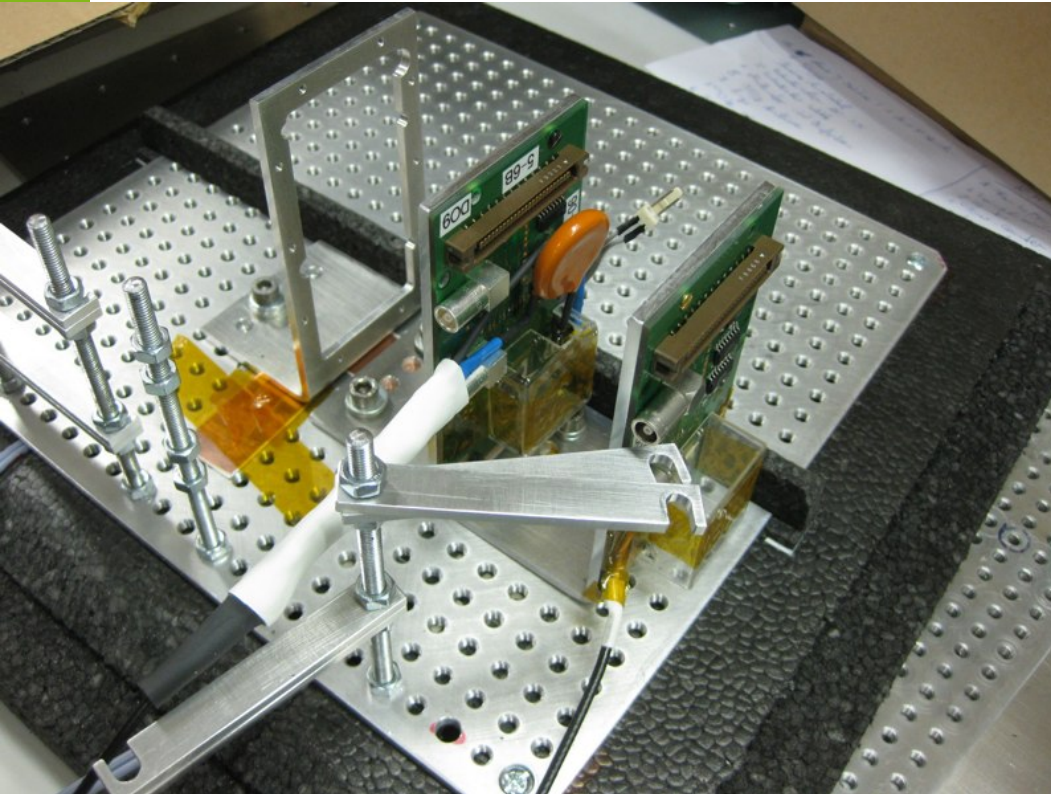
1 hit vs. 2 hit clusters

- For testbeam data with high energy pions there seems to be little difference between the charge spectra of 1-hit and 2-hit clusters.
- Low energy electrons (Sr-90) show increased charge deposition for two hit clusters
→ Only 1 hit clusters regarded for Sr-90 data, conservative choice

Trigger: $5 \cdot 10^{15} \text{ n}_{\text{eg}} / \text{cm}^2$ 600V electrons

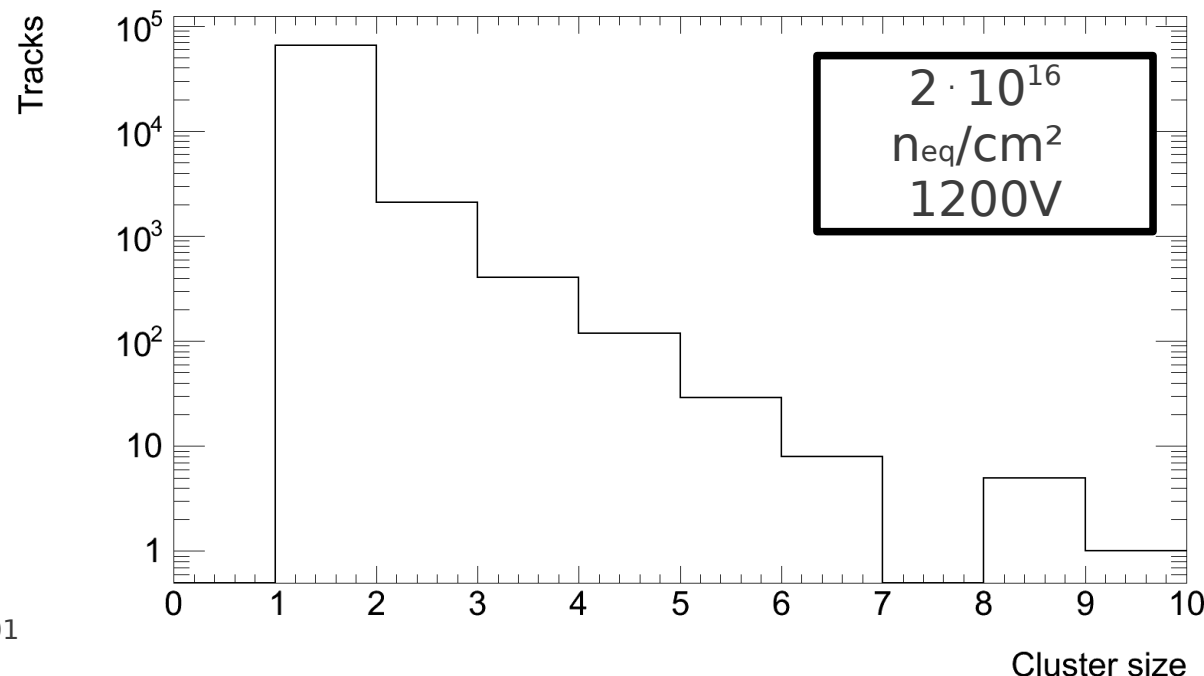
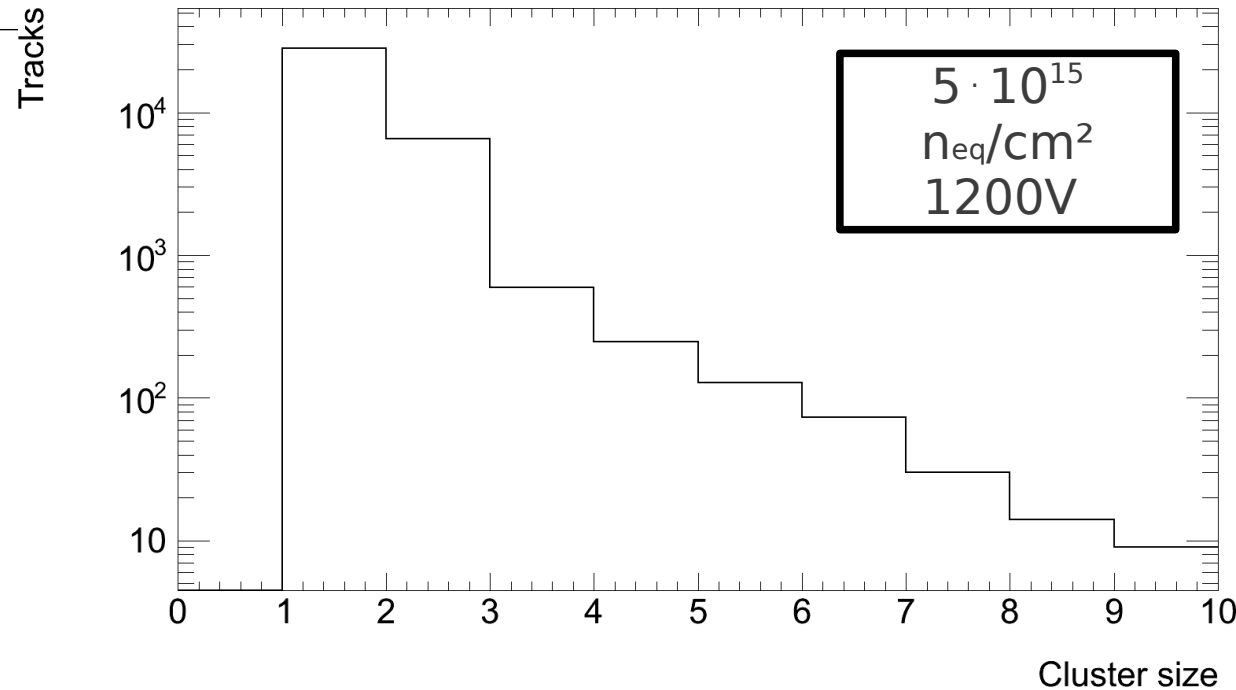
- No visible difference for MPV between scintillator and hitbus-triggered data



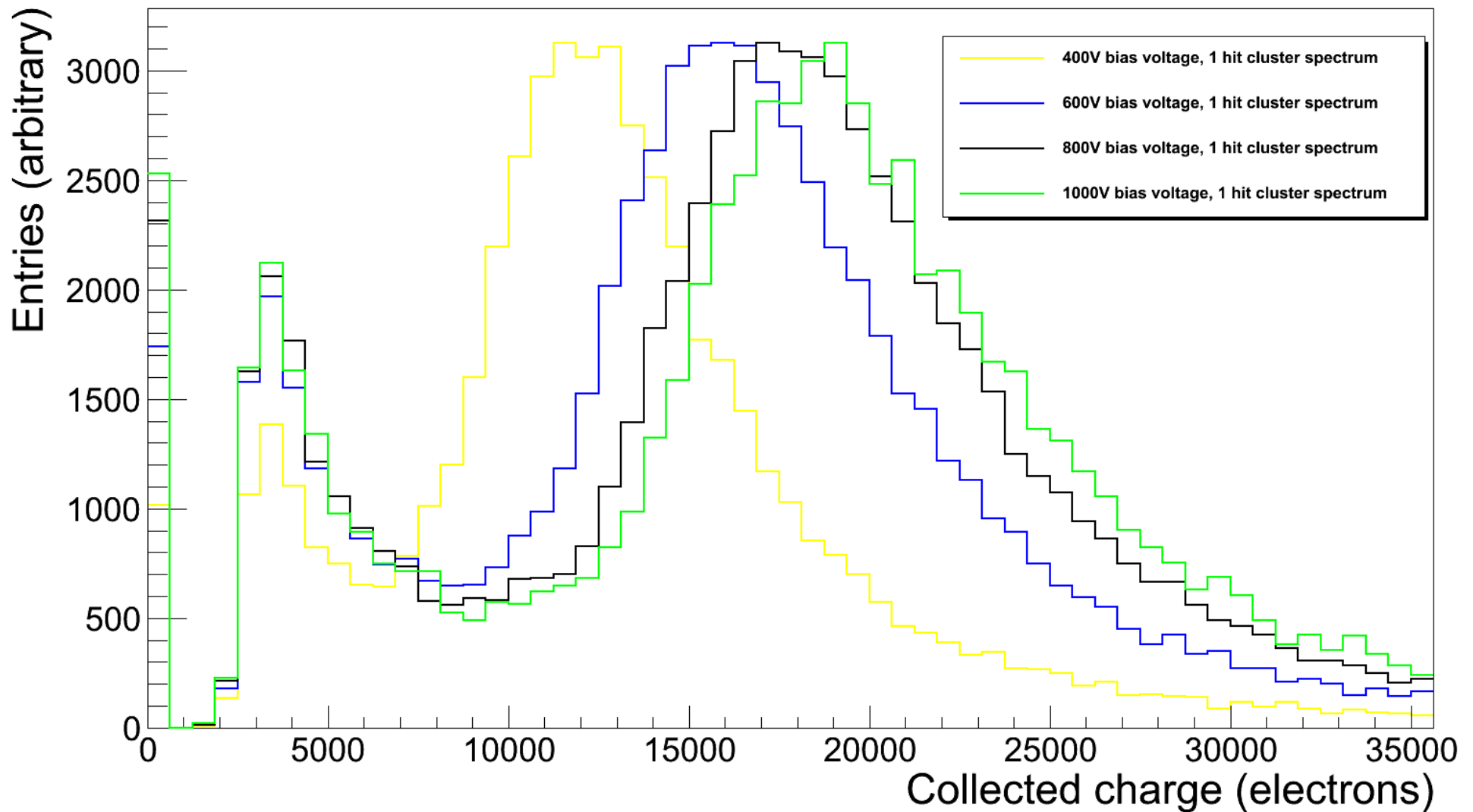


Charge sharing?

- Single-hit cluster fraction grows with fluence (as expected)
- (Much) more shared charge not seen due to threshold effect in the neighbouring pixel
- Scattering is larger with electrons, might (partially) explain lower observed charge with electrons

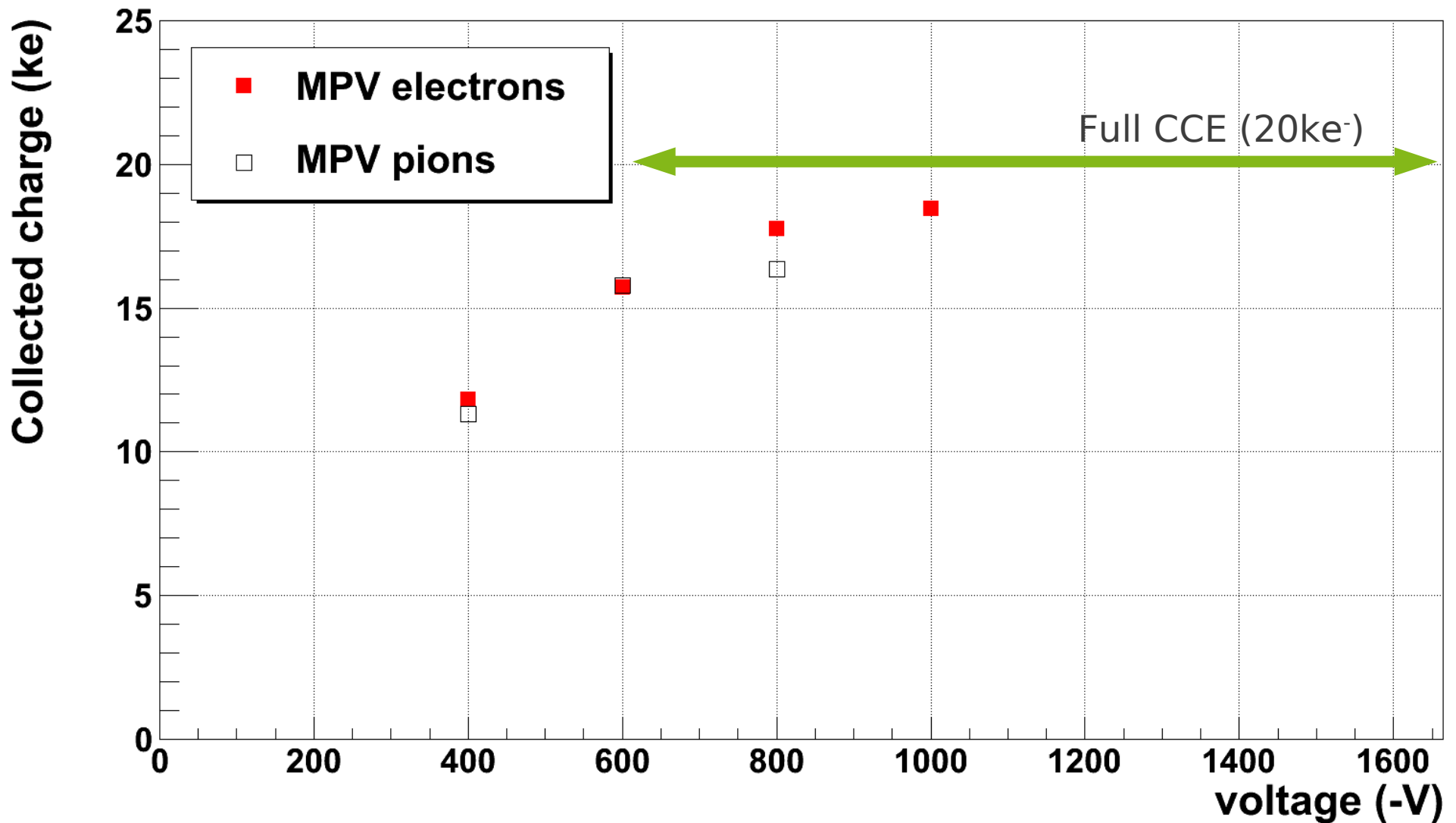


$1 \cdot 10^{15} n_{eq}/cm^2$ with Sr-90 electrons

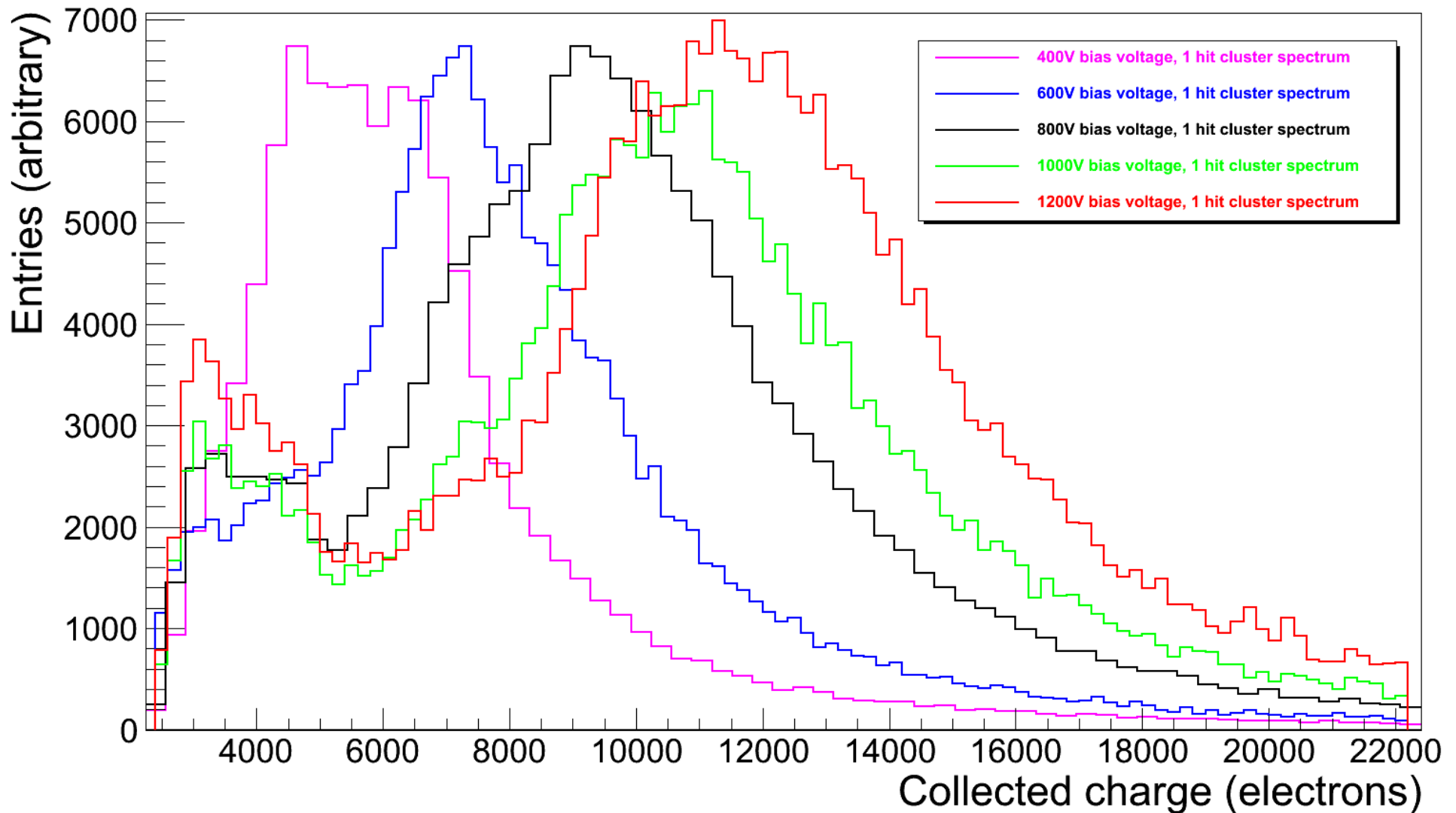


$1 \cdot 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ charge collection summary

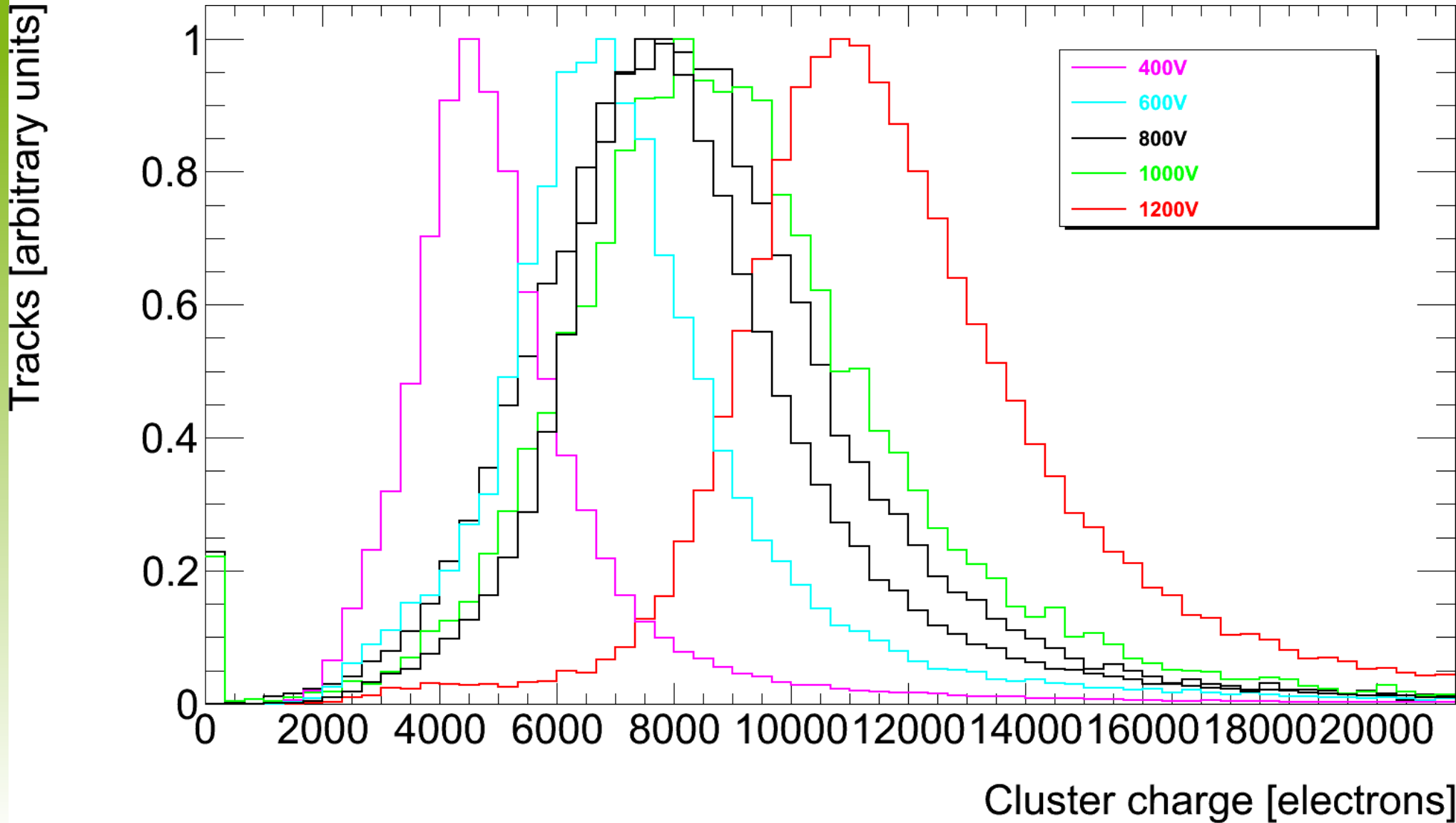
- satisfactory results: 16 ke⁻ at 600V, almost full CCE at 1kV
- agreement with pion measurements



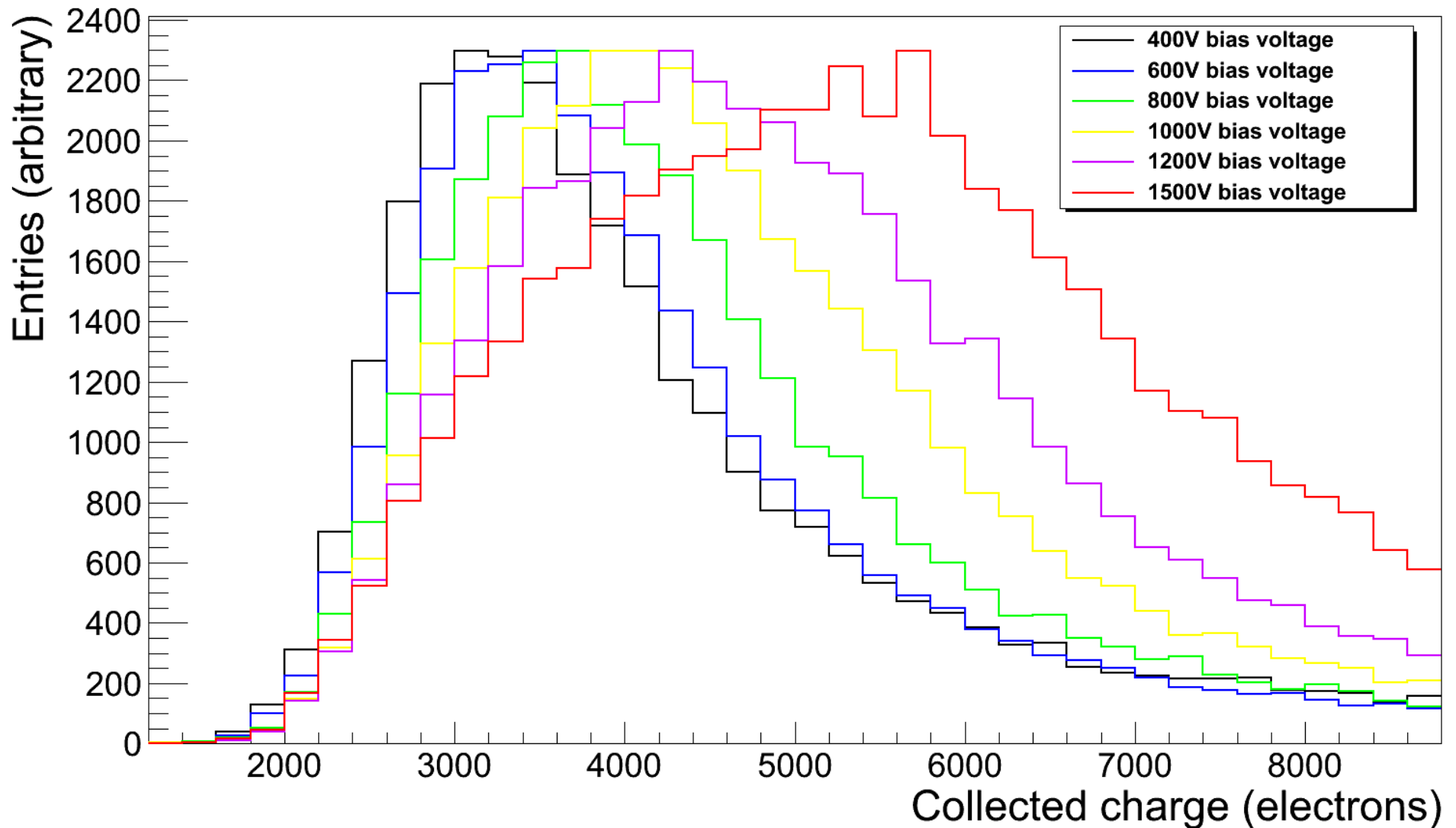
$5 \cdot 10^{15} n_{eq}/\text{cm}^2$ with Sr-90 electrons



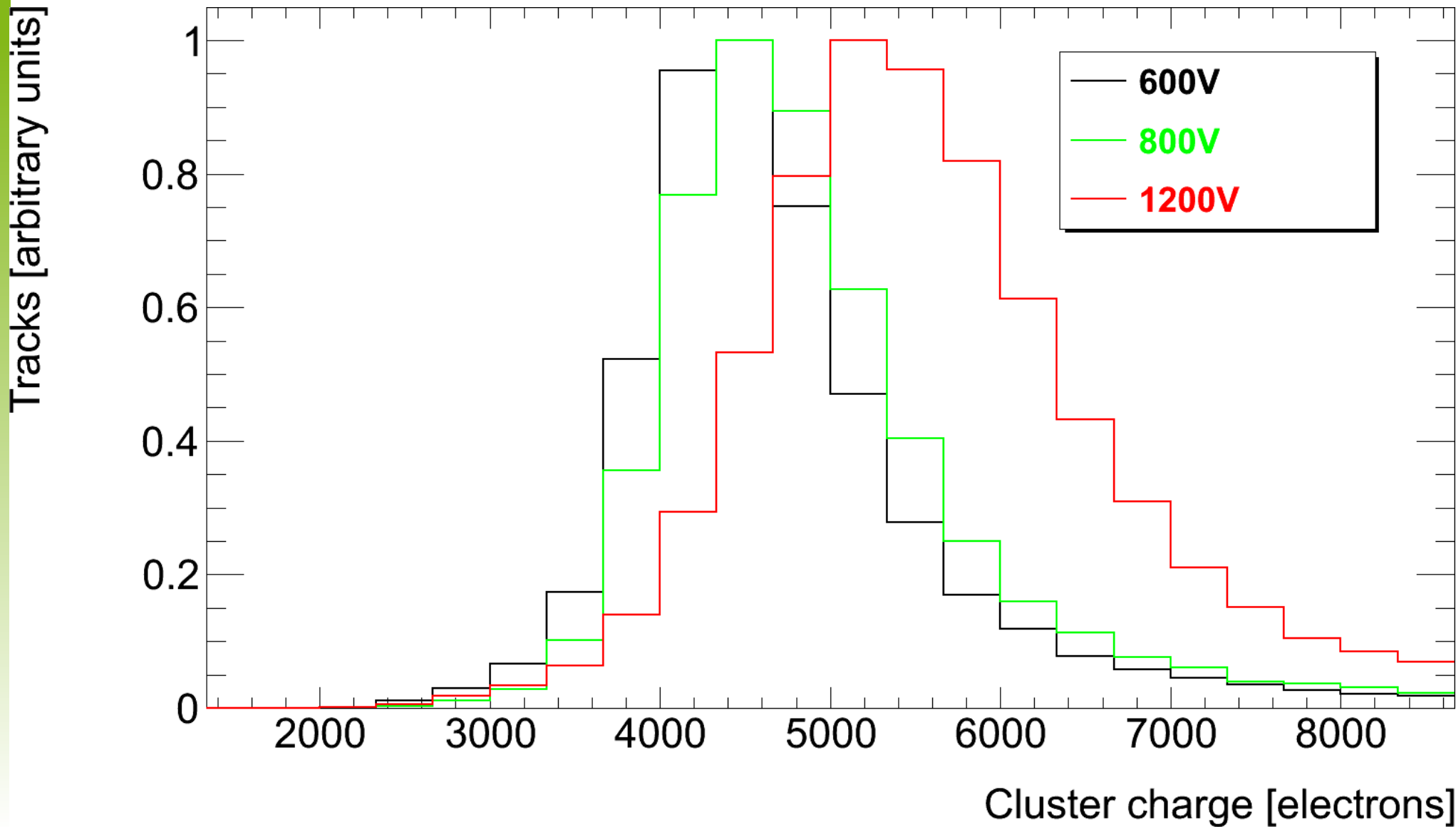
$5 \cdot 10^{15} n_{eq}/\text{cm}^2$ with pions



$2 \cdot 10^{16} n_{eq}/\text{cm}^2$ with Sr-90 electrons



$2 \cdot 10^{16} n_{eq}/\text{cm}^2$ with pions



Integrated temperature sensors

- next to all 4 FE-I4 SC sensors a loop of metal conductor is implemented on the p-side
- possibility to determine the sensor temperature via measurement of (temperature depending) resistance
- length of $\sim 1.2\text{m}$
 - resistance in the order of $\sim 1\text{-}10\text{k}$ ohms
- two dicing streets to have the possibility of cutting away the loop or leave it attached to the sensor
- on three FE-I4 SCs and one MCM a shorter loop ($\sim 21\text{cm}$ length) is implemented in the edge of the sensor (within the dicing streets)

