ALICE

MAPS-based tracker developments from ITS3 towards FCC-ee

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Outline

- ALICE Upgrades and FCC-ee **common challenges**

- **ITS3**: ALICE vertex detector upgrade for **LHC Run 4**
  - Ultra-thin, truly cylindrical, wafer-scale MAPS

- **ALICE 3**: future heavy-ion experiment for **LHC Run 5** and beyond
  - Compact all-silicon MAPS tracker, from 5 mm to

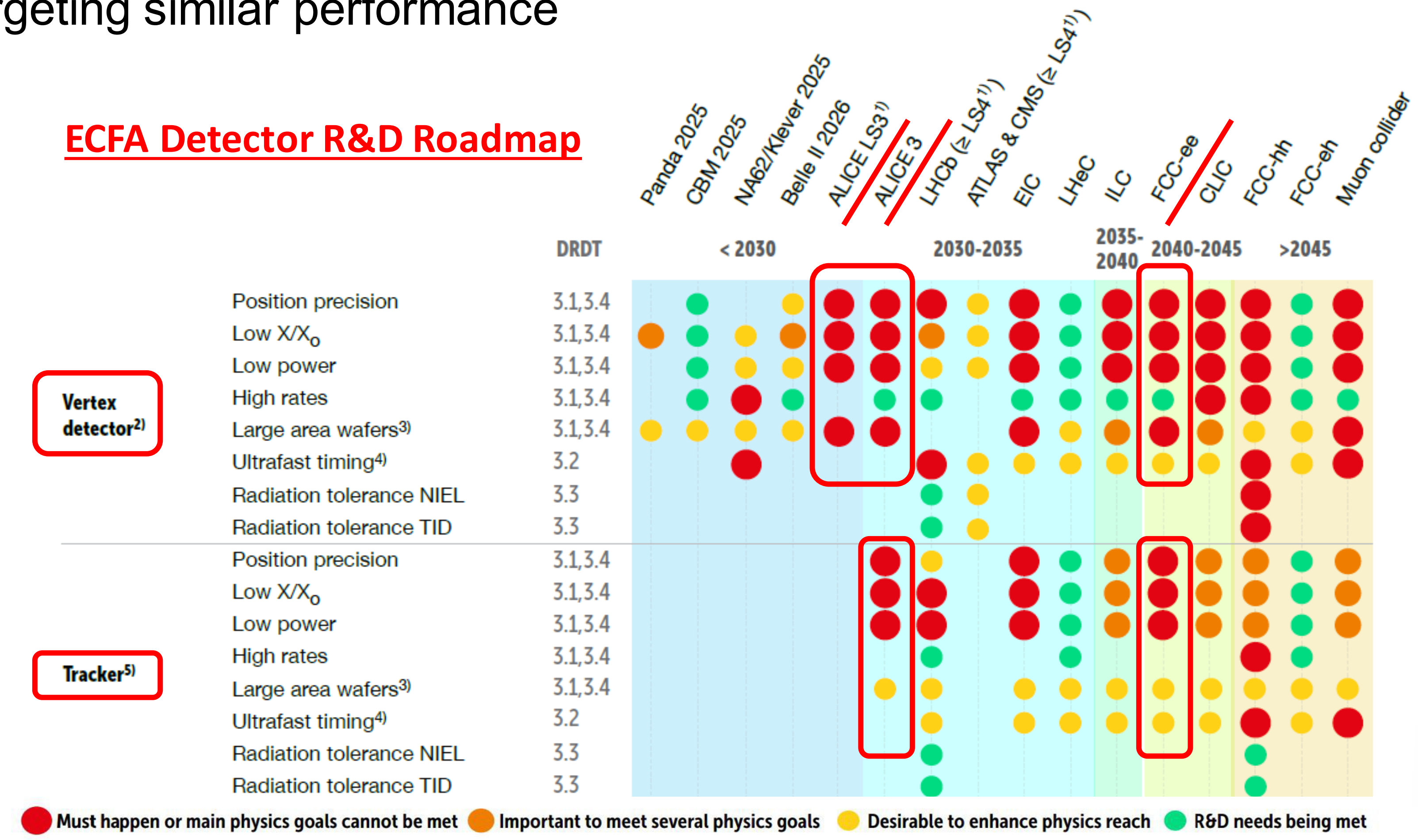
- Conclusions

ALICE Upgrades and FCC-ee common challenges

- The ALICE silicon upgrades planned for LHC LS3 and LS4 and the FCC-ee vertex and tracker detectors are targeting similar performance

Can the R&D for ITS3 and ALICE 3 serve as a stepping stone for FCC-ee vertex and tracker detectors?

ECFA Detector R&D Roadmap



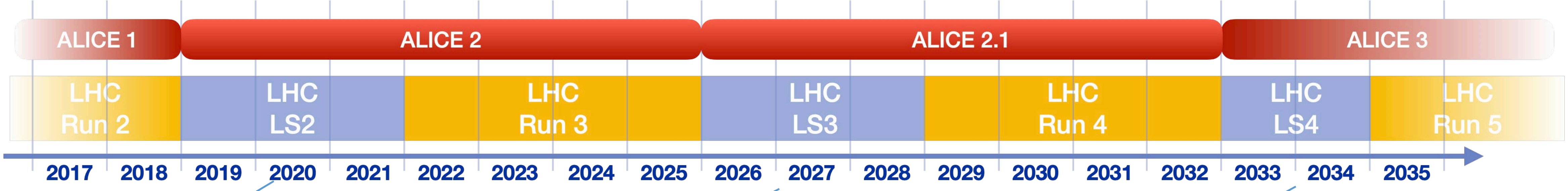
ALICE Upgrades and FCC-ee common challenges

- The ALICE silicon upgrades planned for LHC LS3 and LS4 and the FCC-ee vertex and tracker detectors are targeting similar performance

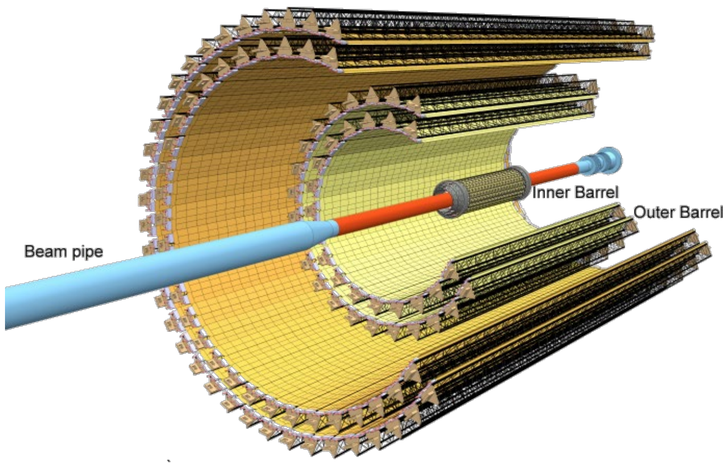
Target performance	ITS3	ALICE 3	FCC-ee
Position precision	$5\ \mu m$	$2.5\ \mu m$	$3\ \mu m$
X/X_0 per layer	0.09% *(average)* 0.07% *(most of active region)*	$0.1\ \%$	$0.3\ \%$
Power consumption	$40\ mW/cm^2$ *(active region)*	$20\ mW/cm^2$	$50\ mW/cm^2$
NIEL	$10^{13}\ 1MeV\ n_{eq}\ /cm^2$	$10^{16}\ 1MeV\ n_{eq}\ /cm^2$ *(LOI, *)*	$\sim 6 \times 10^{12} n_{eq}/year$
TID	$1\ Mrad$	$300\ Mrad$ *(LOI , *)*	$\sim 3.4\ Mrad/year$
Maximum hit rate	$< 10\ MHz/cm^2$	$94\ MHz/cm^2$	$400\ MHz/cm^2$ *(*)*

** = being revised*

ALICE silicon tracker development path

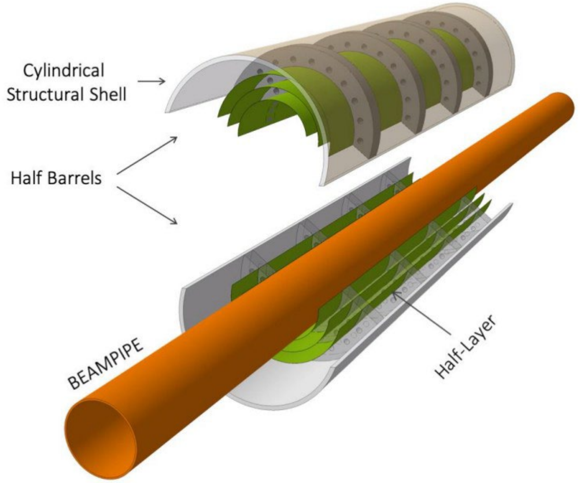


ITS2



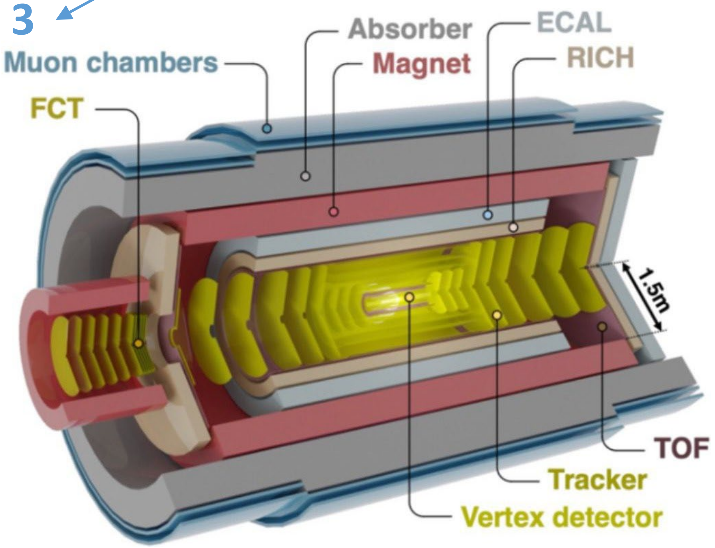
[ALICE Upgrades during LHC LS2]

ITS3



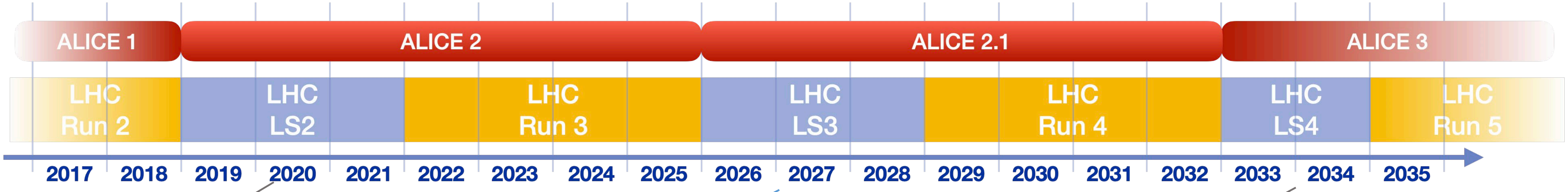
LOI: CERN-LHCC-2019-018
TDR: CERN-LHCC-2024-003

ALICE 3

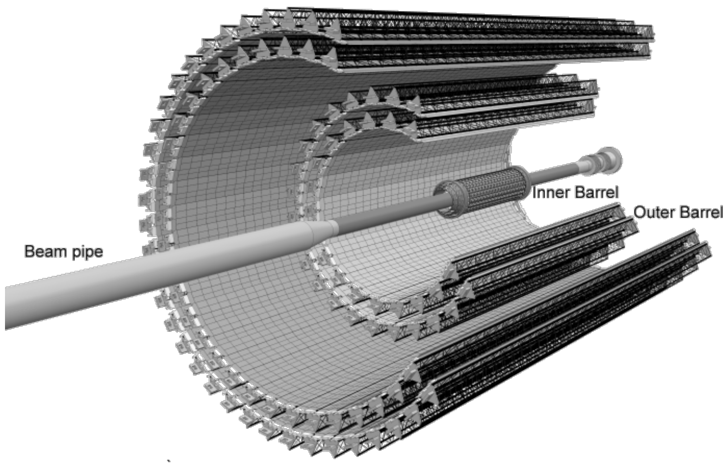


LOI: CERN-LHCC-2022-009
Scoping Document in preparation

ALICE silicon tracker development path

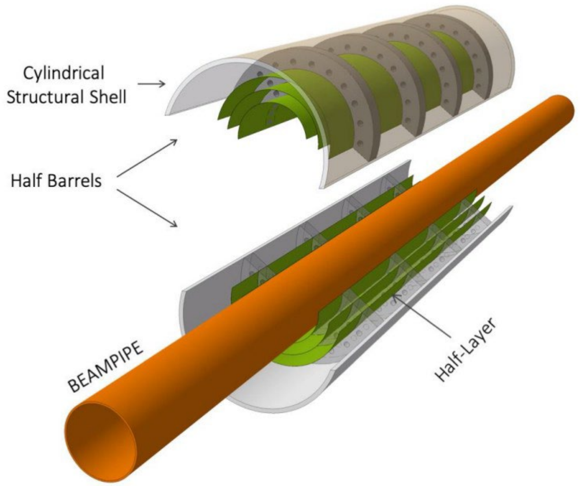


ITS2



ALICE Upgrades during LHC LS2

ITS3



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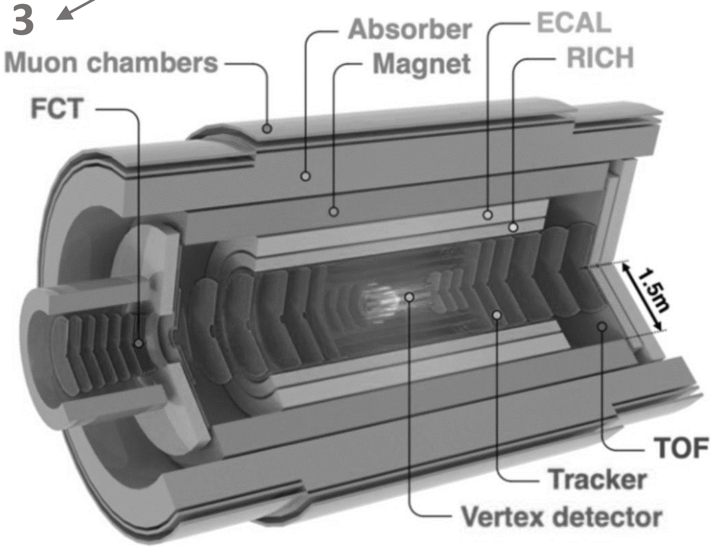
ALICE 3



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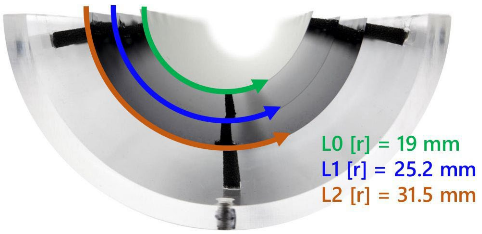
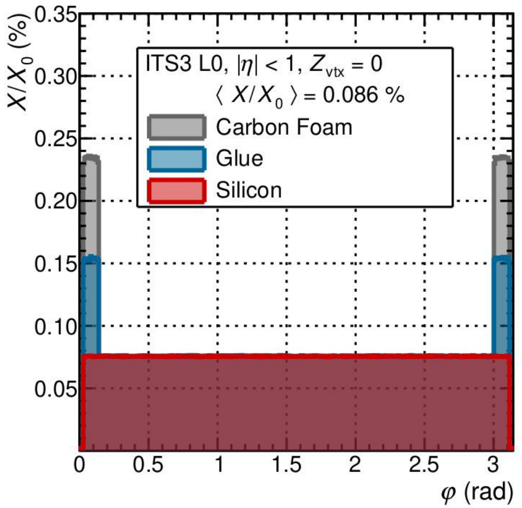
ITS3 layout and material budget

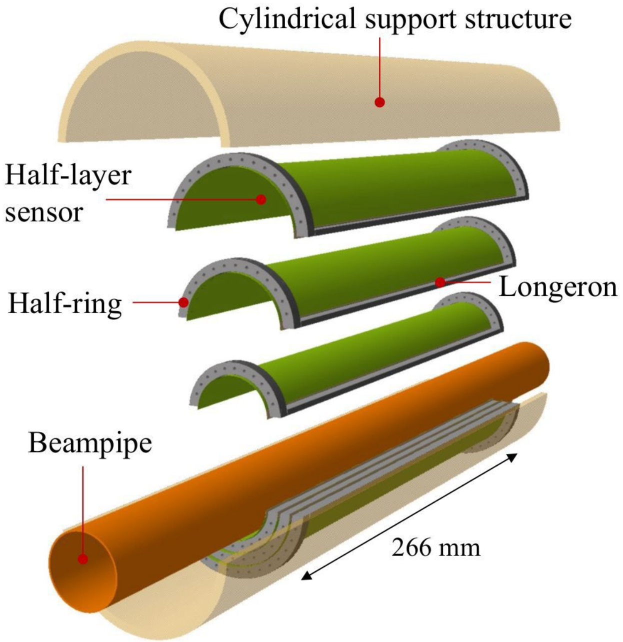
- **3 layers of curved, ≤ 50 µm thick, wafer-scale MAPS in TPSCo 65 nm CMOS process**
  - Replacing ITS2 Inner Barrel (innermost radius reduced from 24 mm to **19 mm**)
  - Each half-layer made of one wafer-size **flexible sensor**
  - **In-silicon** data transmission and power distribution
  - Minimal **carbon foam** support structures
  - **Air cooling**





Minimal material budget: ~0.09% X_0 on average

- **Uniform ~0.07% X_0** on most of the acceptance
- Longerons at the equatorial long edges of the half-layer
- Half-rings at the bent ends of the half-layer



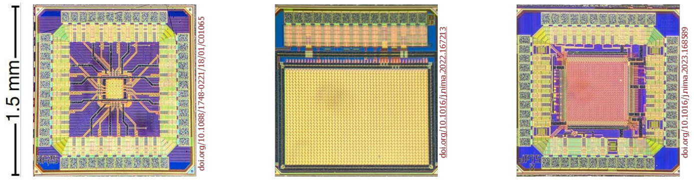
ITS3 chip development plan

PAST

PRESENT

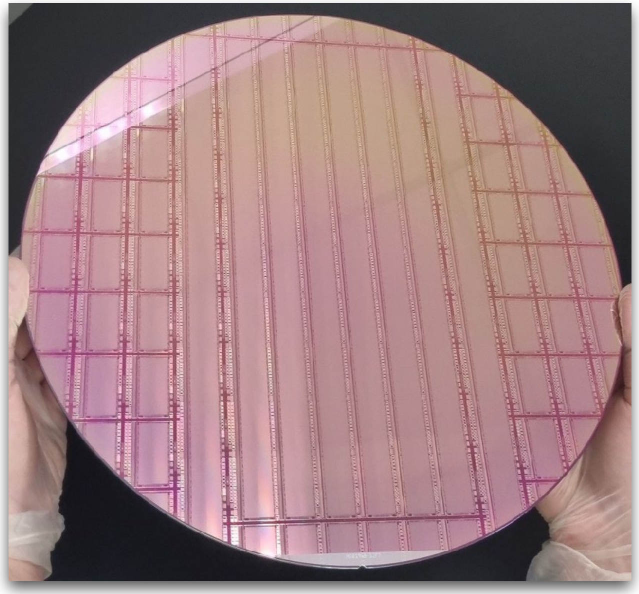
FUTURE

- Multi-Layer Run 1 (MLR1): **first MAPS in TPSCo 65 nm** CMOS
  - Transistor test structures
  - Analog and digital test structures
  - Achieved goal: **full process qualification**



APTS CE65 DPTS

- Engineering Run 1 (ER1): **first large area** sensors
  - Main goals: **excercize and validate stitching**
  - Chips work, main yield issue understood
  - Full characterization currently ongoing



ER1 wafer

- Engineering Run 2 (ER2): **first ITS3 sensor prototype**
  - Now: **specifications frozen**, design being finalized
  - Submission to foundry planned for Fall 2024
- Engineering Run 3 (ER3): **ITS3 sensor** production

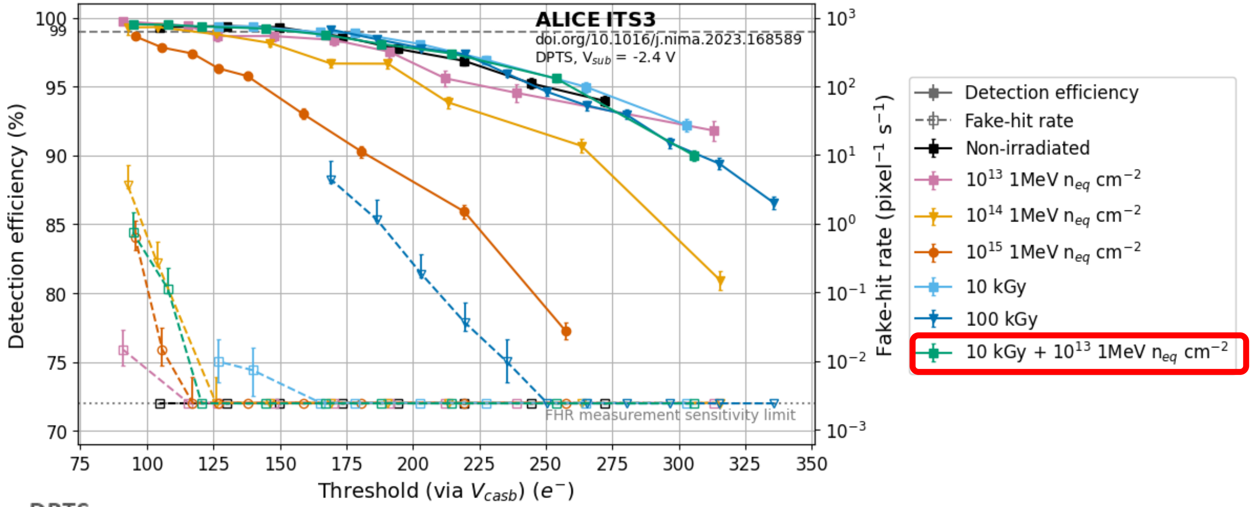
65 nm CMOS process validation and radiation hardness

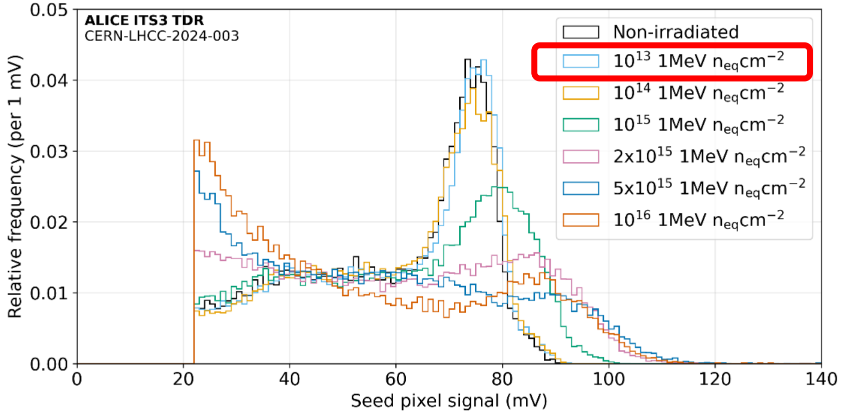
TPSCo **65 nm CMOS process validated** on MLR1 test structures:

- Efficiency > 99%
- Fake-hit rate < $2 \cdot 10^{-3}$ pix^{-1} s^{-1}

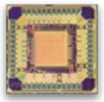
} over a wide operating range

- Radiation hardness demonstrated beyond **10 kGy + 10^{13} 1MeV n_{eq} cm^{-2}** *ITS3 requirement*
  - Still efficient with 10^{15} 1MeV n_{eq} cm^{-2} at room temperature



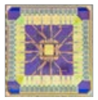


DPTS



Detection efficiency and fake-hit rate Vs threshold and irradiation levels, as measured on 15 μm pitch **Digital Pixel Test Structures (DPTS)**

APTS

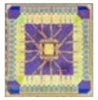


Seed **pixel signal response to ^{55}Fe** Vs irradiation levels, as measured on 15 μm pitch **Analog Pixel Test Structures (APTS)**

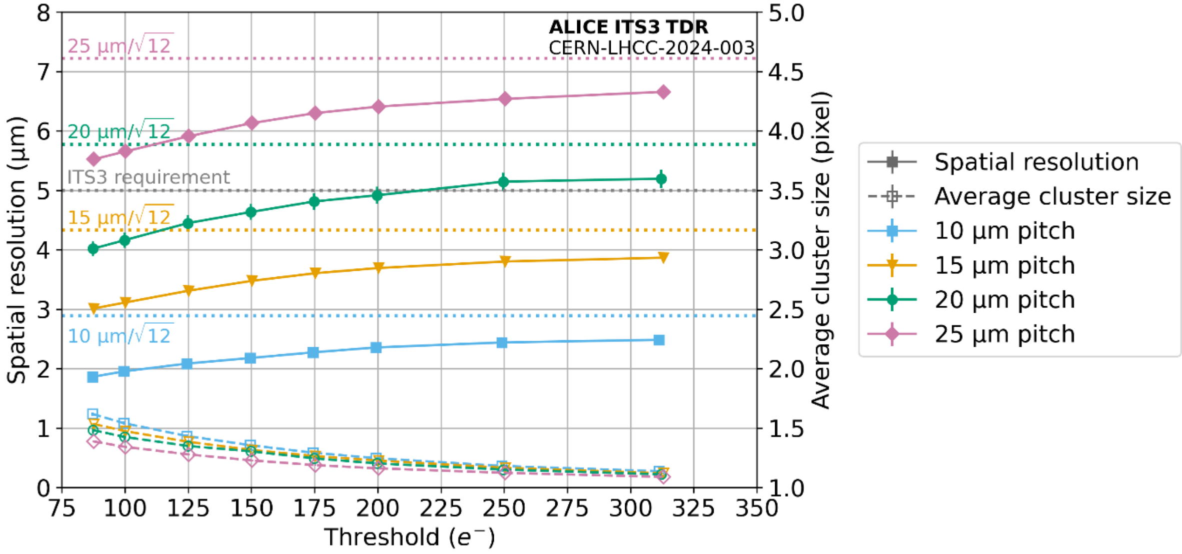
ITS3 sensor performance: spatial resolution

- ITS3 **spatial resolution requirement: 5 μm**
  - Test beam measurements on APTS with different pixel pitches
  - Requirement met for pitch ≤ 20 μm at standard operating settings
  - Projected resolution with (20.8 μm x 22.8 μm) **ITS3 target pixel pitch meets the requirement**

APTS



Spatial resolution Vs threshold and pixel pitch, as measured in testbeams on **APTS**

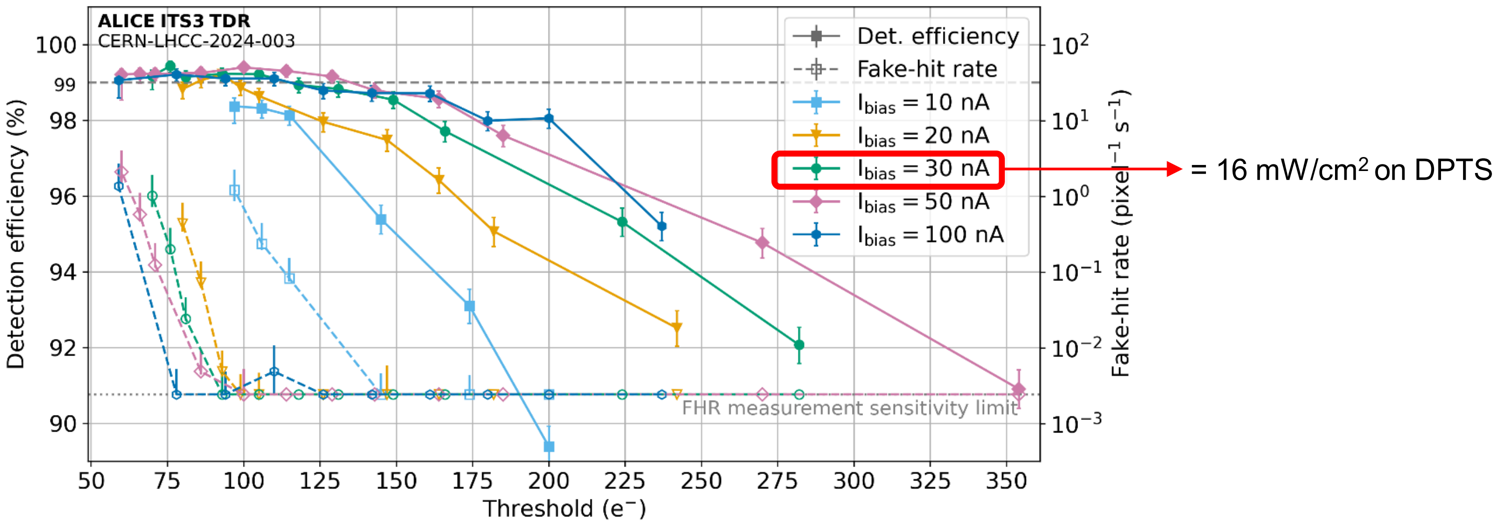


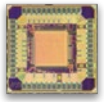
- Sensor **position stability** required to be within 2 μm

ITS3 sensor performance: power consumption

- ITS3 maximum **power density: 40 mW/cm²** in the pixel matrix
- In-pixel power consumption minimization studied on DPTS by optimizing front-end settings
  - 16 mW/cm² as measured on 15 μm pixel
  - 7.6 mW/cm² if projected to the final ITS3 sensor pixel pitch

  } to be measured on stitched sensor matrix

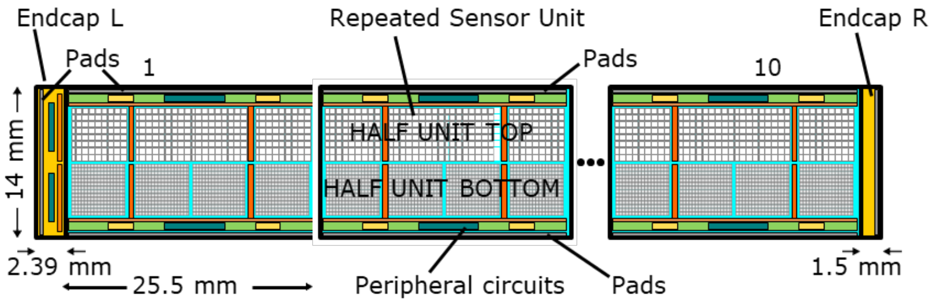


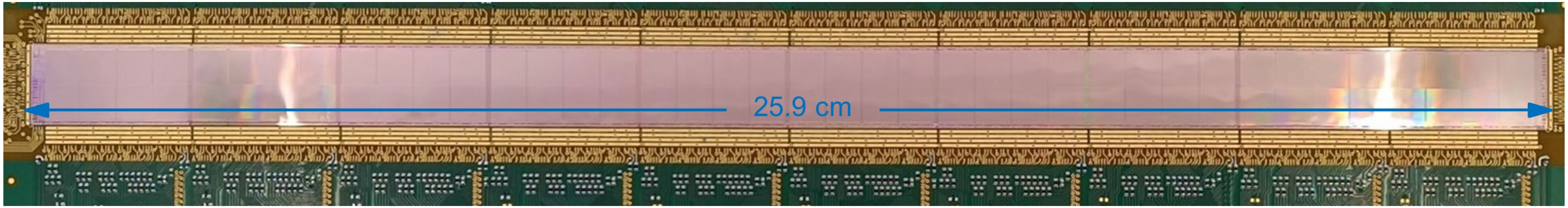


Detection efficiency and fake-hit rate Vs threshold and amplifier biasing current as measured on 15 μm pitch **DPTS**

ITS3 sensor performance: stitching

- **MOnolithic Stitched Sensor (MOSS):**
  - 10 Repeated Sensor Units (RSU) stitched together
  - **25.9 cm x 1.5 cm** – 18 μm and 22.5 μm pitch – 5 FE variants
  - **Stitched backbone** allows to control and read out from left edge
  - Each unit can be powered and tested separately
  - **Main yield issue understood**





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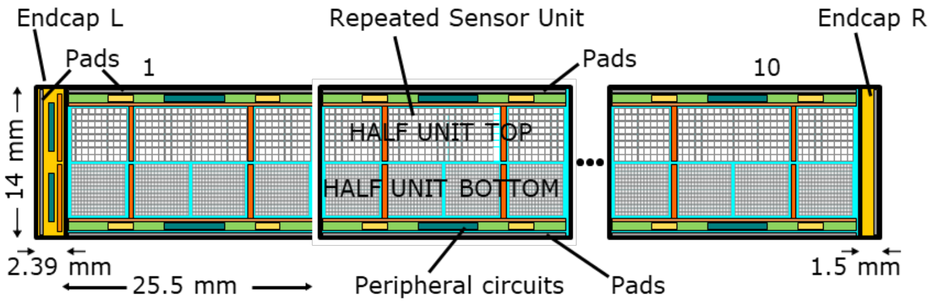
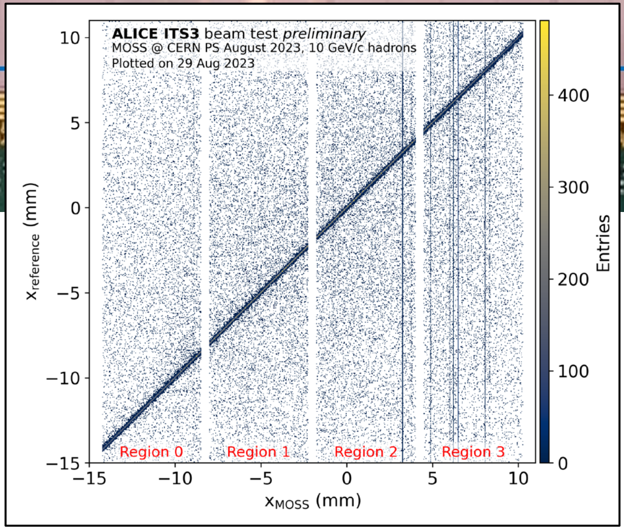
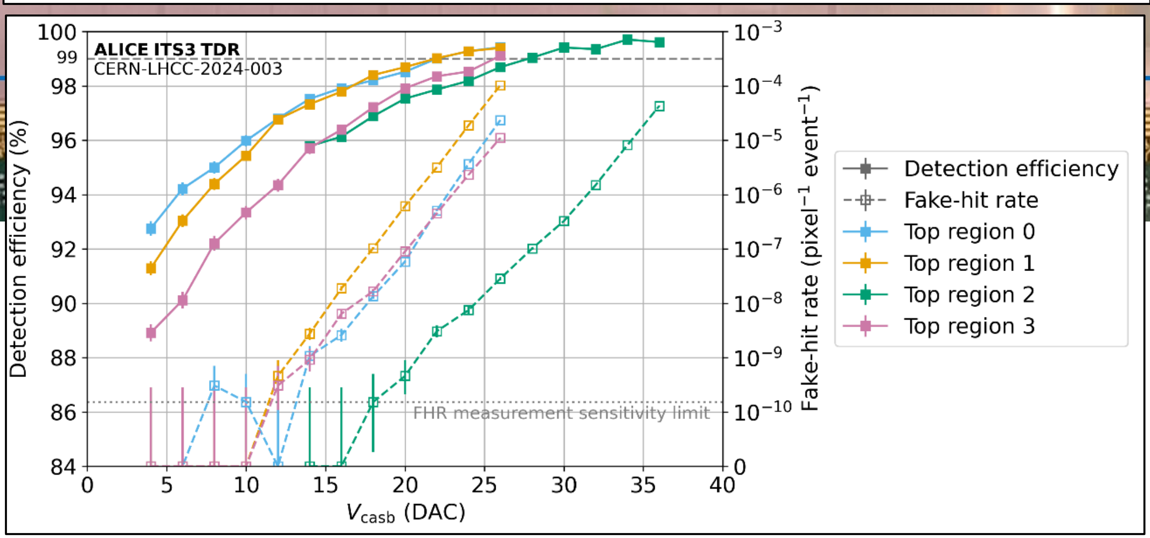


Chip operated in beam tests

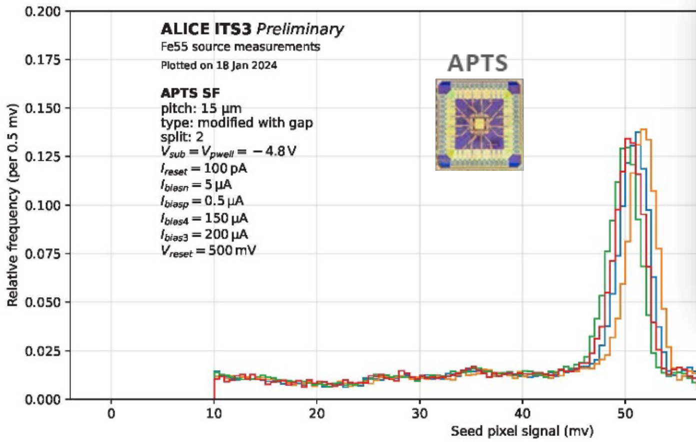
MLR1-level detection efficiency and fake-hit rate are confirmed

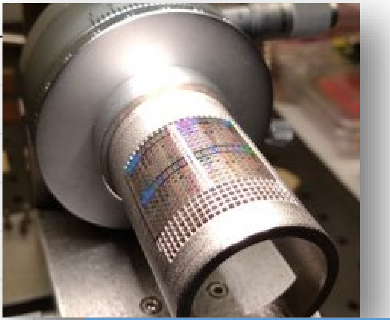




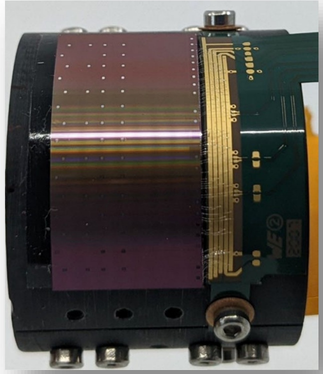
Bent MAPS: performance validation

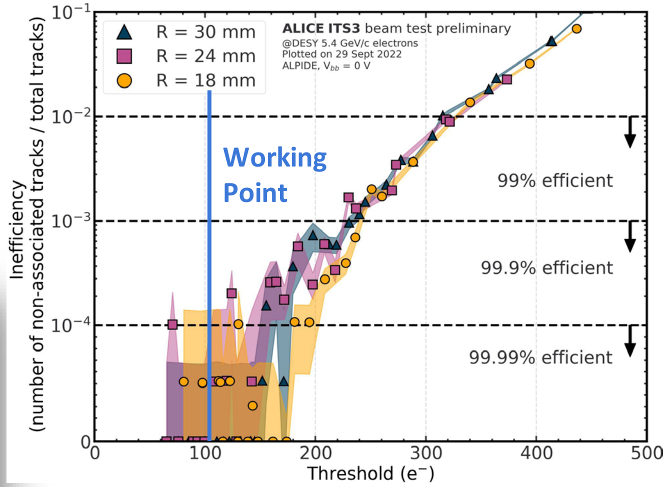
- MAPS performance in **curved geometry** has been validated
  - Efficiency preserved on bent ALPIDE (180 nm CMOS sensors)
  - Charge collection properties preserved on bent APTS (65 nm CMOS)





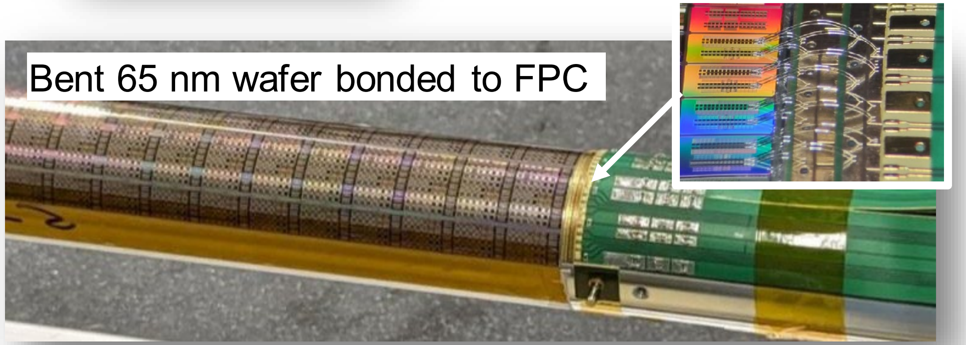
Seed pixel signal response to ^{55}Fe as measured by flat and bent **APTS**





Detection inefficiency Vs threshold for curved 180 nm CMOS sensors (**ALPIDE**), bent beyond the ITS3 radii

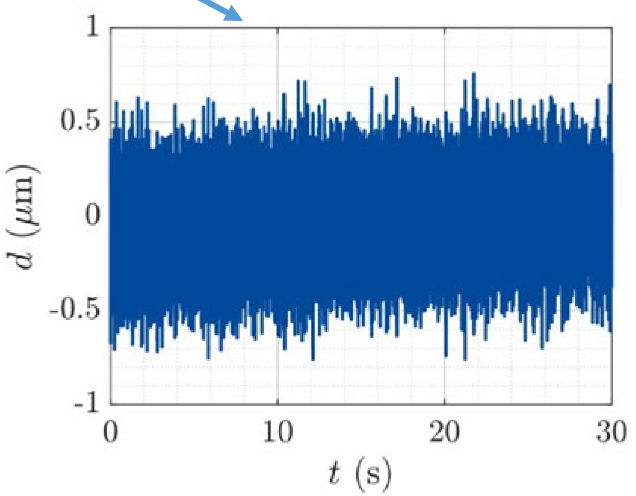
- **Large-area** sensor bending
  - Technique and procedure have been mastered
  - Tests on functional bent stitched sensors in preparation

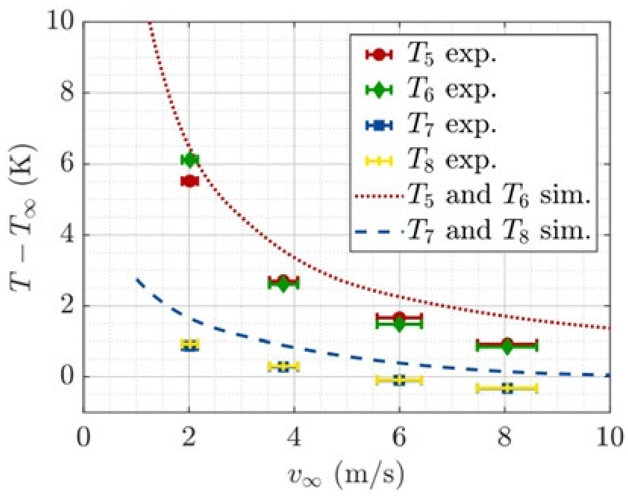


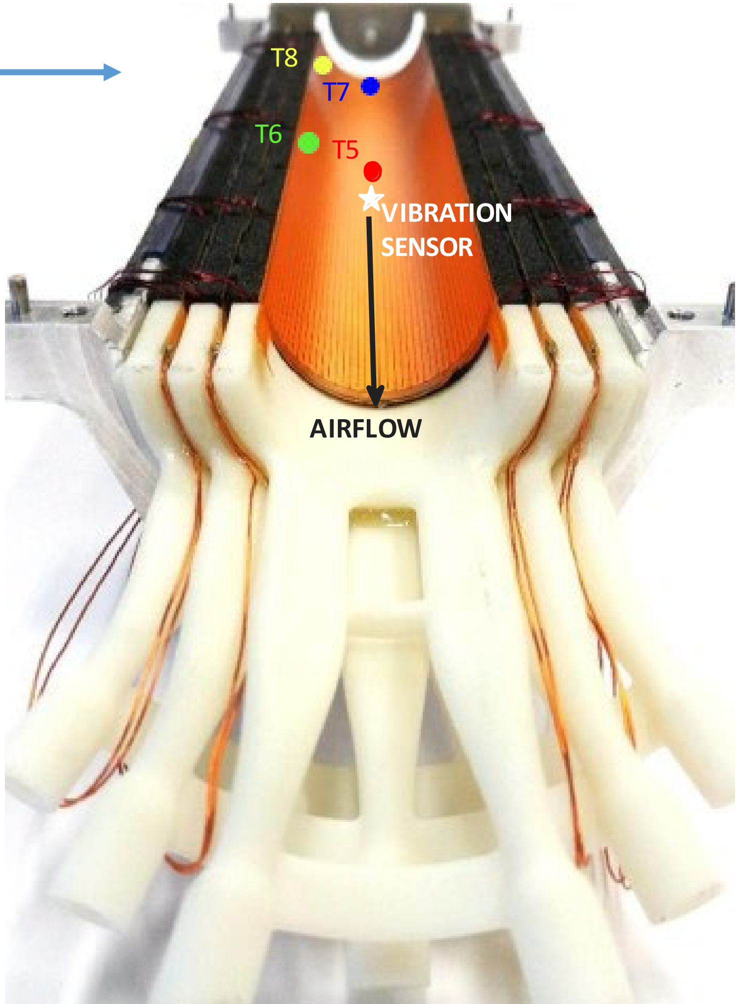
Bent 65 nm wafer bonded to FPC

ITS3 air cooling studies

- **Tests in wind tunnel** on breadboard model
  - Dummy silicon sensor with copper serpentine heater
  - Thermal load: 25 mW cm^{-2} in matrix, 1000 mW cm^{-2} in end-caps
- **Temperature difference** from inlet and within the sensor **< 5°C with 8 m/s airflow** between the layers
- Mechanical assembly with carbon foam half rings keeps **vibrations within ± 0.5 μm** with 8 m/s airflow

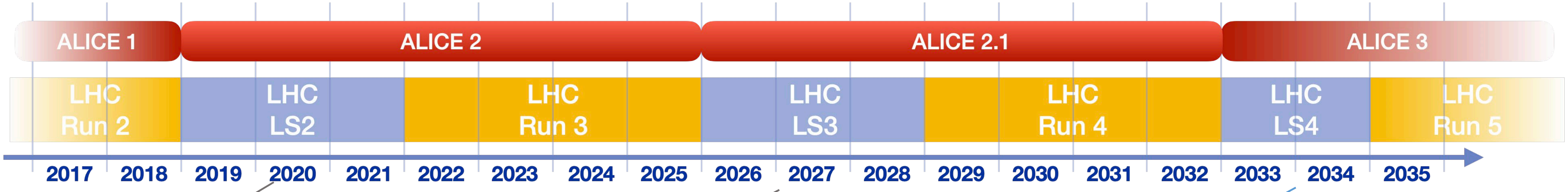




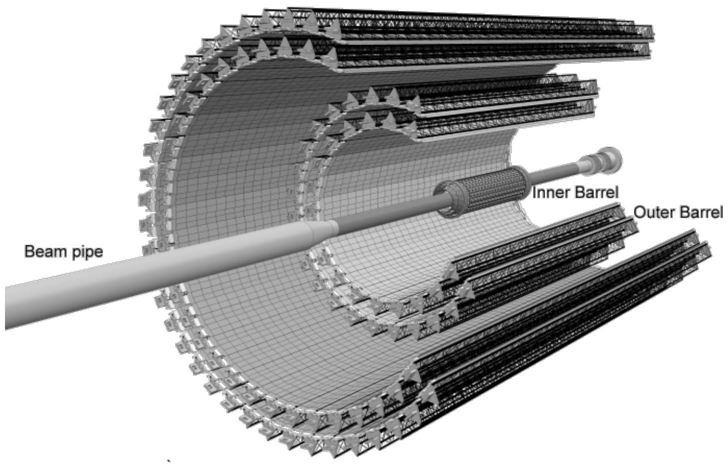


ITS3 Breadboard model

ALICE silicon tracker development path

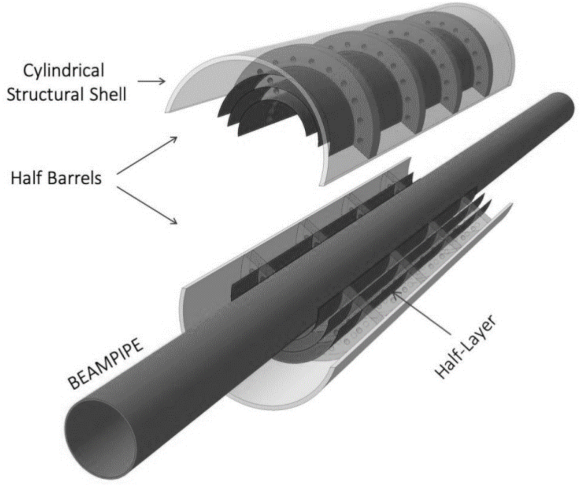


ITS2



ALICE Upgrades during LHC LS2

ITS3



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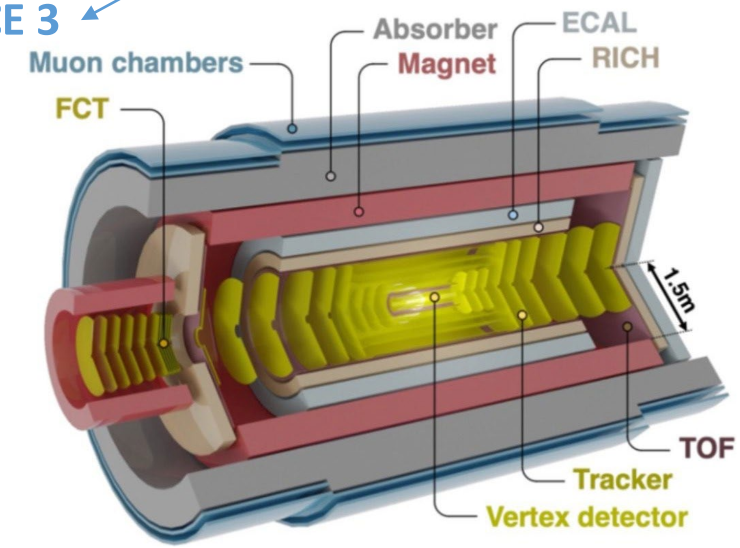
ALICE 3



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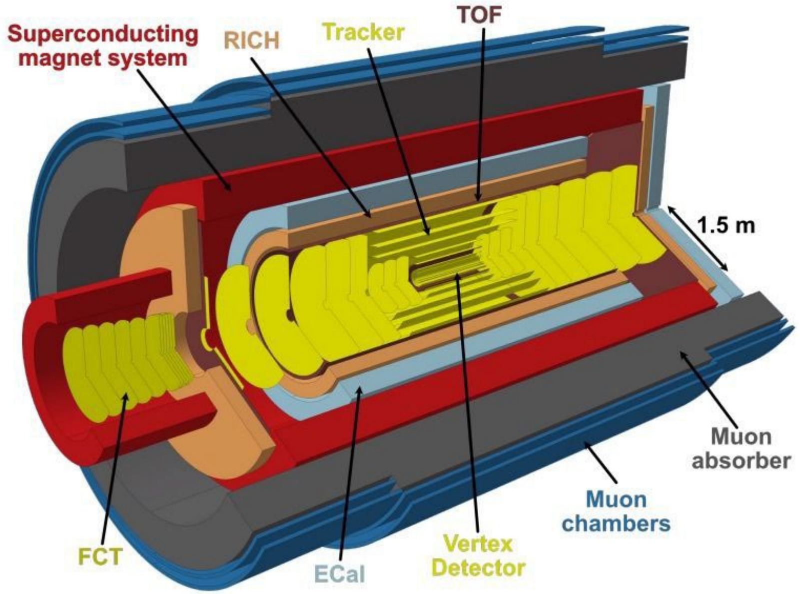
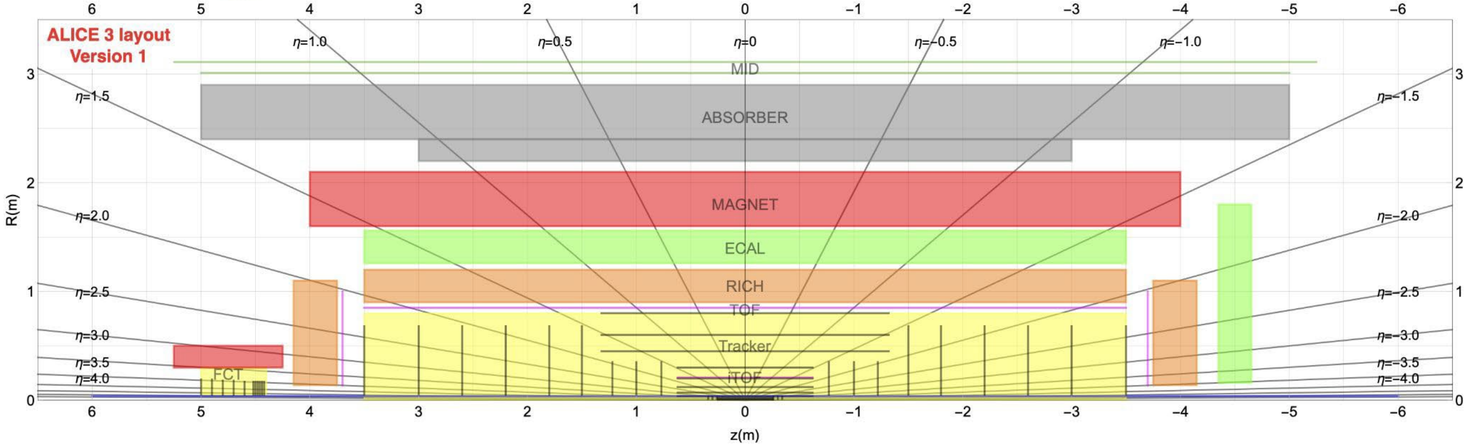


Next generation **compact experiment for LHC Run 5** and beyond

- **60 m^2** low-mass **all-silicon tracker** fully made of MAPS
- **Retractable vertex detector** for unprecedented pointing resolution
- **Large acceptance:** $-4 < \eta < 4$
- Excellent PID capabilities thanks to TOF and RICH detectors
- Superconducting magnet system
- Continuous readout and online data processing to access rare signals
- Target interaction rates x2 in Pb-Pb and x50 in pp (24 MHz) wrt Run 3 & 4

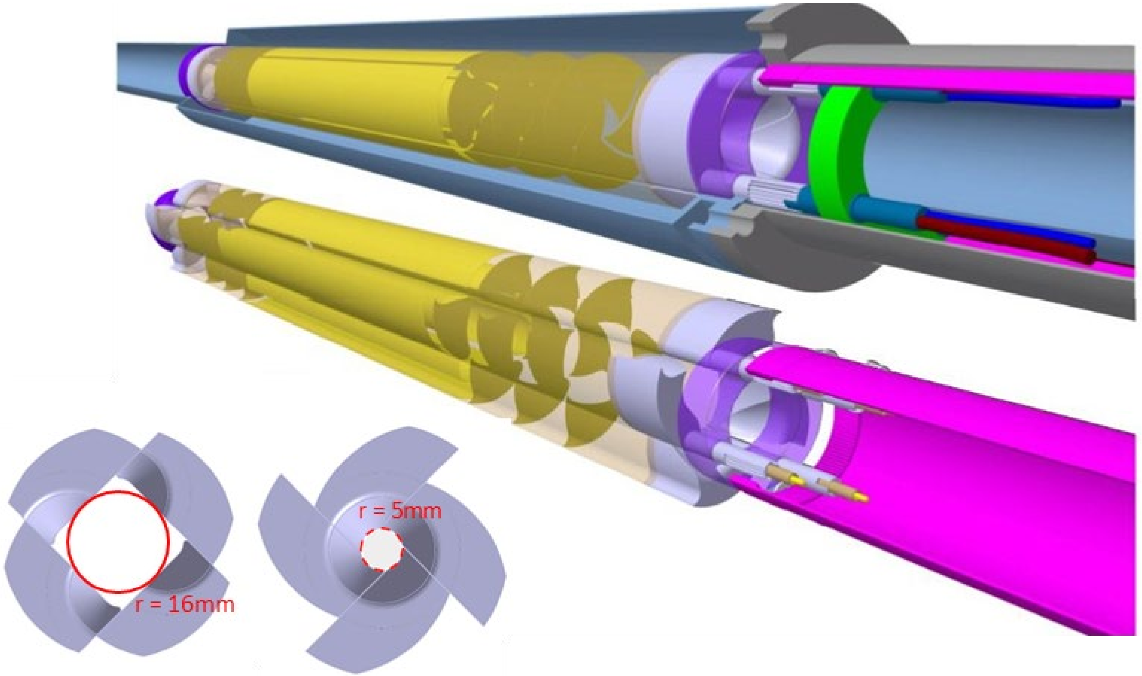


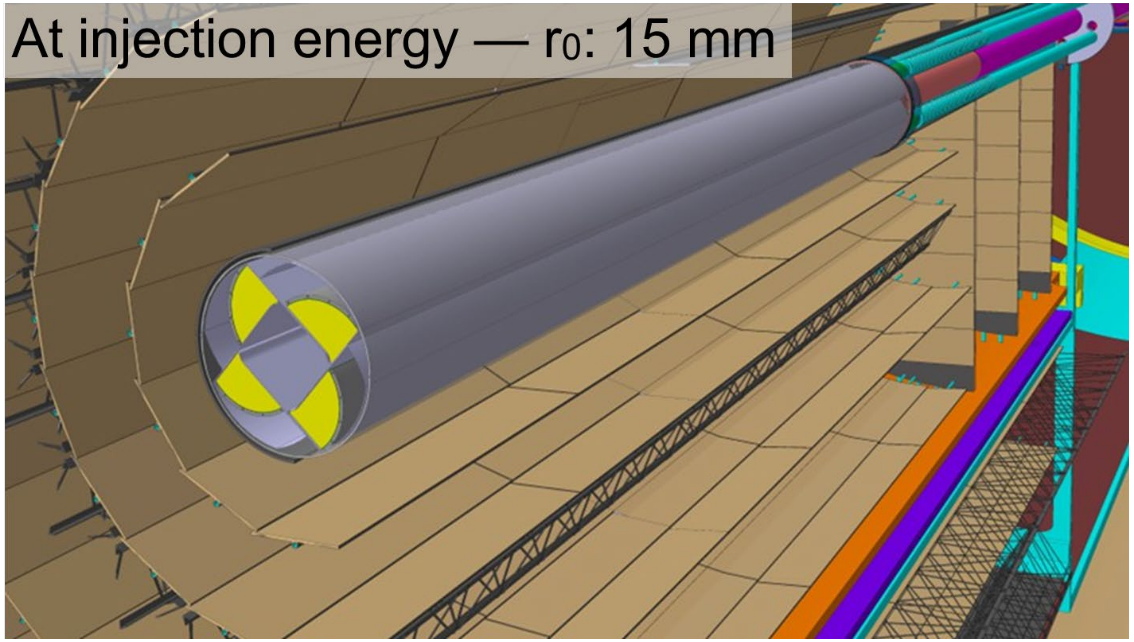
- **LOI** approved in 2022
- **Scoping Document** in preparation
- Specific **R&D starting up**

ALICE 3 Vertex Detector

3 barrel layers of ultra-thin, curved, wafer-scale MAPS

- Retractable structure inside the beam pipe secondary vacuum
- First detection layer at **5 mm from the interaction point**
- Completed by 2 x 3 end-cap disks for high |η| coverage





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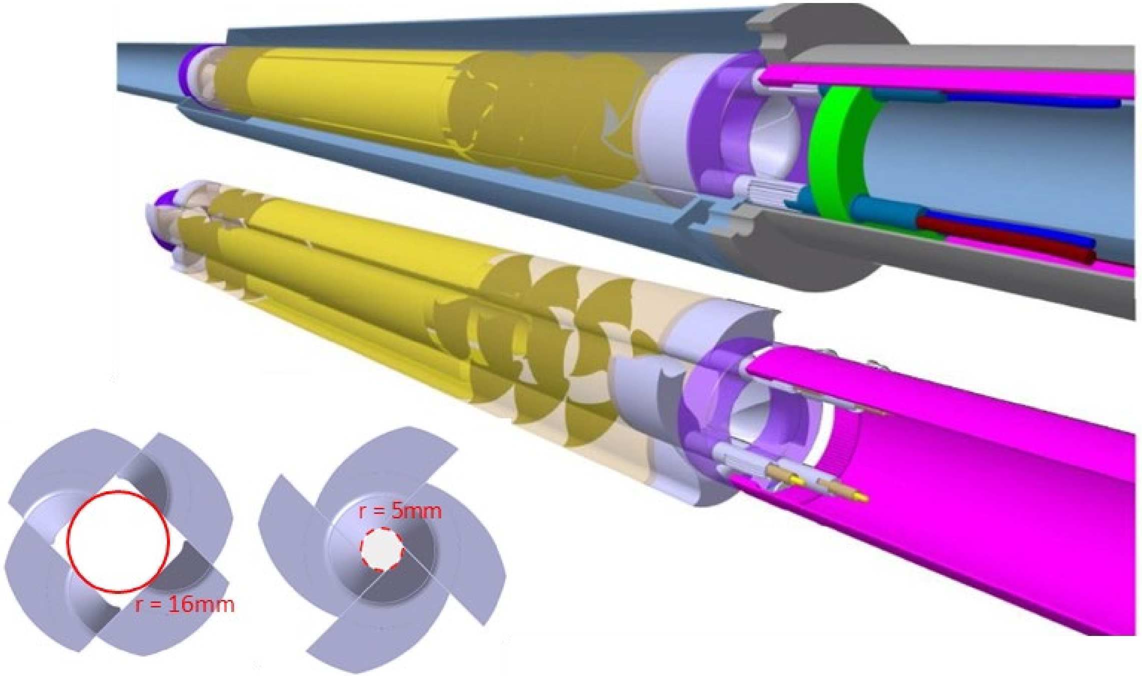

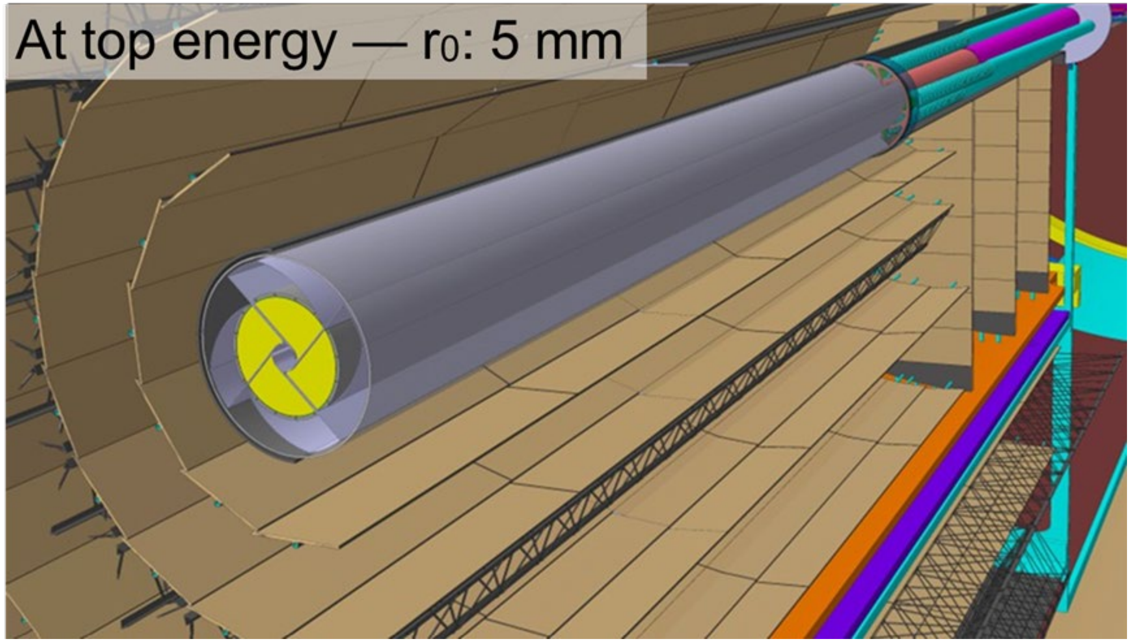

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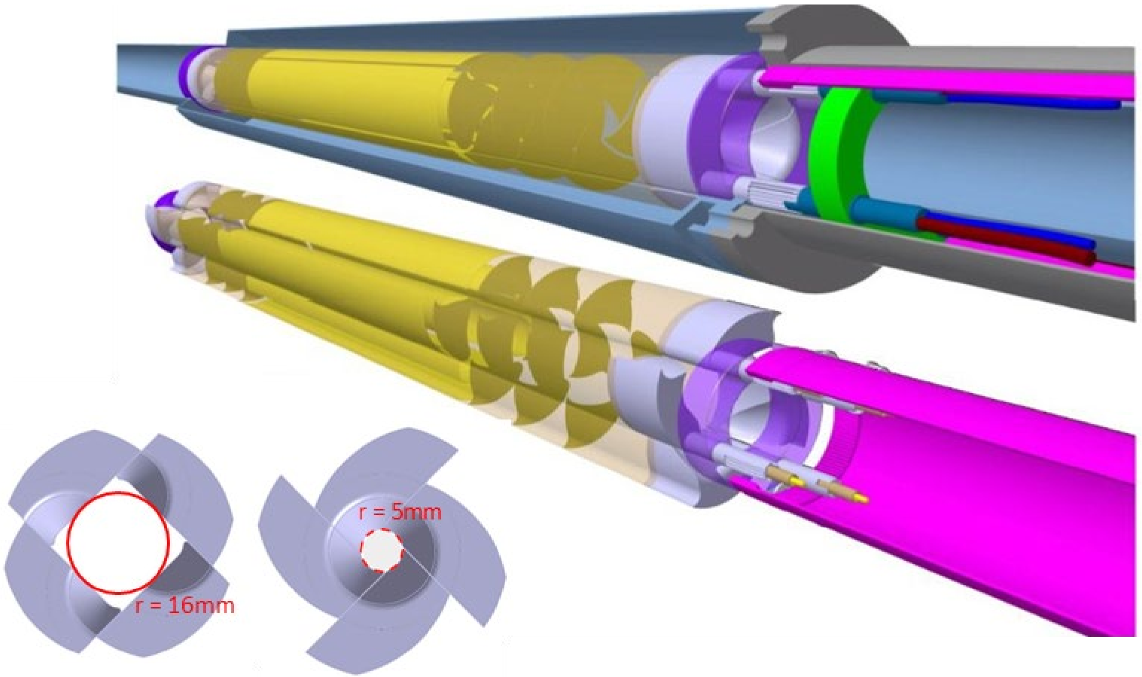


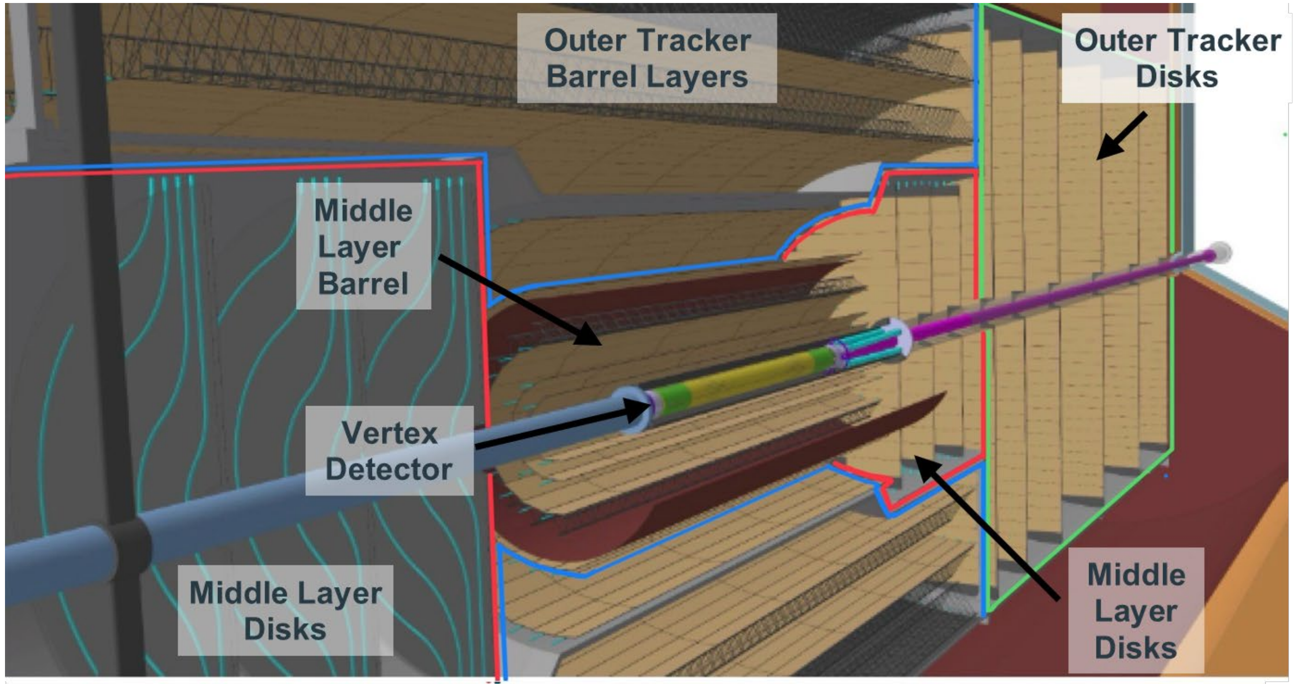
- Unprecedented **spatial resolution: 2.5 µm**
- Extremely low **material budget: 0.1%** X_0/layer
- **Hit rate: up to 94 MHz cm^{-2}**

- **Main R&D challenges:**
  - Radiation hardness
    - **10^{16} 1MeV n_{eq} cm^{-2} + 300 Mrad** *(LOI values)*
  - In-vacuum mechanics and cooling
  - **10 µm pixel pitch**
  - Data and power distribution

ALICE 3 Middle Layers and Outer Tracker

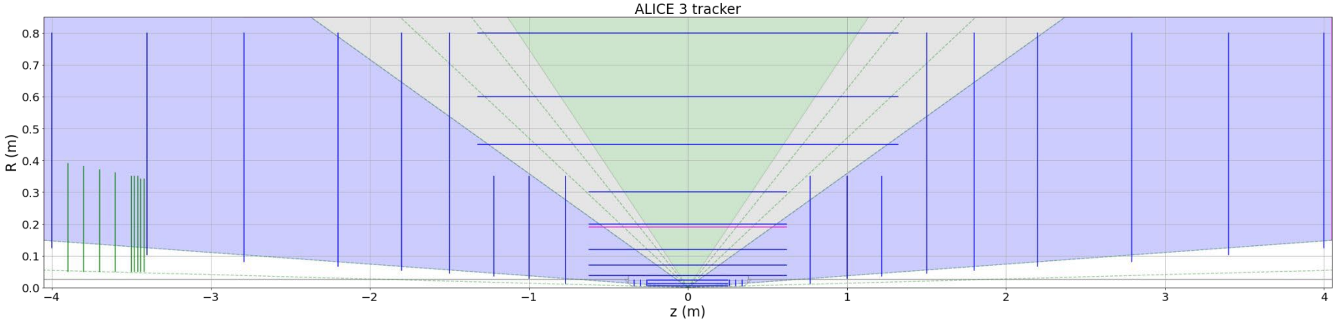
60 m^2 of silicon

  - 8 barrel layers (3.5 cm < radius < 80 cm)
  - 2 x 9 end-cap disks
- Material budget: 1% X_0/layer
- Position resolution: 10 μm (~ 50 μm pixel pitch)
- **Low power consumption < 20 mW/cm^2**
- **100 ns time resolution** to mitigate pile-up



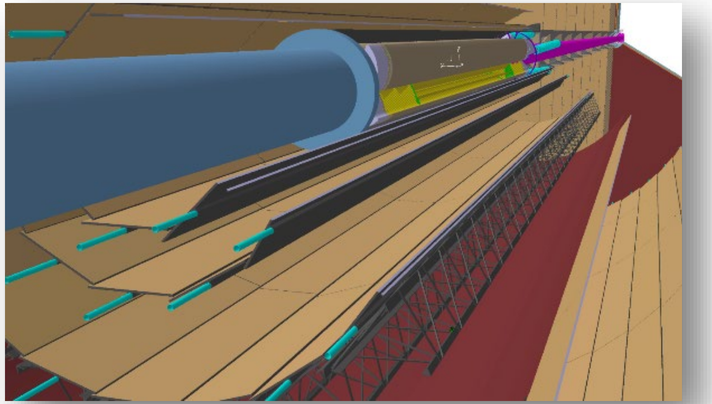
Main R&D challenges:

- Module design for **industrialized production**
- **Low power consumption** while preserving timing performance

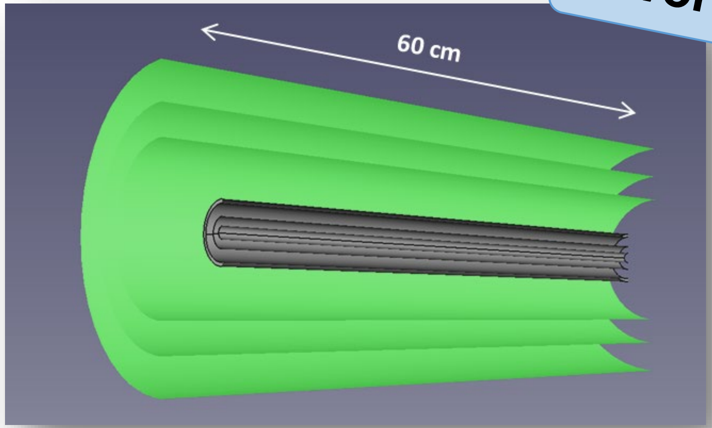


ALICE 3 Middle Layers and Outer Tracker

- Specific layouts being proposed for **Middle Layers**
  - 3-4 layers outside the beam pipe (r < 20 cm)
  - Material budget reduction from 1% to 0.1% beneficial for secondary particles and soft e^-



Standard staves/module layout (LOI)



ITS3-like bent large-area sensors

Work in progress

Blade/wheel barrels and disks

- Vertex Detector, Middle Layers and Outer Tracker need **specific sensor optimizations:**
  - Towards a common, versatile R&D path forking into two separate chips
  - Easier for other applications like FCC-ee to build on it

Conclusions and Outlook

- The **ALICE Upgrades** for LS3 and LS4 are targeting ambitious detector performance
- **ITS3:** ultra-thin, truly cylindrical, wafer-scale MAPS vertex detector upgrade for Run 4
  - Now approaching the construction phase
  - **Full-size stitched sensor** design being finalized
  - R&D on all aspects reached maturity – **TDR** approved by the CERN Research Board
- **ALICE 3**, future LHC heavy-ion collider experiment for Run 5 and beyond
  - Compact **all-silicon tracker** design, pioneering several R&D objectives:
    - Increased spatial resolution, radiation hardness and rate capabilities on In-vacuum retractable **Vertex Detector**
    - Large-scale integration of low power consumption sensors on the **Outer Tracker**
  - **LOI** published, Scoping Document in preparation
- ITS3 and ALICE 3 upgrades can serve as **stepping stones towards FCC-ee**

Thank you for your attention!

Backup

ALICE Upgrades' motivations and requirements

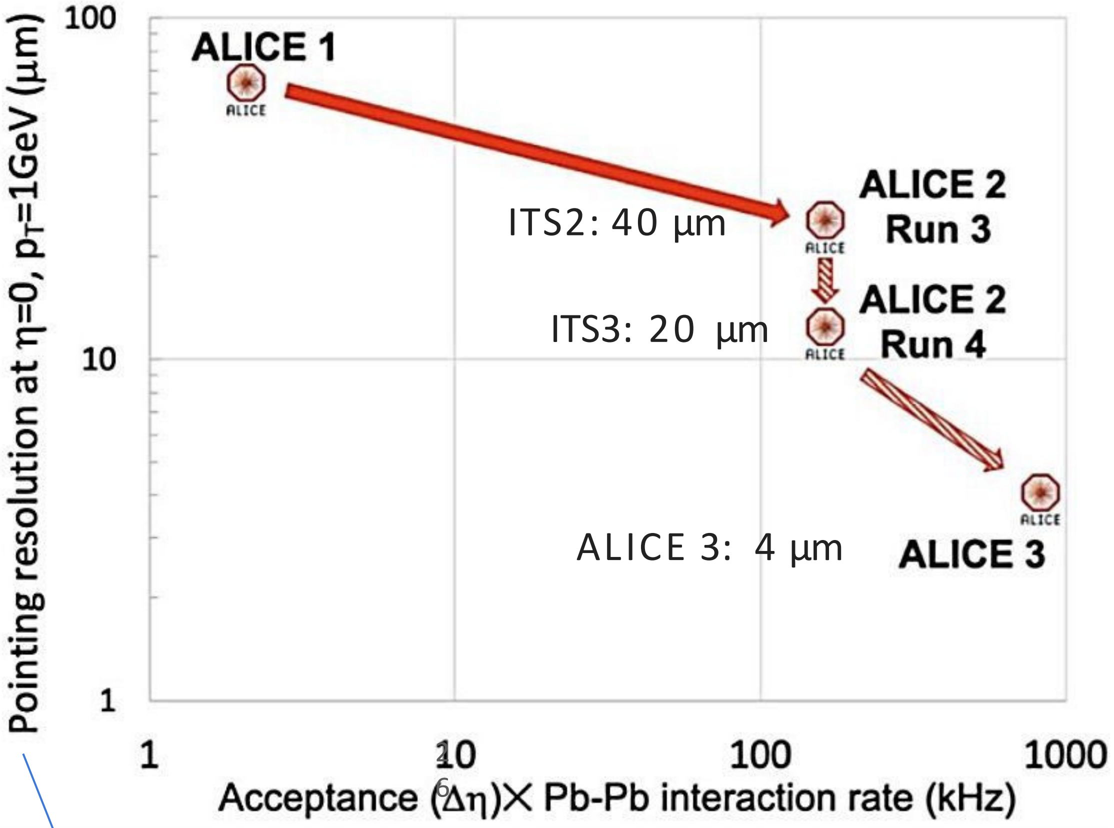
Physics Motivations:

Study of QGP in ultra-relativistic heavy-ions collisions → search for rare, low momentum probes, reconstruction of displaced decay topologies:

- Heavy flavour hadrons at low p_T
- Thermal dileptons
- Precision measurements of light (hyper)nuclei and searches for charmed hypernuclei

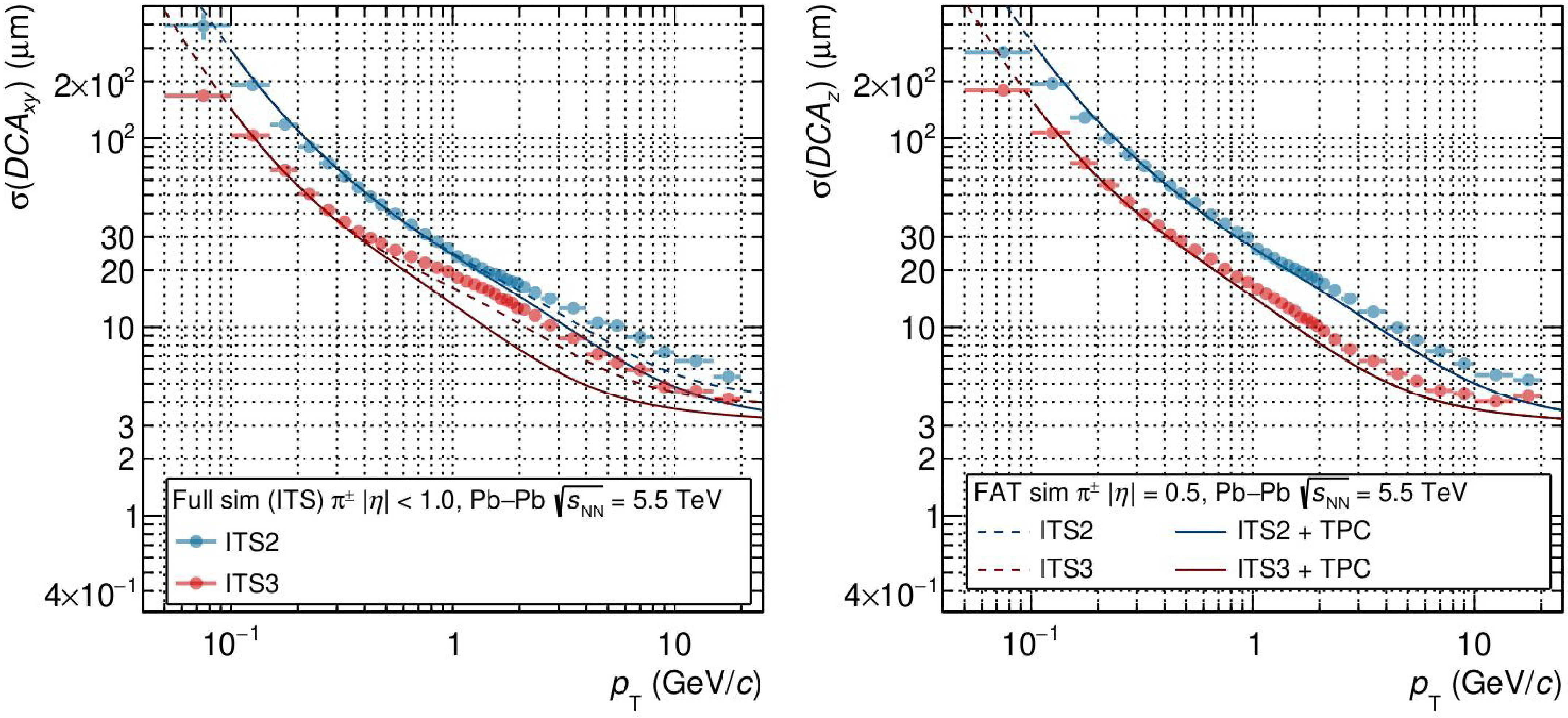
Tracker upgrade requirements:

- Increase of effective acceptance (acceptance x readout rate)
- Improve tracking and vertexing performance low p_T for combinatorial background suppression
→Excellent spatial resolution, minimal inner radius and low material budget are needed

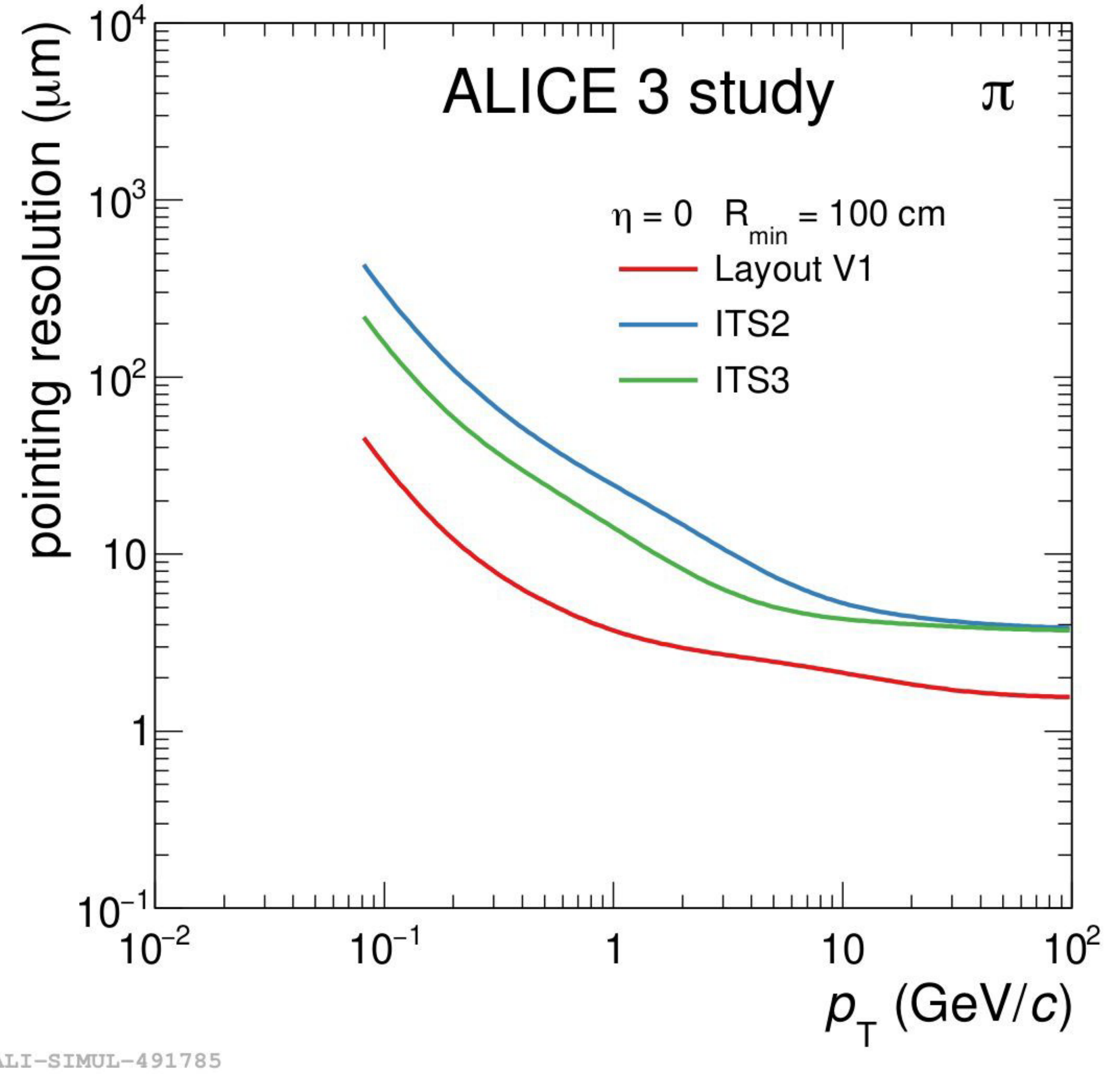


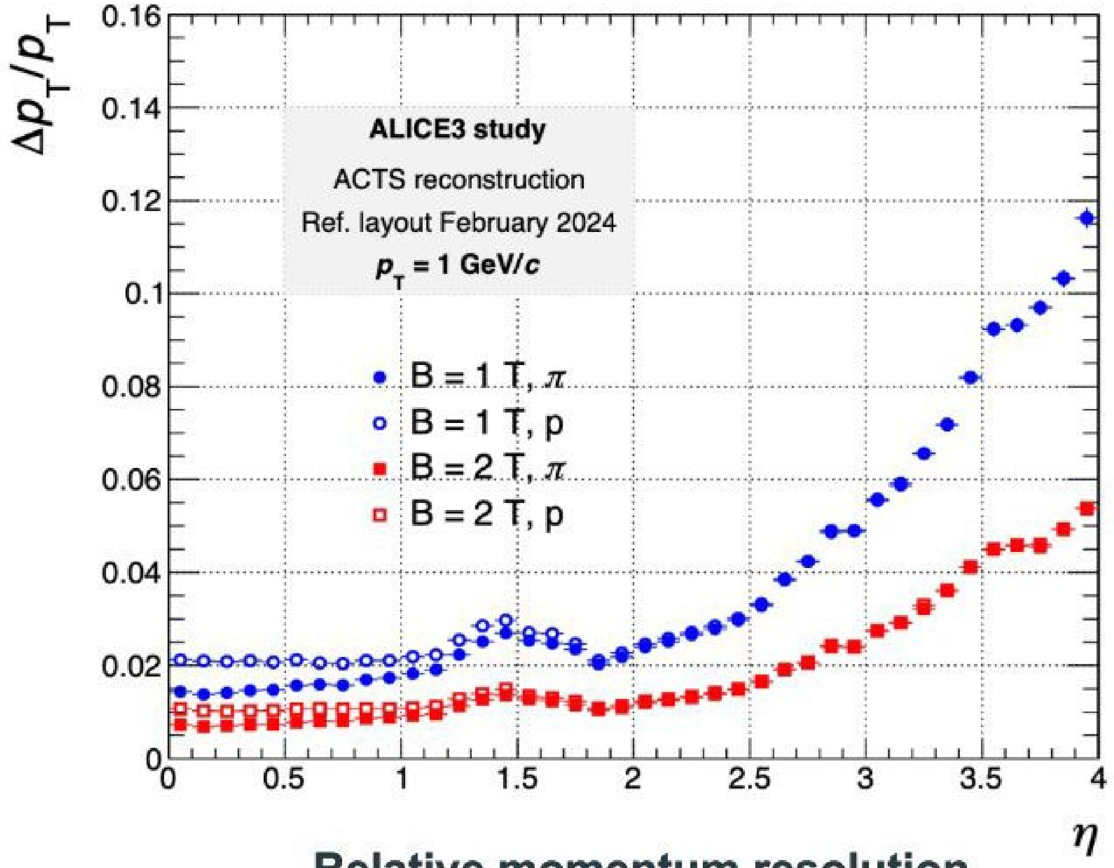
$$\sigma_{DCA} \approx A\,\sigma_{xyz} \oplus B\,\frac{r_0}{p}\sqrt{\frac{X}{X_0}}\cosh\eta$$

ITS3 pointing resolution



ALICE 3 tracking performance





Relative momentum resolution