Fast timing possibilities at FCC-ee

Matthew Gignac

June 11th 2024

SCIPP
SANTA CRUZ INSTITUTE FOR PARTICLE PHYSICS
UC SANTA CRUZ

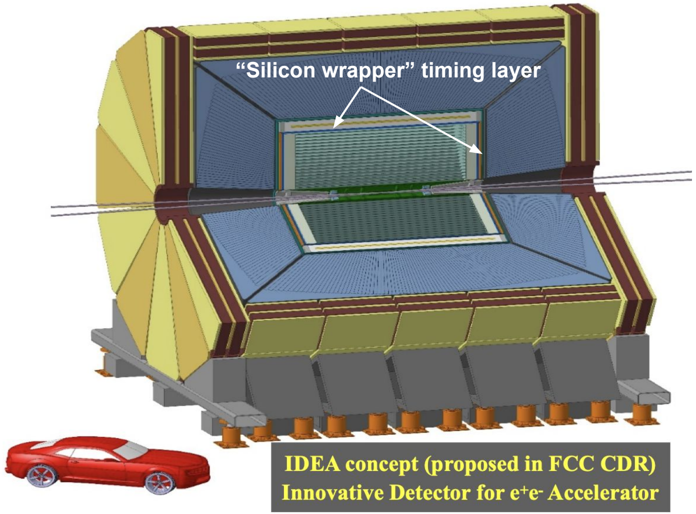
Introduction

UC SANTA CRUZ

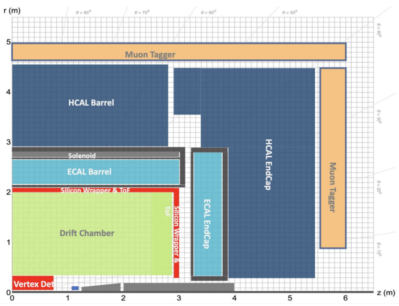
- Topics covered in today's talk:
    - Technologies for 4D tracking
    - LGAD technology
    - AC-LGADs @ EIC
    - Design optimization
    - Front-end readout
    - Monolithic CMOS options

FCC-ee Detector Designs

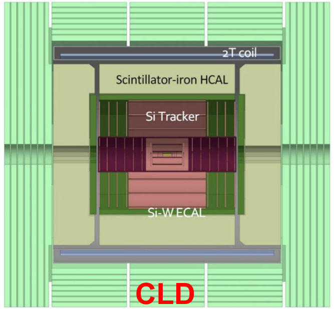
UC SANTA CRUZ



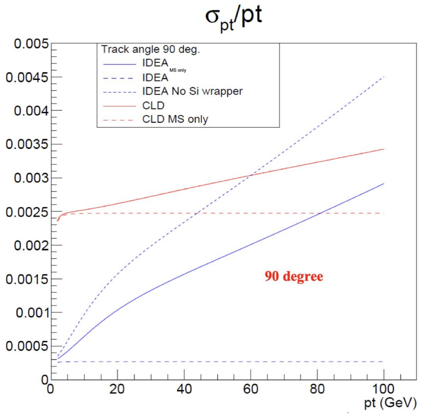
- **Precision silicon layer around the central tracker**
  - Improve momentum resolution
  - Extend tracking coverage in the forward/backward region by providing an additional point to particles with few measurements in the drift chamber
  - Provide a time of flight measurement for particle ID
- **Covered area ~90 m^2**
  - Important impact on services
  - Technology suitable for large size production
  - Do not want acceptance holes

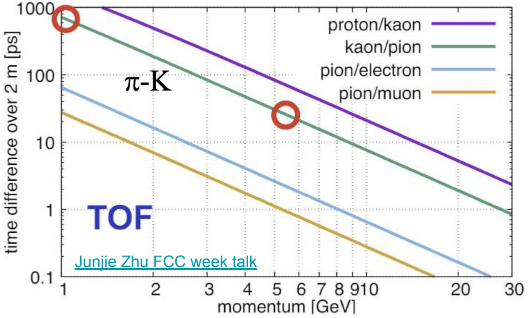


ALLEGRO



CLD



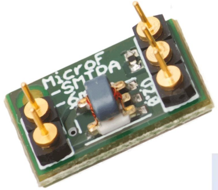


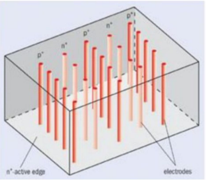
Technology for 4D tracking

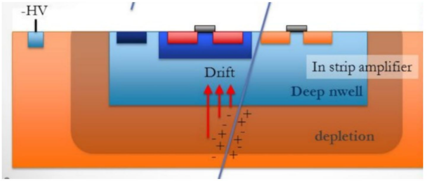
UC SANTA CRUZ

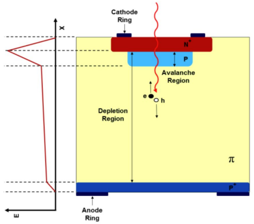
Which technology has sufficient time resolution for 4D tracking

- **SiPM (Silicon photomultiplier)**
  - But very little radiation hardness and low granularity
- **3D silicon sensors**
  - Perpendicular charge collection, ~20-30ps of time resolution, limitations due to dead areas and non-homogeneous field
- **Low Gain Avalanche Detectors (LGADs)**
  - Intrinsic gain, thin bulk, ~20-30ps of time resolution
  - Charge sharing allows spatial resolution <30 um
- **Monolithic CMOS detector**
  - Embedded amplification in the design, ~50-100 ps of time resolution
  - Extremely small pixels possible → excellent spatial resolution
- **In the future: LGAD CMOS? New materials (diamond)?**





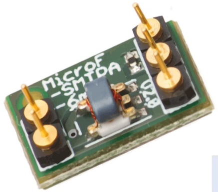


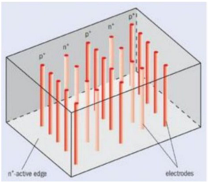


Technology for 4D tracking

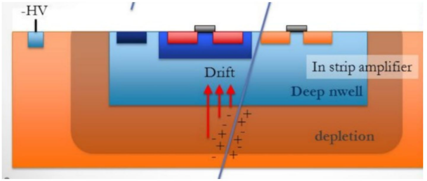
UC SANTA CRUZ

Which technology has sufficient time resolution for 4D tracking

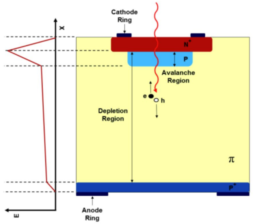




- **SiPM (Silicon photomultiplier)**
  - But very little radiation hardness and low granularity
- **3D silicon sensors**
  - Perpendicular charge collection, ~20-30ps of time resolution, limitations due to dead areas and non-homogeneous field
- **Low Gain Avalanche Detectors (LGADs)**
  - Intrinsic gain, thin bulk, ~20-30ps of time resolution
  - Charge sharing allows spatial resolution <30 um



- **Monolithic CMOS detector**
  - Embedded amplification in the design, ~50-100 ps of time resolution
  - Extremely small pixels possible → excellent spatial resolution
- **In the future: LGAD CMOS? New materials (diamond)?**



“Fast timing”

UC SANTA CRUZ

- An integrated detector with excellent temporal resolution requires **many ingredients:**
  - Sensor
  - ASIC
    - Technology, bandwidth
    - Power
  - Detector design
    - Cabling, module design, sensor biasing, noise rejection, etc …
  - Infrastructure
    - Clock distribution
    - Cooling
    - Data transfer

$$\sigma_t^2 = \sigma_{\text{ionization}}^2 + \sigma_{\text{jitter}}^2 + \sigma_{\text{TDC}}^2 + \sigma_{\text{clock}}^2$$

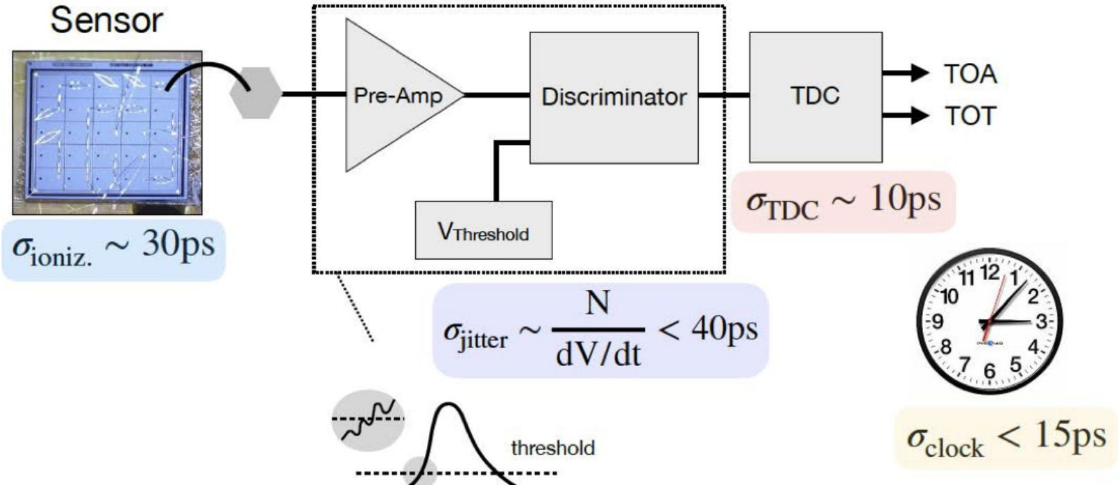


Image credit: Zhenyu Ye

“Fast timing”

UC SANTA CRUZ

Several sources of noise when considering a detector system with excellent temporal resolution:

- $\sigma_{\text{ionization}}$: variations in charge depositions → impacts amplitude and shape of the signal
- σ_{jitter}: minimized with low noise electronics and maximizing the slew rate (dV/dt) of the signal
- σ_{TDC}: the effect of TDC binning
- σ_{clock}: contributions from clock distribution

$$\sigma_t^2 = \sigma_{\text{ionization}}^2 + \sigma_{\text{jitter}}^2 + \sigma_{\text{TDC}}^2 + \sigma_{\text{clock}}^2$$

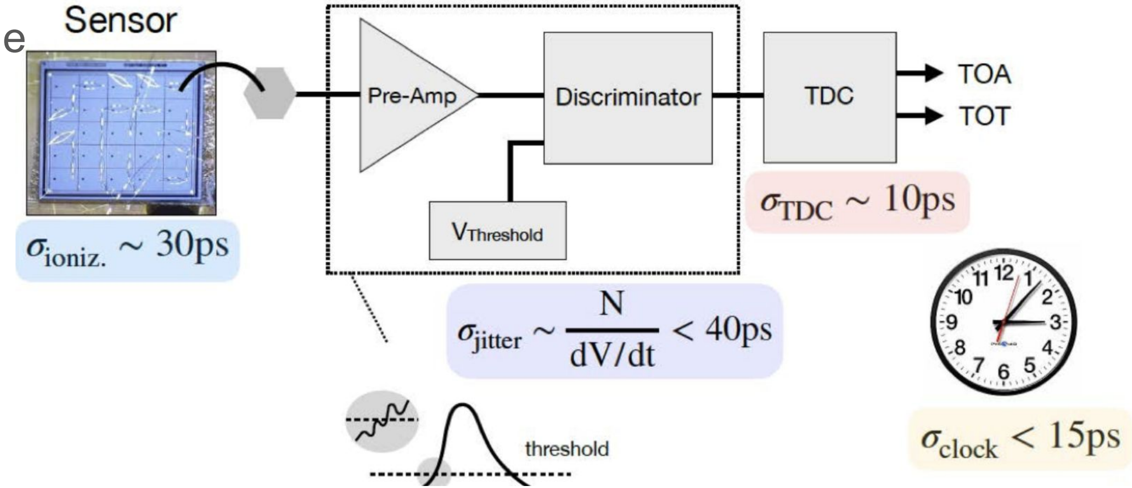
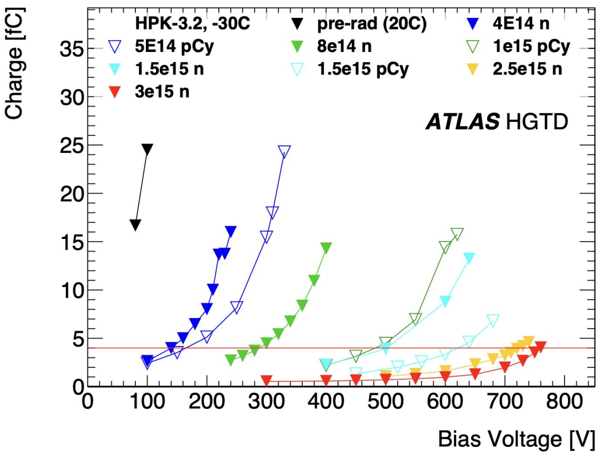


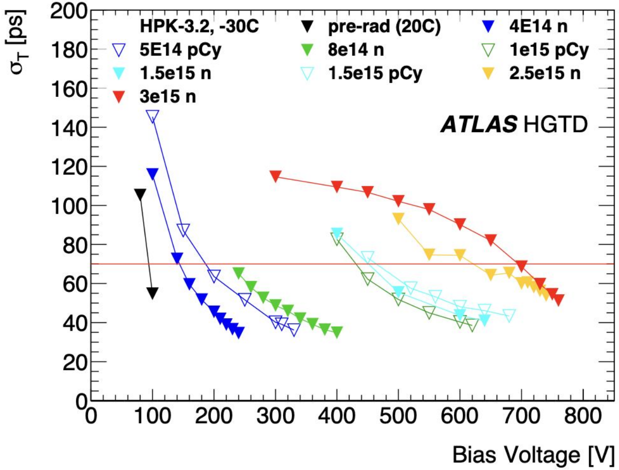
Image credit: Zhenyu Ye

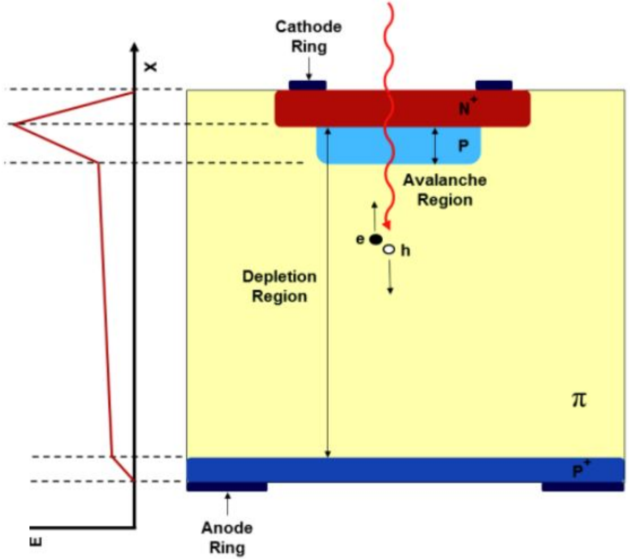
Low Gain Avalanche Detectors

UC SANTA CRUZ

- LGAD: silicon detector with a thin (<5um) and highly doped (~10^{16} P++) multiplication layer
- LGADs have intrinsic modest internal gain (10-50)
  - Not in avalanche mode → controlled & tunable gain with externally applied bias voltage
- Excellent timing resolution even for high fluences!



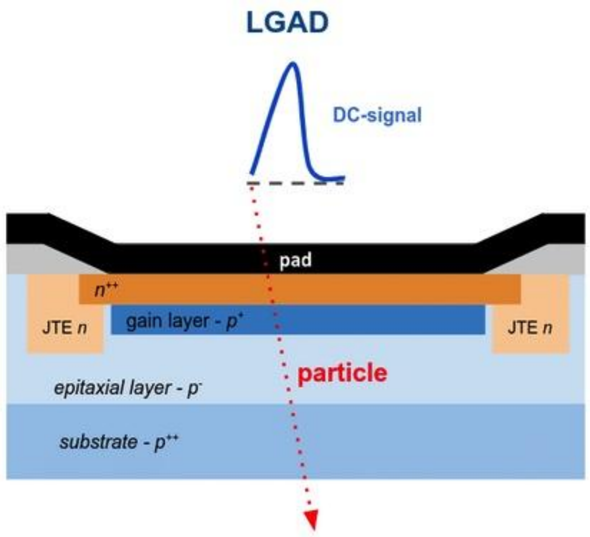




Traditional DC-LGADs

UC SANTA CRUZ

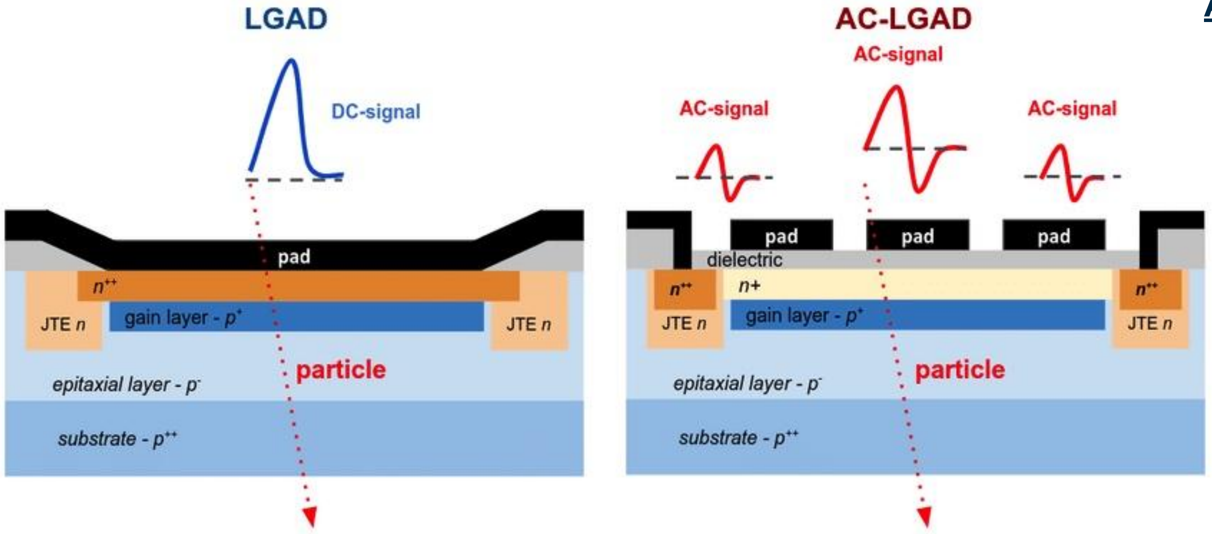
- LGADs have excellent timing resolution, but relatively poor spatial resolution
  - The JTE creates a gap between LGAD pads → 100% fill factors cannot be achieved
  - Position resolution is limited to be sqrt(1/12) of the pad size
- For FCC-ee, **desire position resolution down to O(10) um level and 100% fill factor**
  - **Unachievable with traditional DC-LGAD detectors technology**



AC-LGAD: Improving spatial resolution

UC SANTA CRUZ

- LGADs have excellent timing resolution, but relatively poor spatial resolution
  - The JTE creates a gap between LGAD pads → 100% fill factors cannot be achieved
  - Position resolution is limited to be sqrt(1/12) of the pad size
- For FCC-ee, **desire position resolution down to O(10) um level and 100% fill factor**
  - **Unachievable with traditional DC-LGAD detectors technology**

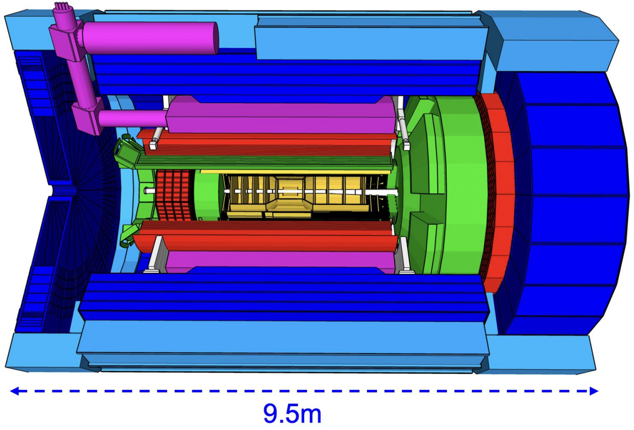


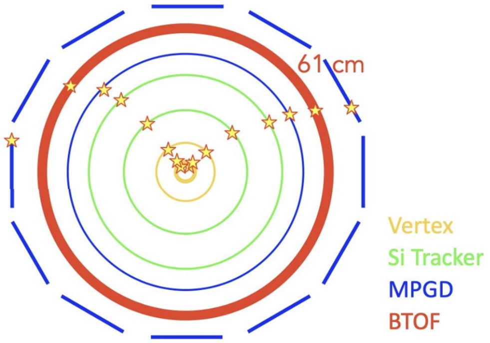
AC-LGAD technology:

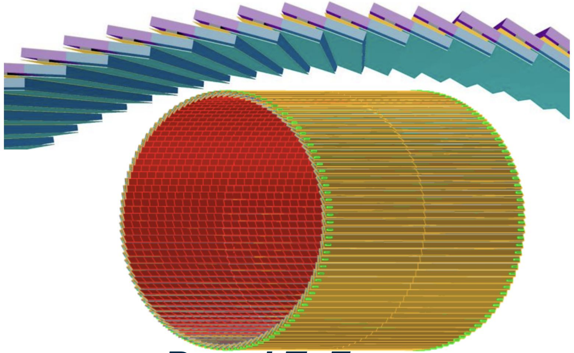
- Replace the segmented n++ layer with a continuous n+ layer
- Electrical signals in the n+ layer are AC coupled to the readout pads/strips, which are separated with a thin dielectric material.
- Charge sharing between strips/pads **significantly improvements spatial resolution and maintains temporal resolution!**

EIC Silicon Time of Flight Detector

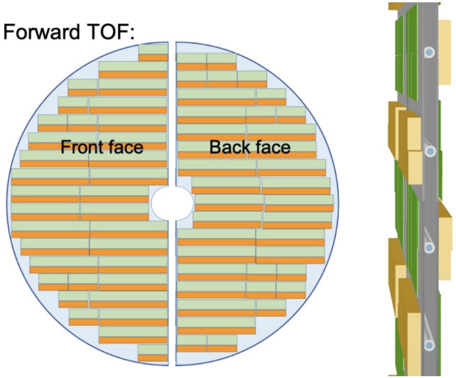
- **Electron Ion Collider will include an AC-LGAD time of flight layer: used in tracking and PID**
- Single AC-LGAD layer: **Barrel (strips) and end-cap (pads) with total area of ~13m^2**
- Much of the design & challenges being faced for this project directly transferable! **But, FCC-ee will be almost an order of magnitude larger…!**
- Timing and spatial requirements similar to those that would be needed for FCC-ee







Barrel ToF

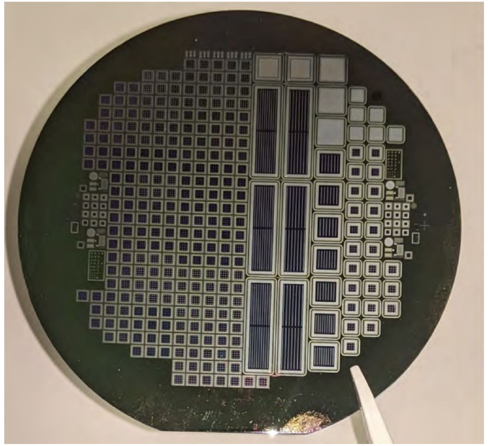


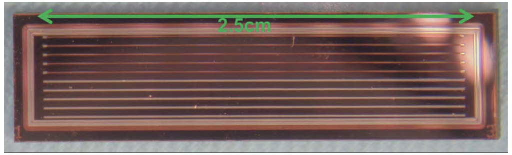
Forward ToF

Sensor design optimization

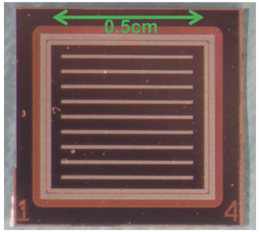
UC SANTA CRUZ

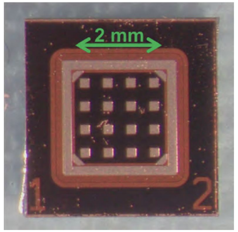
- Strict timing and spatial requirements for all time of flight detectors for ePIC
- Several years of sensor optimization:
  - **BNL:** quick turnaround time, very useful for R&D
  - **HPK:** commercial vendor for large scale production
- **Investigating properties:**
  - **n+ layer : very important for charge sharing**
  - **Strip length/pitch: minimize channel count → reduces power consumption**
  - **Sensor thickness: aim to improve timing resolution**





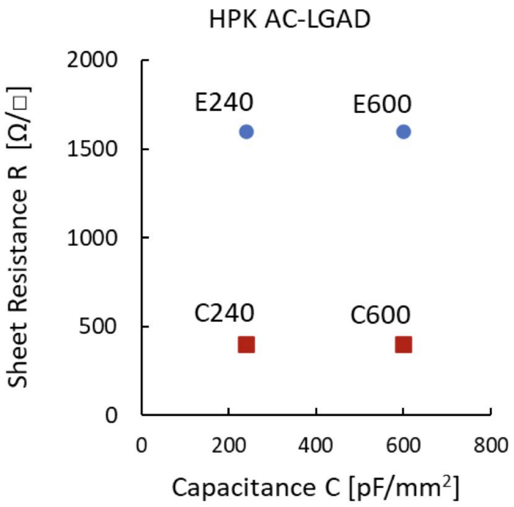
	Area (m^2)	Time resolution	Spatial resolution	Material budget
Barrel Time-of-Flight	10	35 ps	30 μm in $r \cdot \phi$	0.01 X_0
Forward Time-of-Flight	2.2	25 ps	30 μm in x and y	0.05 X_0
B0 Tracker	0.07	30 ps	20 μm in x and y	0.01 X_0
Roman Pots	0.14	30 ps	140 μm in x and y	no strict req.
Off-Momentum Detectors	0.08	30 ps	140 μm in x and y	no strict req.

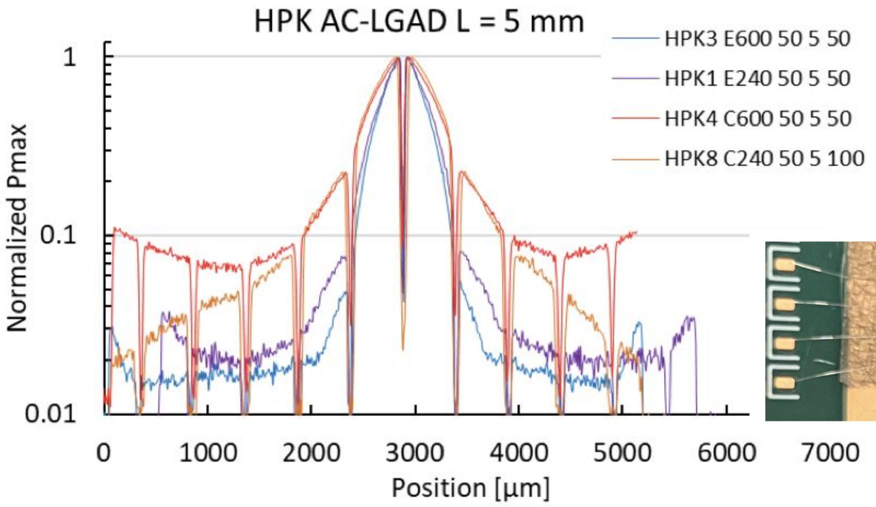




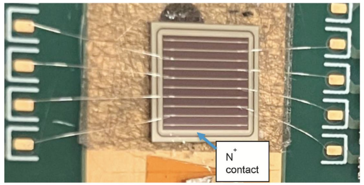
Charge sharing in AC-LGADs

- Charge sharing between neighboring strips is essential for good position resolution
  - However large sharing beyond the next neighbor generates background signals which in general are detrimental to the sensor goal of low occupancy





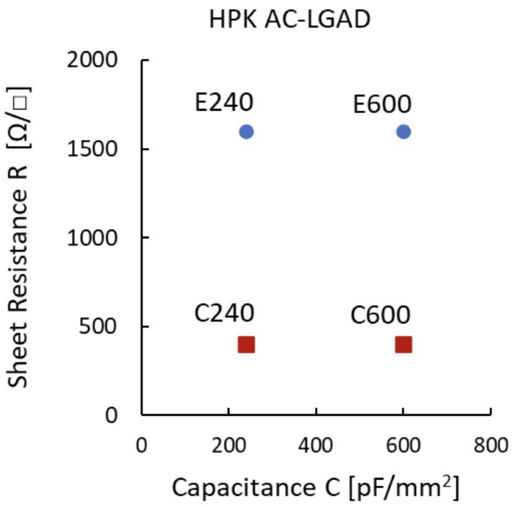
Link

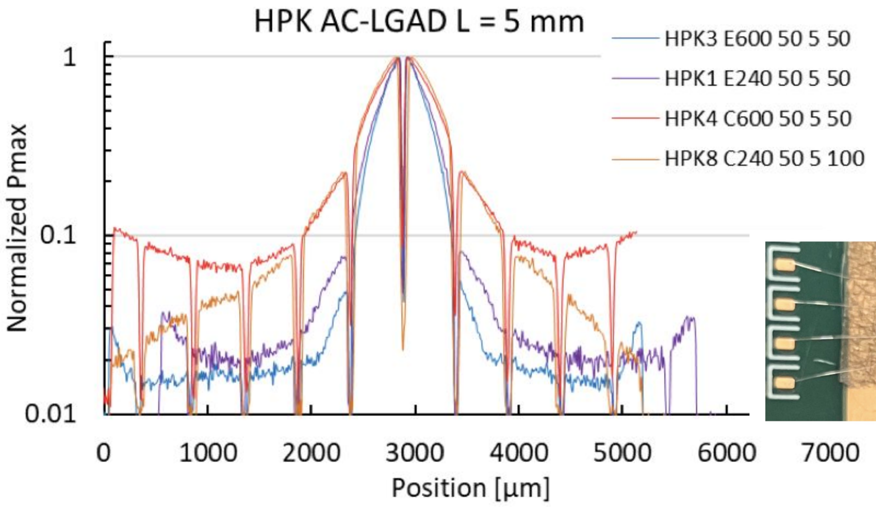


Charge sharing in AC-LGADs

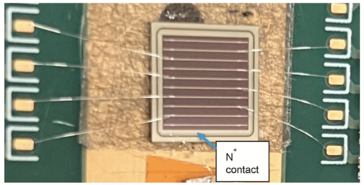
UC SANTA CRUZ

- Charge sharing between neighboring strips is essential for good position resolution
  - However large sharing beyond the next neighbor generates background signals which in general are detrimental to the sensor goal of low occupancy





Link

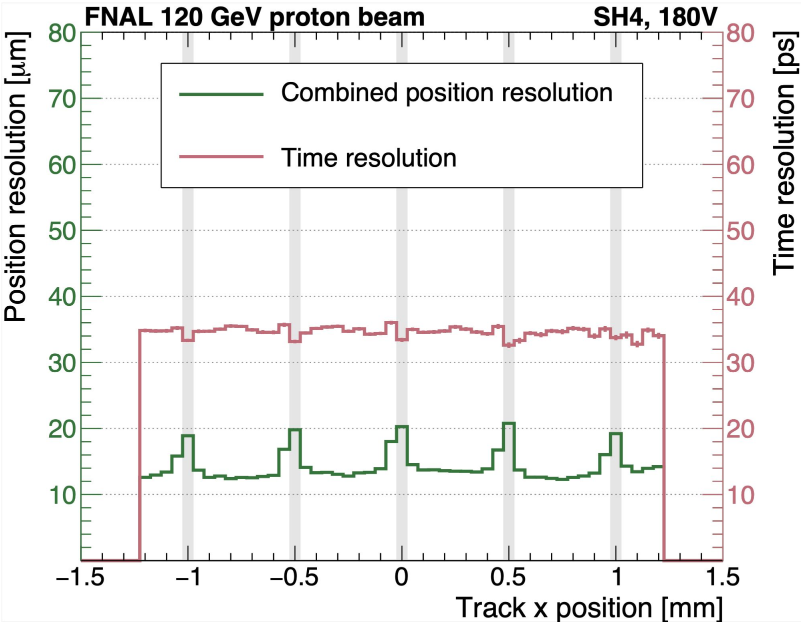


→ Sensors with large sheet resistance give best performance with next neighbour charge sharing at the 10-15% level

Timing & position resolution

UC SANTA CRUZ

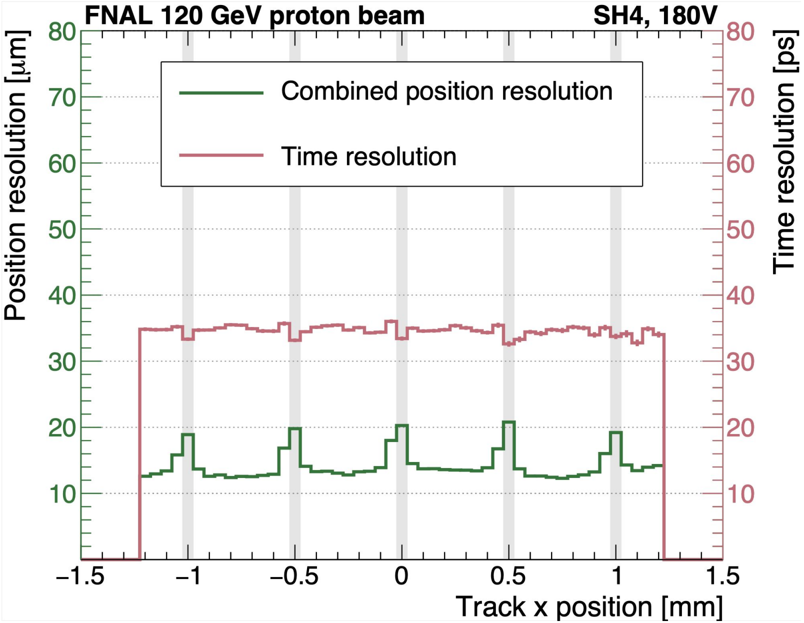
- Sensors with different configurations tested with 120 GeV protons @ FNAL

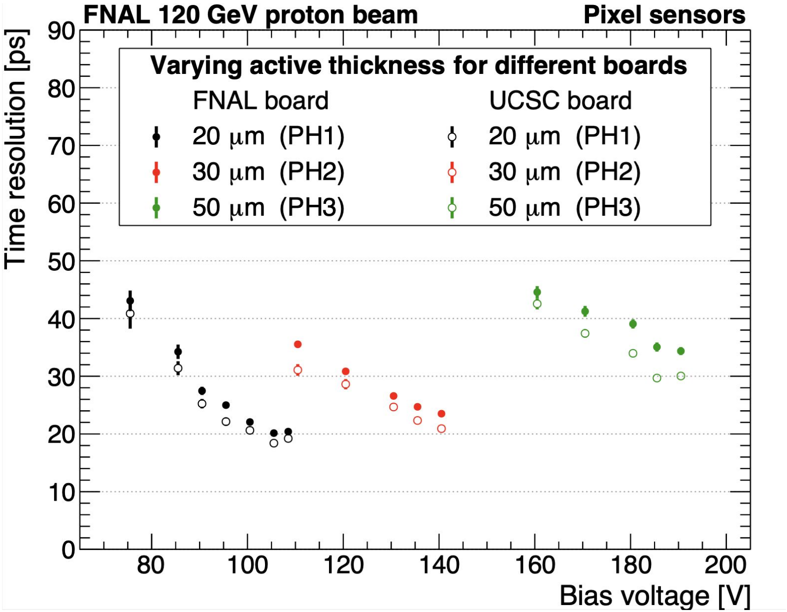


HPK <u>strip sensors</u> with 500 μm pitch:
→ Simultaneously achieving ~15 um position and ~35 ps timing resolution achieved in one sensor!

Timing & position resolution

- Sensors with different configurations tested with 120 GeV protons @ FNAL





HPK strip sensors with 500 μm pitch:
→ Simultaneously achieving ~15 um position and ~35 ps timing resolution achieved in one sensor!

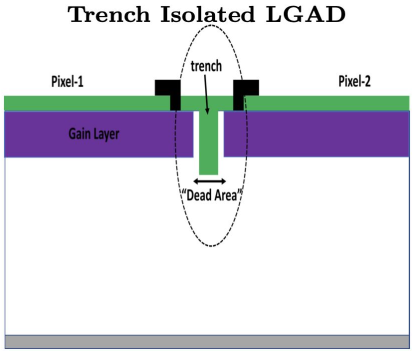
HPK pixel sensors with different thickness:
→ Thinner sensors capable of achieving time resolution down to 20 ps!

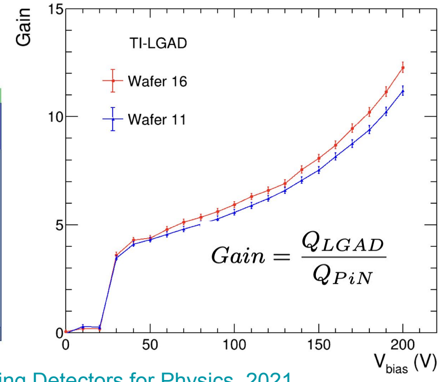
Other high granularity LGADs

UC SANTA CRUZ

Trench insulated LGADs (TI-LGADs)

- Replace JTE and p-stop of LGADS with a narrow (<1um) & shallow trench of SiO_2
  - Trenches act as a drift/diffusion barrier
  - Dead regions significantly reduced!
- Several advantages over traditional LGADs: smaller gain-loss region, great timing resolution & improved spatial resolution

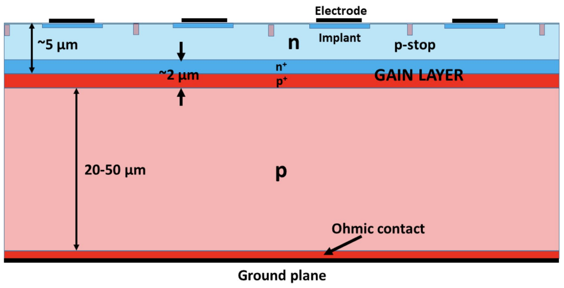


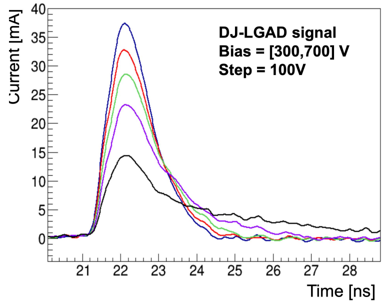


Ashish Bisht, Picosecond Timing Detectors for Physics, 2021

Deep-Junction LGAD (DJ-LGAD)

- Gain layer is buried, so the top can be segmented as in normal silicon detectors
- First production completed by Cactus material in collaboration with BNL and UCSC
- Promising performance (gain of ~5) and good pad insulation (few um IP gap)
- Similar granularity as regular silicon sensors



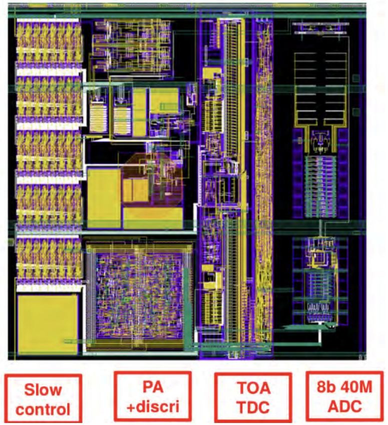


Y. Zhao et al 2022 J. Phys.: Conf. Ser. 2374 012171

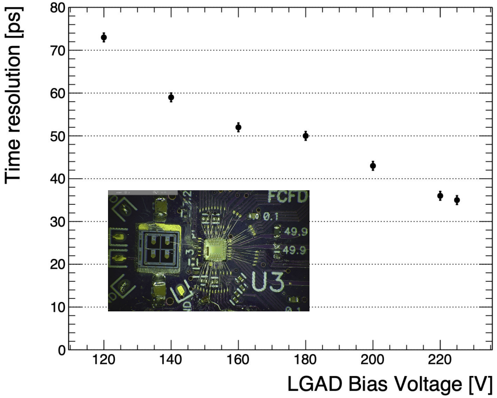
Readout ASIC R&D

Several ongoing activities:

- **EICROC (Omega/Irfu/AGH)**
  - Aspects based on ALTIROC & HGCRoC from HL-LHC upgrades
  - Designed for low sensor capacitance → planned to readout forward detectors with pixel sensors and be bump-bondable
- **Fermilab Constant Fraction Discriminator (FCFD):**
  - Constant fraction discriminator (CFD) to measure signal arrival time → robust against amplitude variations of the signal
- **High Timing Precision System on Chip (HPSoC)**
  - Operate with 10 GSa/s waveform digitization, and use autonomous triggering, feature extraction and multichannel data fusion while providing timing precision <10 ps
- **AS-RoC (SiGe, low power), FAST (large dynamic range), …**



EICROC0



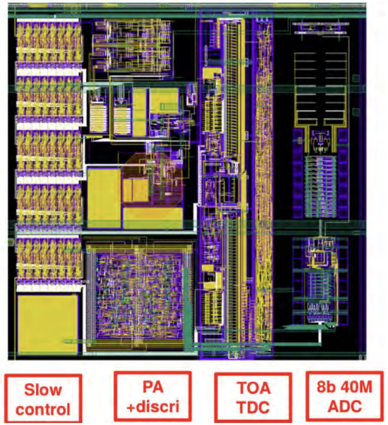
FCFD-v0

Readout ASIC R&D

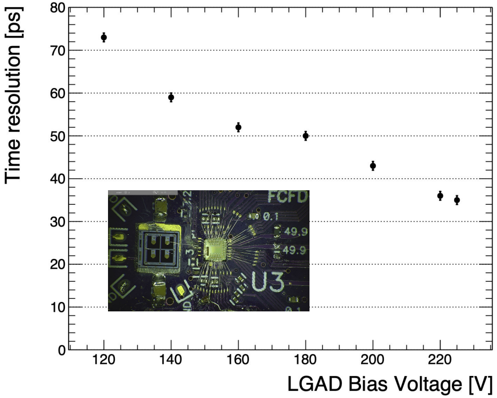
UC SANTA CRUZ

Several ongoing activities:

- **EICROC (Omega/Irfu/AGH)**
  - Aspects based on ALTIROC & HGCRoC from HL-LHC upgrades
  - Designed for low sensor capacitance → planned to readout forward detectors with pixel sensors and be bump-bondable
- **Fermilab Constant Fraction Discriminator (FCFD):**
  - Constant fraction discriminator (CFD) to measure signal arrival time → robust against amplitude variations of the signal
- **High Timing Precision System on Chip (HPSoC)**
  - Operate with 10 GSa/s waveform digitization, and use autonomous triggering, feature extraction and multichannel data fusion while providing timing precision <10 ps



EICROC0

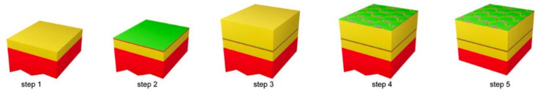


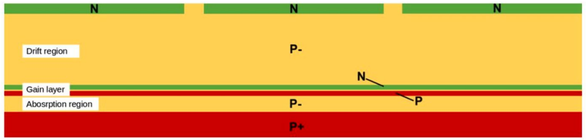
FCFD-v0

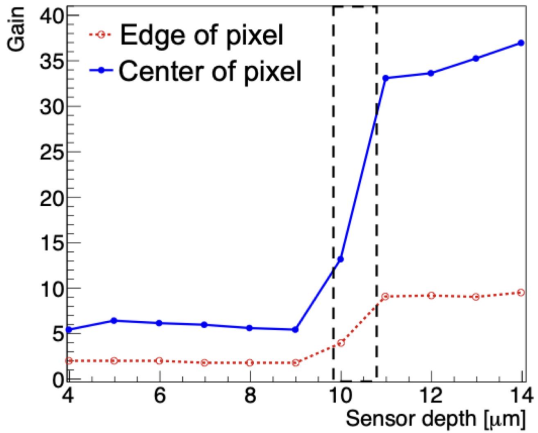
→ For FCC-ee, prefer **longest possible strips length (i.e. large input capacitance) to reduce number of readout channels**, **R&D efforts critical** to achieve desired timing resolution!

HV-CMOS LGADs

- Combination of HV-CMOS technology and LGAD technology
- Internal gain by LGAD-like gain layer and embedded amplification
- Several challenges to overcome:
  - LGAD gain layer has high electric field near the surface, not easy to work with CMOS tech in it
  - LGADs mostly produced on 4” and 6” wafers while CMOS foundries work with 8” wafers
- First successful LGAD CMOS: 130 nm SiGe BiCMOS process by IHP microelectronics PicoAD:
  - Exagonal pads, 65 µm
  - About 25 µm depletion
  - Thinned to 60 µm
  - **Resolution of about ~ 38 ps,**
  - **Very small pixels!**





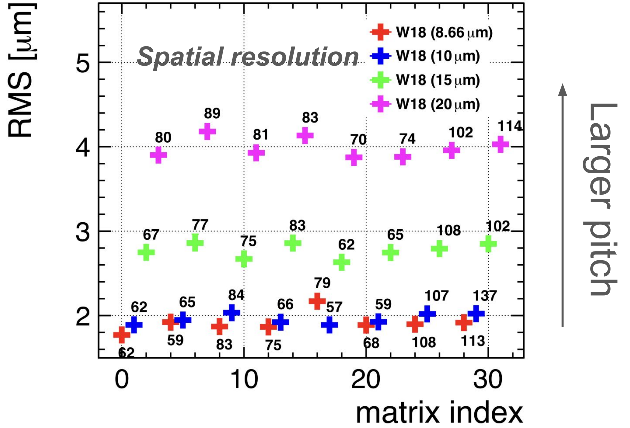


CMOS Sensors without internal gain

UC SANTA CRUZ

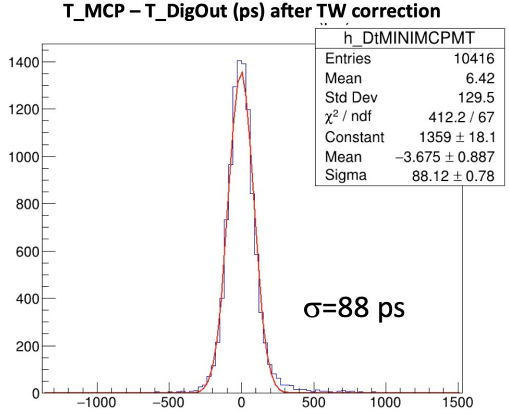
FASTPIX is a **180 nm CMOS monolith project** aiming at combining temporal stamping with excellent position precision

- Lateral doping gradient leads to accelerated charge collection times. Optimization underway
- *Very* small pixels ~8-20 um → impressive spatial resolution!
- Timing resolution ~ 100-200 ps,



MiniCACTUS is a **150 nm CMOS monolith project**

- Front-end mostly optimized for 1 mm^2 pixels with peaking time of 1-2 ns @ 1-2pF
- Resolution of about ~ 90 ps,
- Large pixel, 0.5 x 1 mm^2



Conclusions

UC SANTA CRUZ

Fast timing detectors are proposed as part of a silicon timing layer at FCC-ee

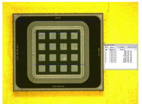
- LGADs are a promising technology for an all silicon wrapper, capable of providing O(10) ps timing resolution and <30um spatial resolution
  - Many experiments (e.g. EIC, PIONEER) in late stages of developing systems that use AC-LGADs → lessons from these experiments useful starting place for FCC-ee!
  - Scaling to FCC will require R&D towards longer strip lengths to reduce channel count, move fabrication to larger wafers to improve yield and reduce costs, etc…
- Fully integrated CMOS systems very promising avenue to explore
  - Capable of extremely small pixels → excellent spatial resolution!
  - Very impressive timing resolutions already achieved

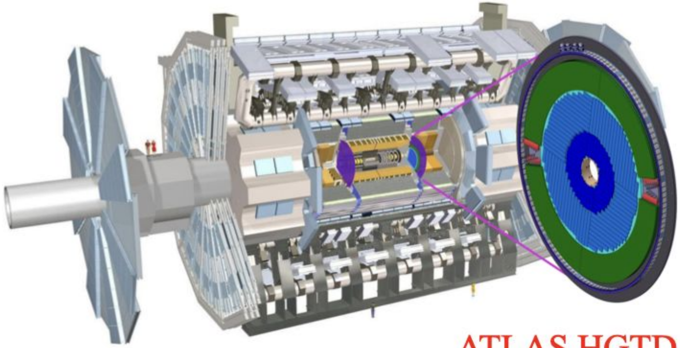
Extra slides

Fast timing @ HL-LHC

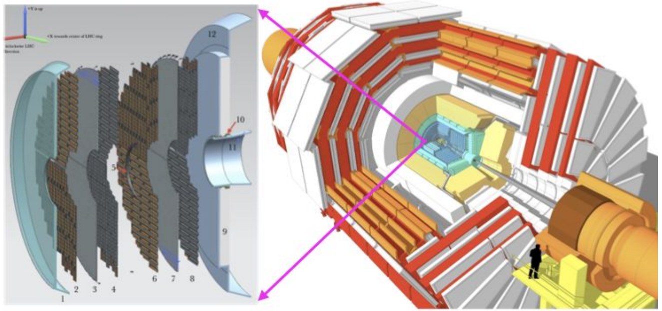
UC SANTA CRUZ

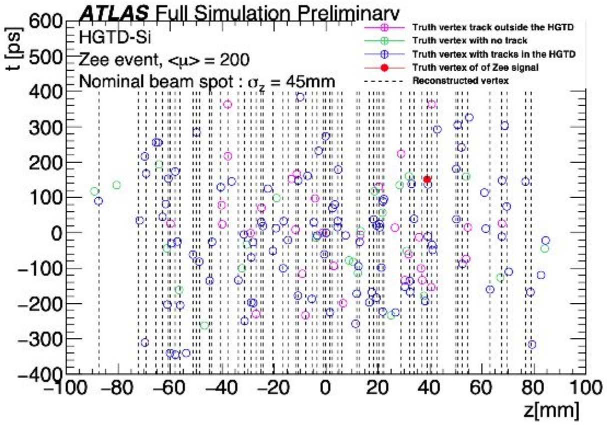
- Unprecedented challenges presented by HL-LHC conditions → require innovation and creativity → precision timing!
- ATLAS High-Granularity Timing Detector (HGTD)
  - Sensors pads 1.3 x 1.3 mm^2
  - Rise time ~ 500 ps
- Extremely useful in dense environments, PID, …

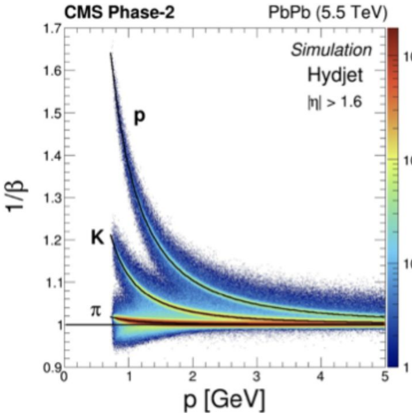




ATLAS HGTD

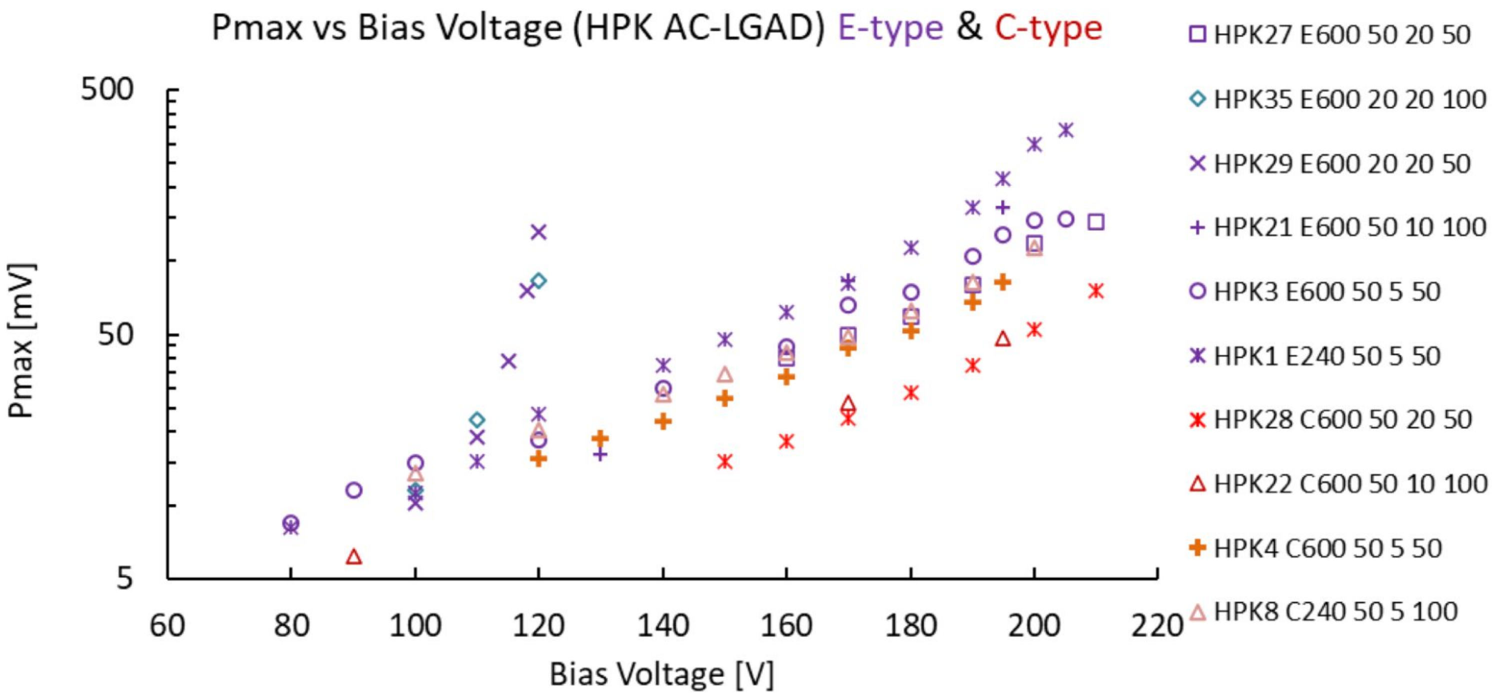






Pmax for various HPK sensors

UC SANTA CRUZ



FASTPIX

UC SANTA CRUZ

- Hexagonal pixels – large signal-to-noise ratios, high detection efficiency and **precise timing**
- Minimizing the maximum distance between charge generation and collection is a first step in the optimization for timing uniformity and is realized by the hexagonal arrangement of collection electrodes and the O(10μm) pixel pitch.
    - With the modified process, a uniform low-dose n-type implant is introduced allowing full lateral depletion of the 25 μm epitaxial layer.