FCC Week 2024

Status of DRD6 Work Package 2

Review of Noble-Liquid Calorimetry

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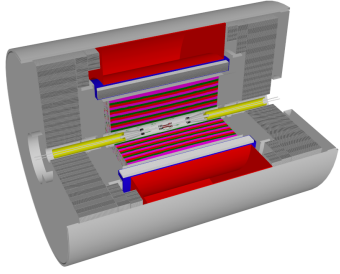
June 11, 2024

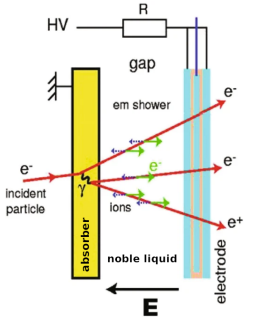
ALLEGRO detector concept

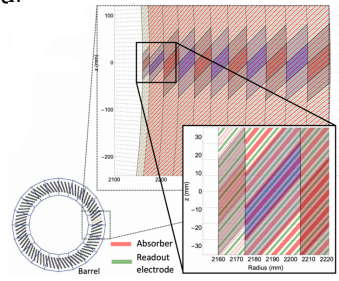
- Proposed general-purpose detector for FCC-ee
- Recently coined as ALLEGRO
  - A Lepton-Lepton collider Experiment with Granular Read-Out
- High-granularity noble-liquid ECAL a central and most studied feature
  - LAr or LKr as active medium, Pb or W absorbers
  - Multi-layer PCB as readout electrode
- Vtx detector, drift chamber and ECAL inside 2 T solenoid magnet, sharing cryostat
- HCAL and muon system outside solenoid
- Optimized for full FCC-ee physics program
  - Focus on PFlow & particle ID performance



Noble-liquid calorimetry

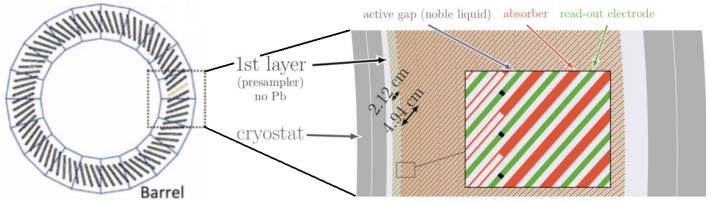
- Sampling calorimetry relying on ionization of active material (liquefied noble gas)
- Based on alternating layers of absorbers, noble liquid and readout electrodes
  - Voltage applied across noble-liquid gap
  - Incident particle ionizes noble liquid
  - e^- (and ions) drift to electrodes and induce current signal
- Successful in many HEP experiments
  - MarkII, DØ , H1, NA48/62, ATLAS
- Advantages: excellent energy resolution, linearity, stability and uniformity, good timing properties
- Challenges: complex mechanical structure inside cryostat, signal feed-through, granularity

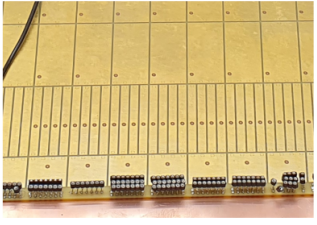




High-granularity noble-liquid calorimeter

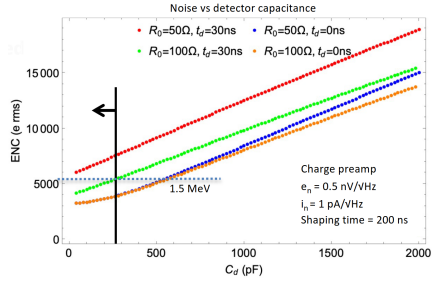
- Printed circuit board (PCB) technology allows "arbitrarily" high granularity
  - Signal traces inside the electrode
  - Target: at least 10x ATLAS granularity
- CERN prototype PCB 58 cm $\times$ 44 cm $\rightarrow$
  - 50° inclination, gives 40 cm (22 χ_0) thick ECAL
  - Split to 16 θ-towers & 12 depth layers
  - Narrow strips in front for π^0 detection
  - 7-layer PCB, complex internal structure
  - 240 cells, readout from inner and outer edge

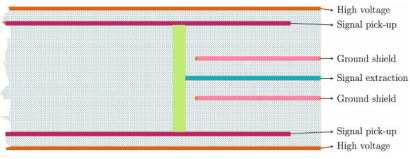


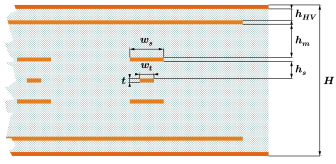


Readout electrode structure & shielding

- Signal traversing under other cells induces *cross-talk* (x-talk) that worsens resolution
- Can be mitigated by sandwiching signal traces between grounded shields
- **Trade-off between x-talk and electronics noise**
  - Shields reduce x-talk but increase capacitance to ground and hence noise
- In PCB v0 baseline is 2x width shields above and below each signal trace
  - Other configurations implemented for studies

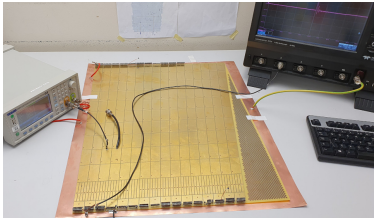


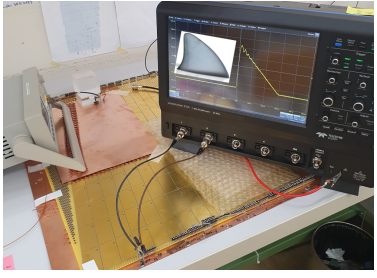




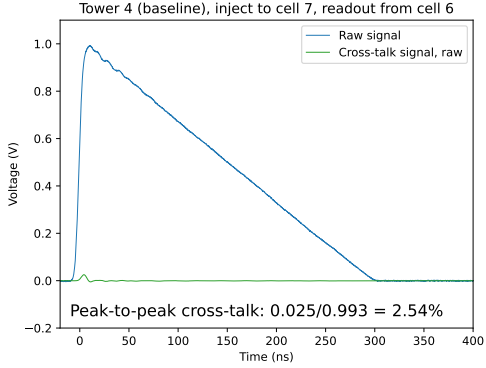
PCB measurement setup

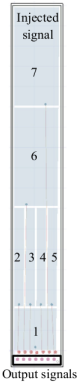
- Electrical properties measured with a table-top setup
- Copper sheet as grouding and "absorbers" above and below the electrode
- Function generator used for injecting shark-fin signal
  - 300 ns wide 1 V peak at 5 ms intervals
  - Mimics the real signal of drifting charges
- Main and x-talk signal read with oscilloscope and analyzed offline
- Extra care needed for good quality measurements
  - Short cables, thorough grounding, impedance matching





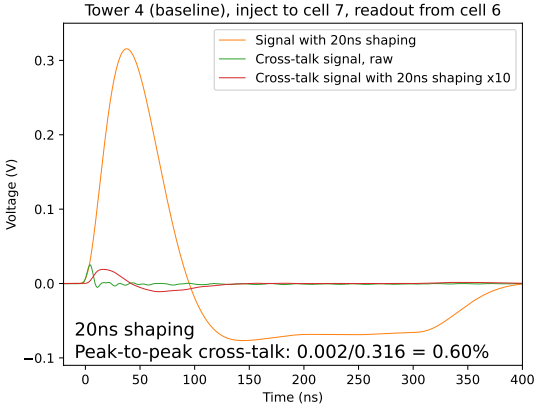
PCB measurements

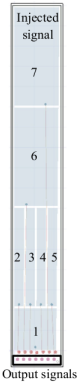




- Compare main signal magnitude to x-talk signal
- X-talk measured as "peak-to-peak" ratio
- 2.5% raw x-talk is too much; fraction of signal lost to each cell
- X-talk ratio of <1% is needed and achieved with *shaping*

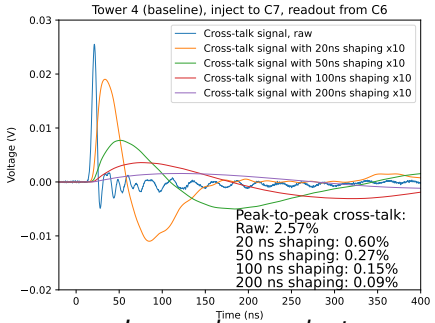
PCB measurements



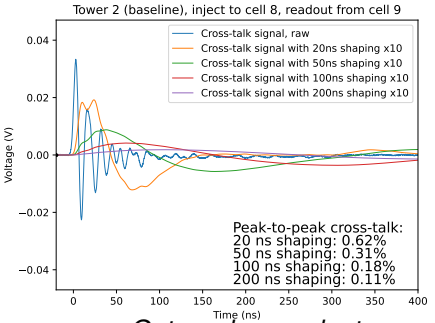


- Signals shaped with ATLAS-style CR-RC^2 shaper
  - Here modeled by an analytical function
  - In reality implemented with electronics
- After shaping x-talk signal too small to see $\rightarrow \times 10$

Cross-talk and shaping time



Inner edge readout

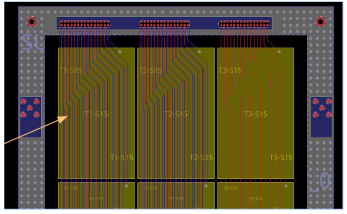


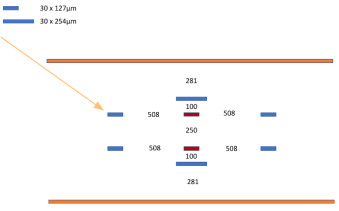
Outer edge readout

- Longer shaping time gives lower x-talk
  - At LHC long shaping times not good due to pileup, but fine in e^+e^-
- X-talk down to 0.1% and less with long shaping time
- Low x-talk seen also in other shielding configurations and outer edge readout
  - Oscillation present but gets "shaped out". Origin to be studied with simulations.

Paris readout electrode prototypes

- New prototype arrived to IJCLab, Paris, in January
- Doubled signal strips, no HV layer
  - 6 copper layers
- Readout only from outer edge
- New shielding configuration: lateral shields between signal traces in 2 towers, 3rd as a reference
- Connectors added by manufacturer
  - No cumbersome soldering needed
- Being characterized and prepared for automated testing





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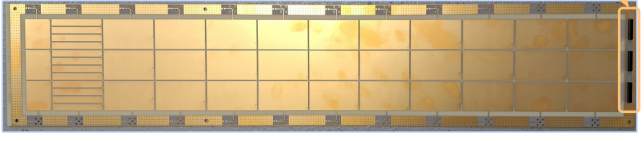
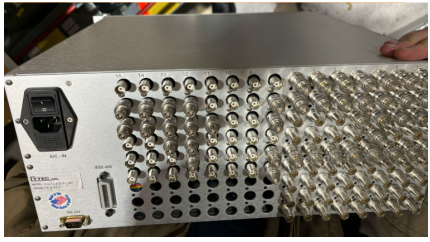
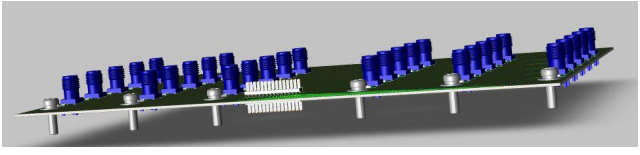
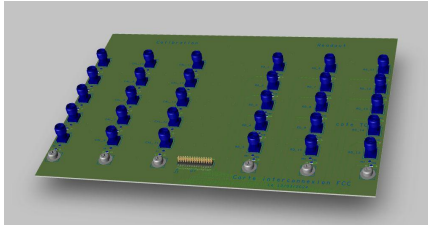


Towards automated measurements

- Fully automated PCB test setup in preparation at IJCLab
  - Preparations and measurements "by hand" not optimal...
- A "fanout board" designed and produced for connecting PCB to a multiplexer
  - Signals routed to an oscilloscope through the multiplexer
- Also calibration signal can be sent through a connector

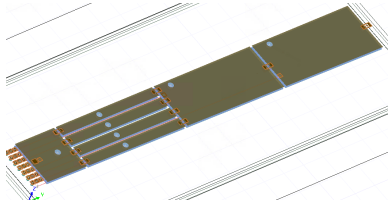


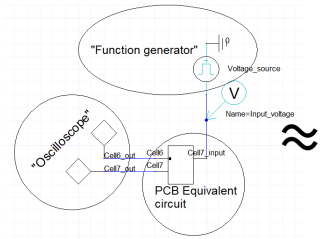




Readout electrode simulation studies

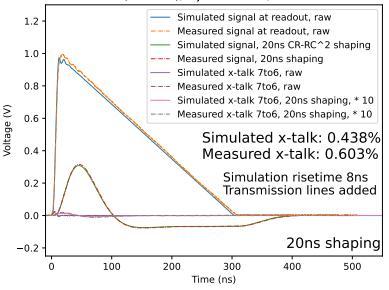
- Electrode properties also studied with simulations
  - Using Ansys Electronics Desktop
- A cut-out of the PCB taken and prepared to equivalent configuration as in the lab
  - Same conductor & dielectric materials, grounding, absorbers, input & output ports
- Model analyzed and converted to equivalent circuit, results analyzed

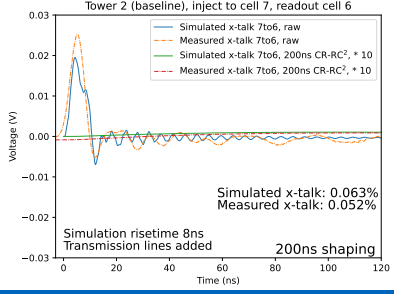




PCB simulation studies

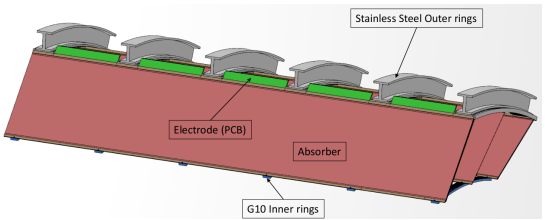
- Main signal and x-talk signal shapes in good agreement with measurements
  - Accounting for the finite turn-on of the analog signal
- X-talk in the same ballpark with 20 ns shaping
  - Exact replication of laboratory setup hard to achieve
  - With 200 ns shaping time x-talk values agree well
- Agreement sufficient for trying new ideas
  - Different shielding scenarios (e.g. lateral shields)
  - 6-layer PCB with one-sided or alternating shields

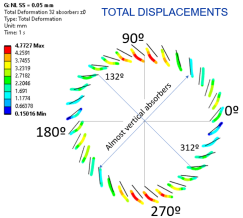


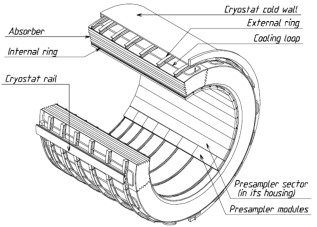


Barrel ECAL - mechanical design

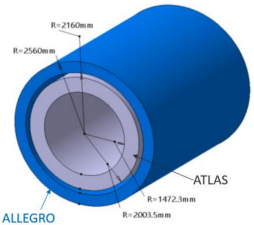
- ATLAS LAr ECAL used as reference
  - Larger radius, new electrode geometry
- Finite element analysis used for structural element design (strength, size)
- Clever solutions needed for making the structure possible to build!







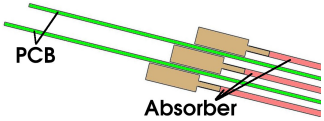
ATLAS liquid argon calorimeter general layout

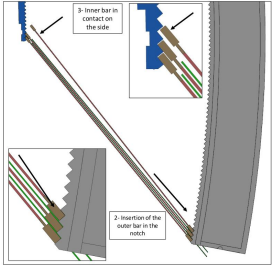


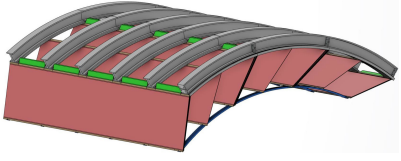
EM calorimeter size comparison

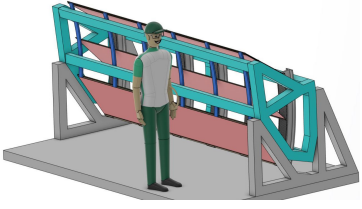
Structural design

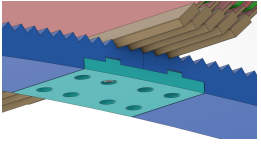
- Assembly of the barrel ECAL alone a major challenge
  - Complex and heavy structure of PCB's and absorbers to be operated in cryogenic temperatures
- Ability for precise positioning of components has to be planned from the start
- Accessing PCB readouts through the support structure affects also PCB design
- Several solutions being investigated by our engineers in Marseille and at CERN





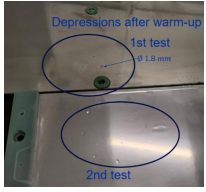


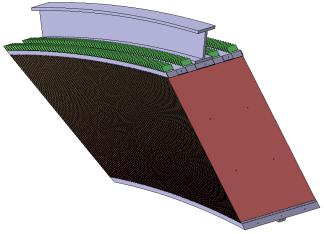


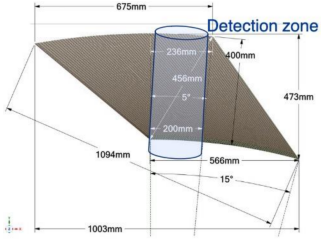


Absorbers & test-beam prototype

- First absorber prototypes produced with 1.8 mm of lead with 50 μm steel cladding
- Immersed in liquid nitrogen, small depressions seen after cold test
  - Origin being investigated, thicker 100 μm steel cladding being studied
- Design of test beam prototype frozen by 9/2025
  - 64 electrodes and absorbers
  - Big enough for containing a typical shower
  - To be placed in a cryostat for beam tests





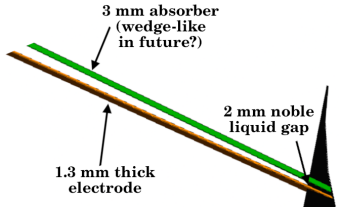


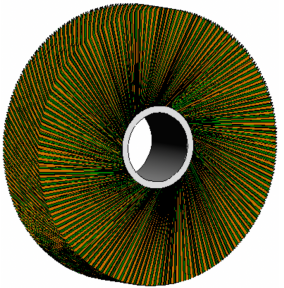
Endcap EM calorimeter

- Noble-liquid based ECAL, designed to feature:
  - Thin absorbers (high granularity)
  - Readout from outside faces only (no dead material), uniformity in ϕ

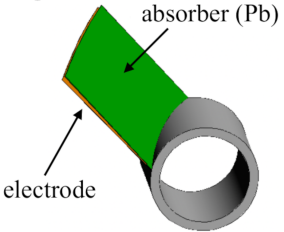
$\Rightarrow$ **Turbine-like geometry as one option**

- $\sim$240 absorbers and electrodes each
- Geometry ported to FCC-SW for FCC-ee simulations
- **See talk by Erich Varnes later in this session!**





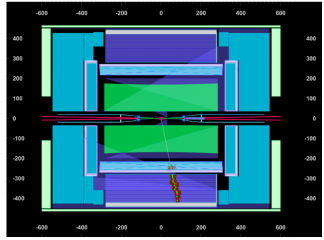
single unit cell:

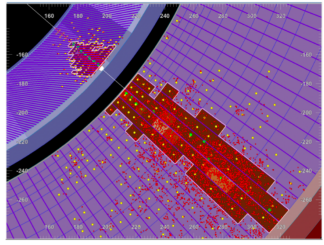


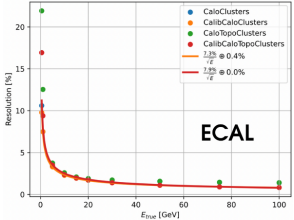
drawings by Rob Walker

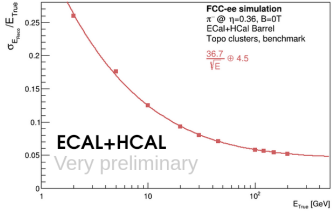
Detector simulation & clustering

- Optimal granularity & materials being studied with simulations
  - Find optimal granularity for π^0/γ separation
  - LAr or LKr as liquid, Pb or W as absorbers
- Full-Sim of ALLEGRO being built to FCC-SW
  - ECAL+HCAL topo-clustering, ML-based calibration
  - Next: add tracking and Particle Flow
- EM resolution with a sampling term of 7-8%
- **More on simulation by B. François in this room at 6pm**



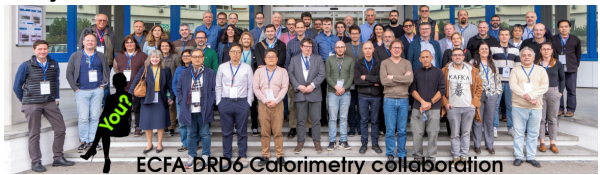






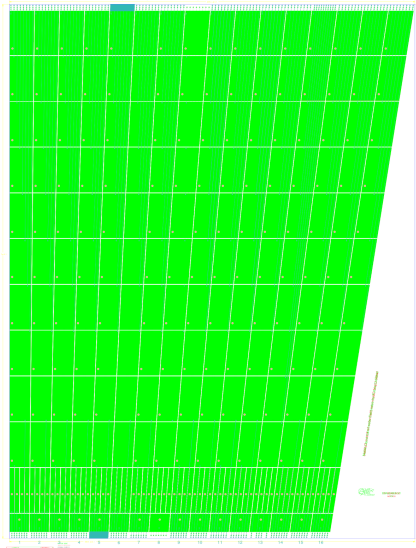
Conclusions & outlook

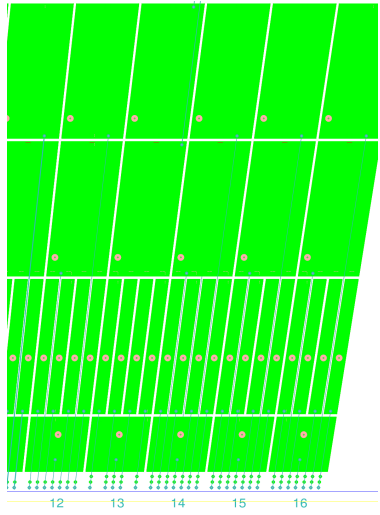
- ALLEGRO is a general-purpose FCC-ee detector concept
  - Multi-layer PCB's as readout electrodes allow high granularity
- Actively prototyping electrodes and absorbers
  - Test-beam prototype to be built by 2027-28
- Work towards readout electronics will start in 2024/2025
  - "Cold electronics" inside the cryostat a possibility
    - \+ Less noise, no analog feed-throughs
    - – Need very low power, hard to repair
- ECFA DRD6 Calorimetry collaboration founded in April
  - Noble-liquid calorimetry in work package 2
- Team is growing fast, already 20 institutions joined!
  - **Ideal time to join ALLEGRO!**



ECFA DRD6 Calorimetry collaboration

Back-up

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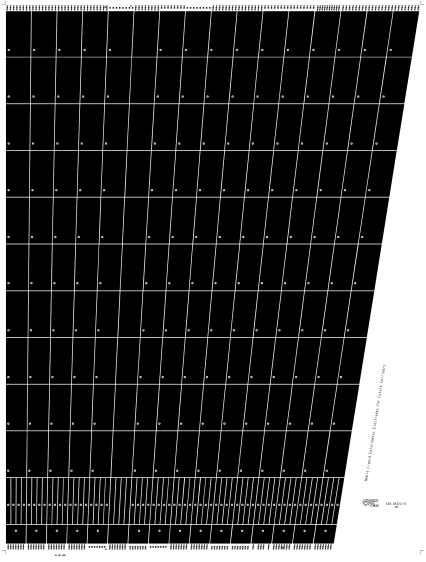
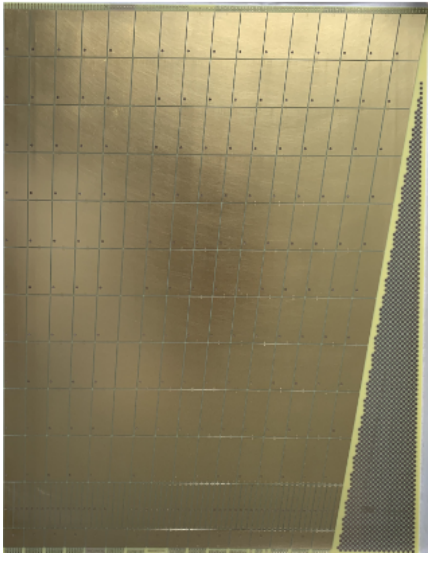
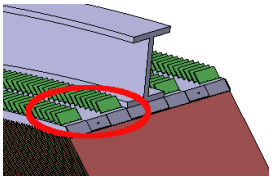
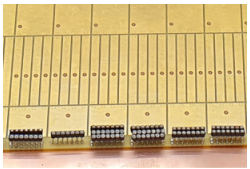


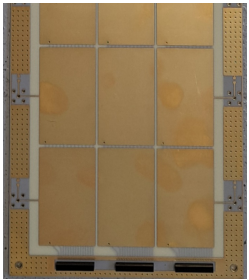


Plans for next PCB prototype

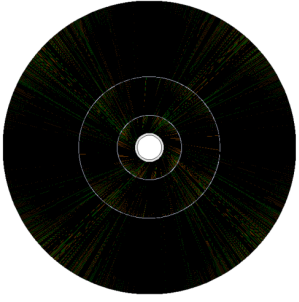
- Simulation studies underway for optimizing granularity
- Readout from outer edge only for minimizing dead material
  - X-talk of strip layer a challenge due to smaller signal
  - Singnal traces need to be "funneled" thru support structure
  - readout pins become tiny
- Would only one shield per signal strip be sufficient?
  - 6-layer PCB easier to manufacture and thinner $\rightarrow$ increased sampling ratio
- Need to re-design readout connections
  - Industry standard connector?
  - Soon results from Paris prototype $\Rightarrow$







- Another consideration is the variation of the gap with radius
  - means that response is very different at the inner and outer radii (41 cm and 275 cm)
- To mitigate this, the detector can be subdivided into a set of nested cylinders:



Tradeoff between minimizing variation in gap width vs. minimizing transitions/dead areas

In this example, each cylinder has $r_o/r_i \approx 1.9$