The OBELIX sensor for the Belle II VTX upgrade

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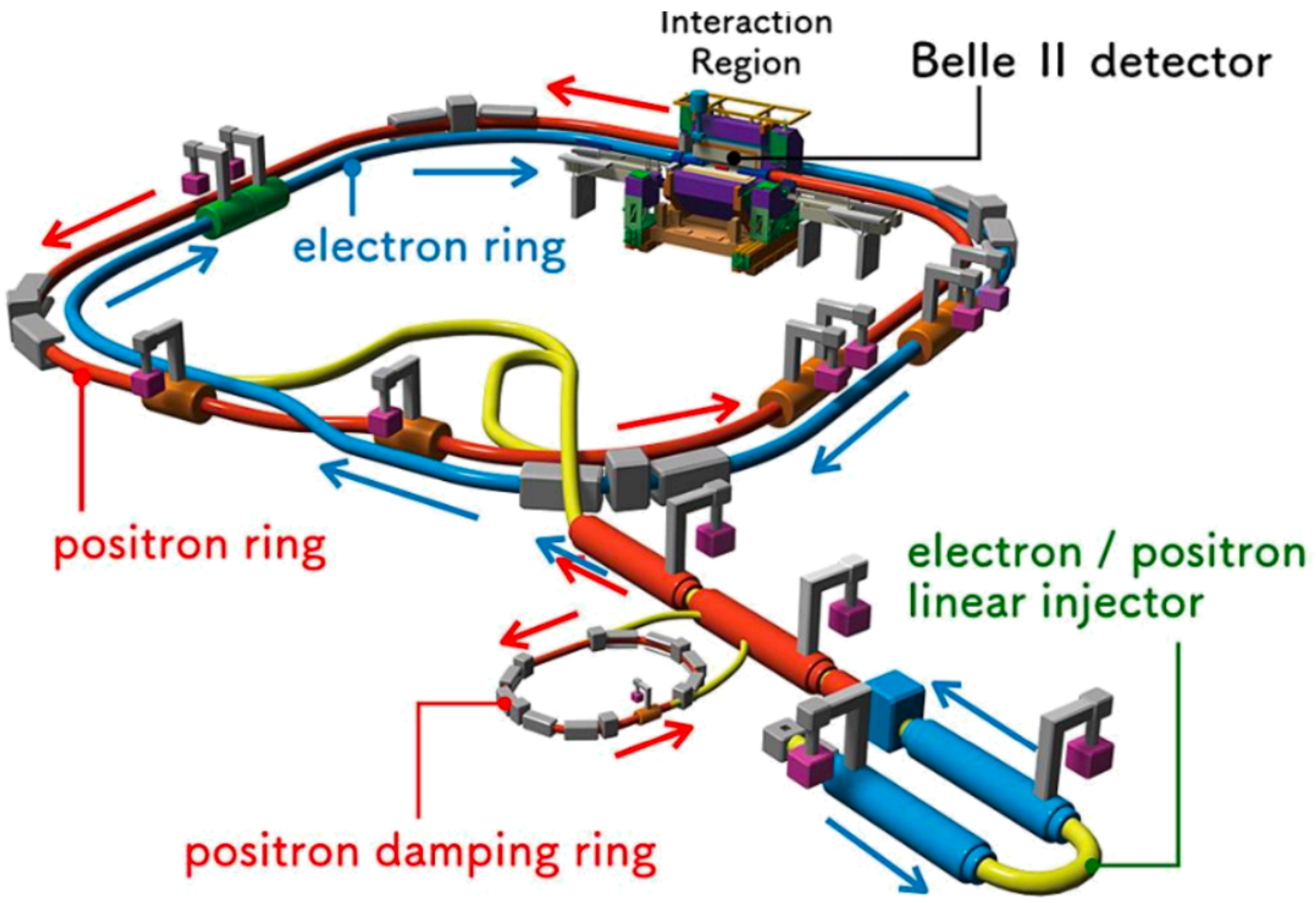
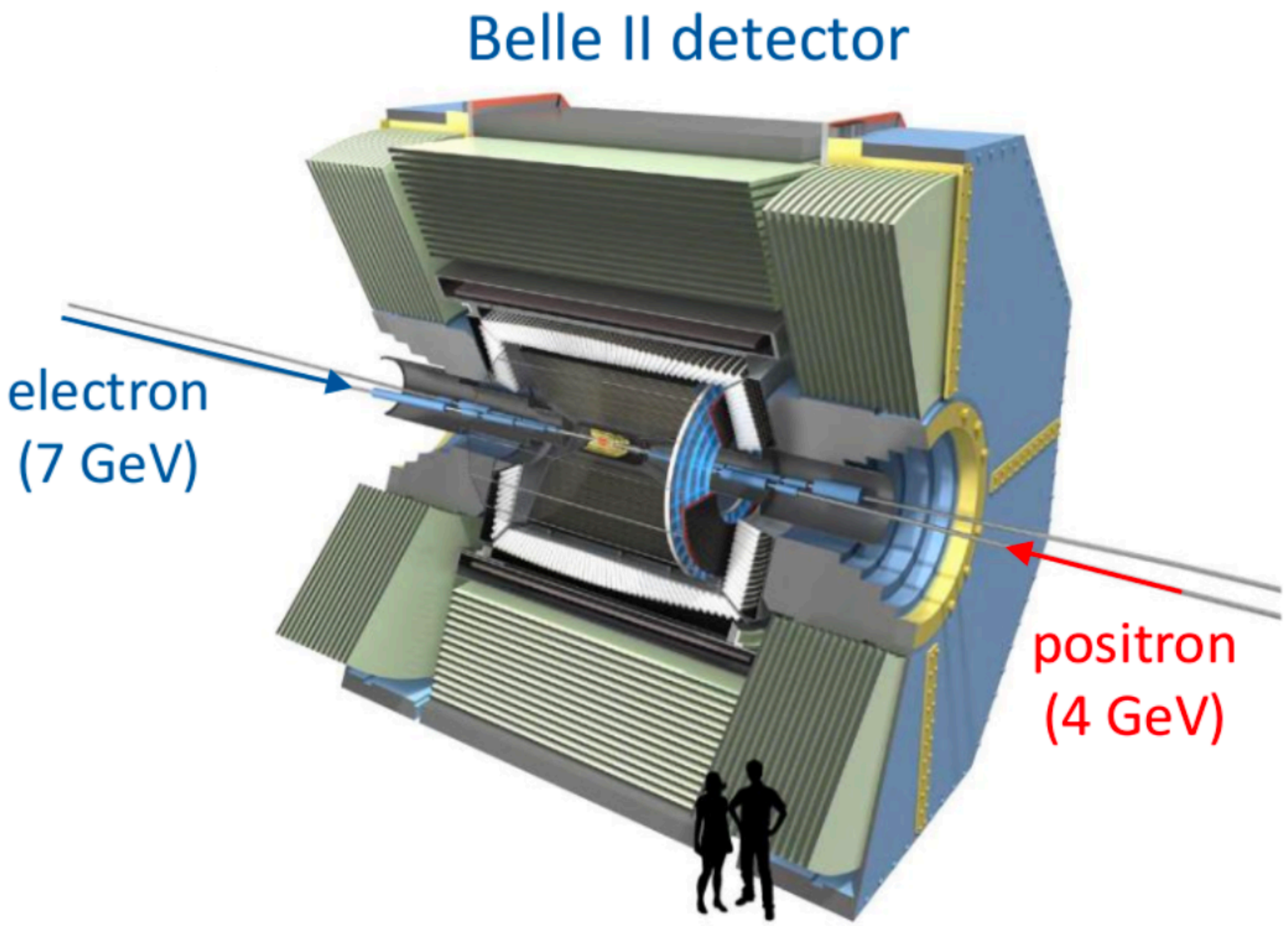
The Westin St. Francis

Belle II @ SuperKEKB

- Luminosity frontier experiment to search for Physics beyond the Standard Model
  - e^+e^- asymmetric collision at the $\Upsilon(4S)$
  - High current / nano-beams, challenging background conditions
- Achieved in run 1:
  - $\mathscr{L} = 4.7 \times 10^{34}$ cm^{-2} s^{-1}, $\int \mathscr{L} = 428$/fb
- Target:
  - $\mathscr{L} = 6 \times 10^{35}$ cm^{-2} s^{-1}, $\int \mathscr{L} = 50$/ab

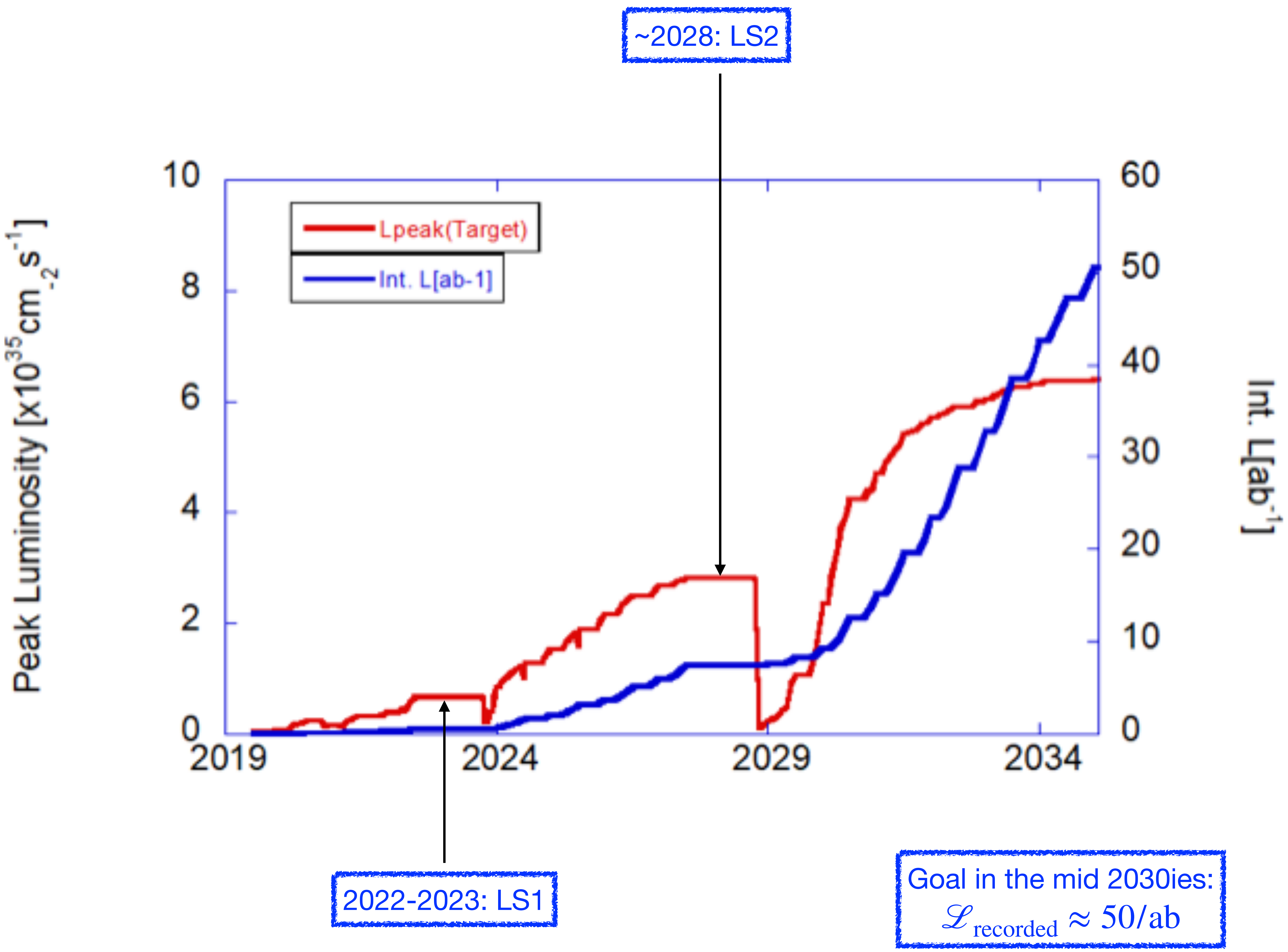




Belle II timeline

Luminosity projection

- **Run 1 2019-2022**
  - Pixel Detector (PXD): layer 1 + only 20% of layer 2
  - Full 4-layers strip detector (SVD)
- **Long Shutdown 1 (June 2022 to end of 2023)**
  - Several accelerator and detector maintenance & improvements
  - Installation of 2 layer PXD + SVD
- **Run 2: started in Jan 2024**
  - Instantaneous luminosity ramping up in next years

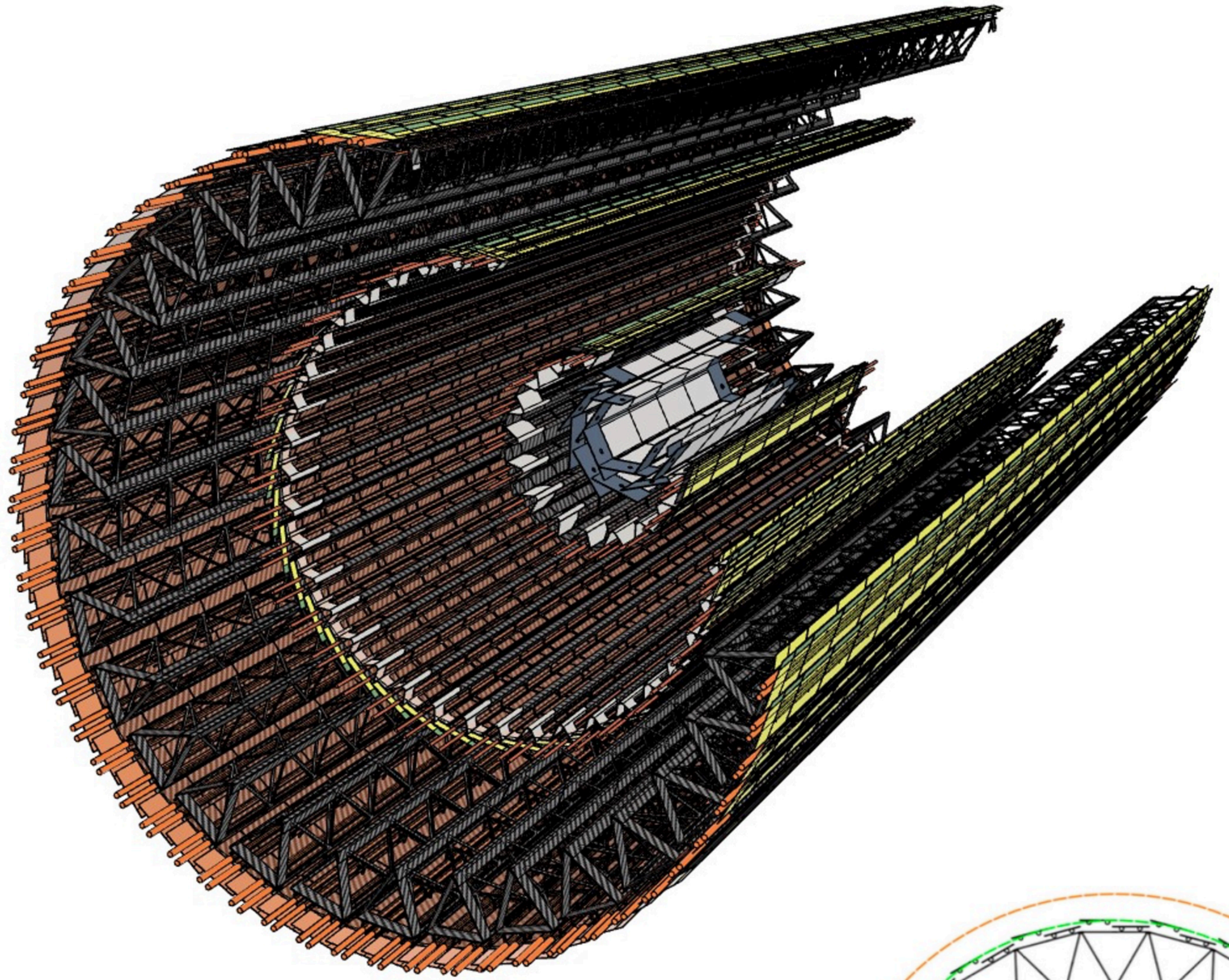


Motivation for vertex upgrade in LS2

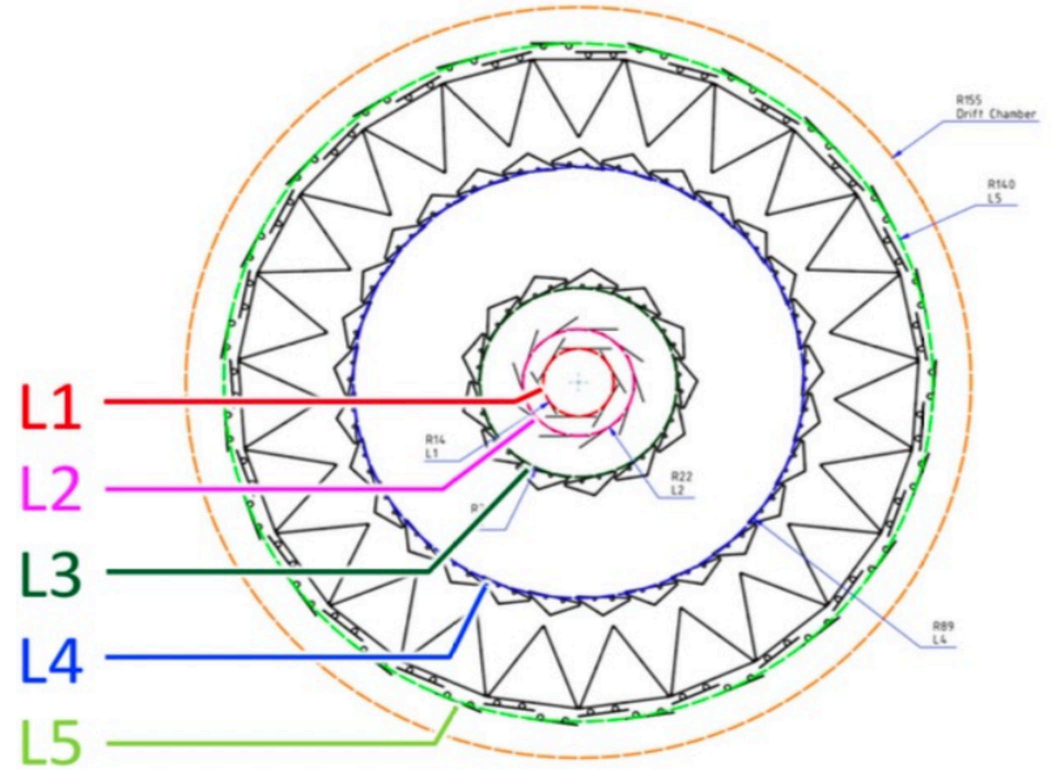
- Steep path to higher luminosity
  - x13 in peak luminosity, x2 LER/HER beam currents, x3 smaller beam size
  - Background in the VXD is expected to increase steeply reducing the safety margin for reliable tracking/vertexing
- Upgrade of accelerator complex required to reach 6×10^{35}/cm^2/s
  - This might include a major redesign of the Interaction Region (IR)
- Prepare a safety net in case of failure of detector components or accidents
- The new VTX is part of the Belle II Upgrade Program
  - Framework CDR ready: available soon on arXiv!

The VTX upgrade proposal

Planned for LS2 ~2028



- 5 straight detector layers with depleted monolithic active pixel sensors (DMAPS) operated at room temperature
- The same sensor is used in all layers: **O**ptimized **BEL**le II p**IX**el sensor (OBELIX)
  - Some features disabled on inner layers
- iVTX: L1, L2
  - All silicon ladders
  - Air cooling (stringent constraints on power consumption)
- oVTX: L3, L4, L5
  - Carbon fiber support frame
  - Cold plate with liquid cooling



	L1	L2	L3	L4	L5	Unit
Radius (mm)	14.1	22.1	39.1	89.5	140	mm
#Ladders	6	10	17	40	31	
#Sensors	4	4	7	16	2x24	per ladder
Expected hit rate*	19.6	7.5	5.1	1.2	0.7	MHz/cm2

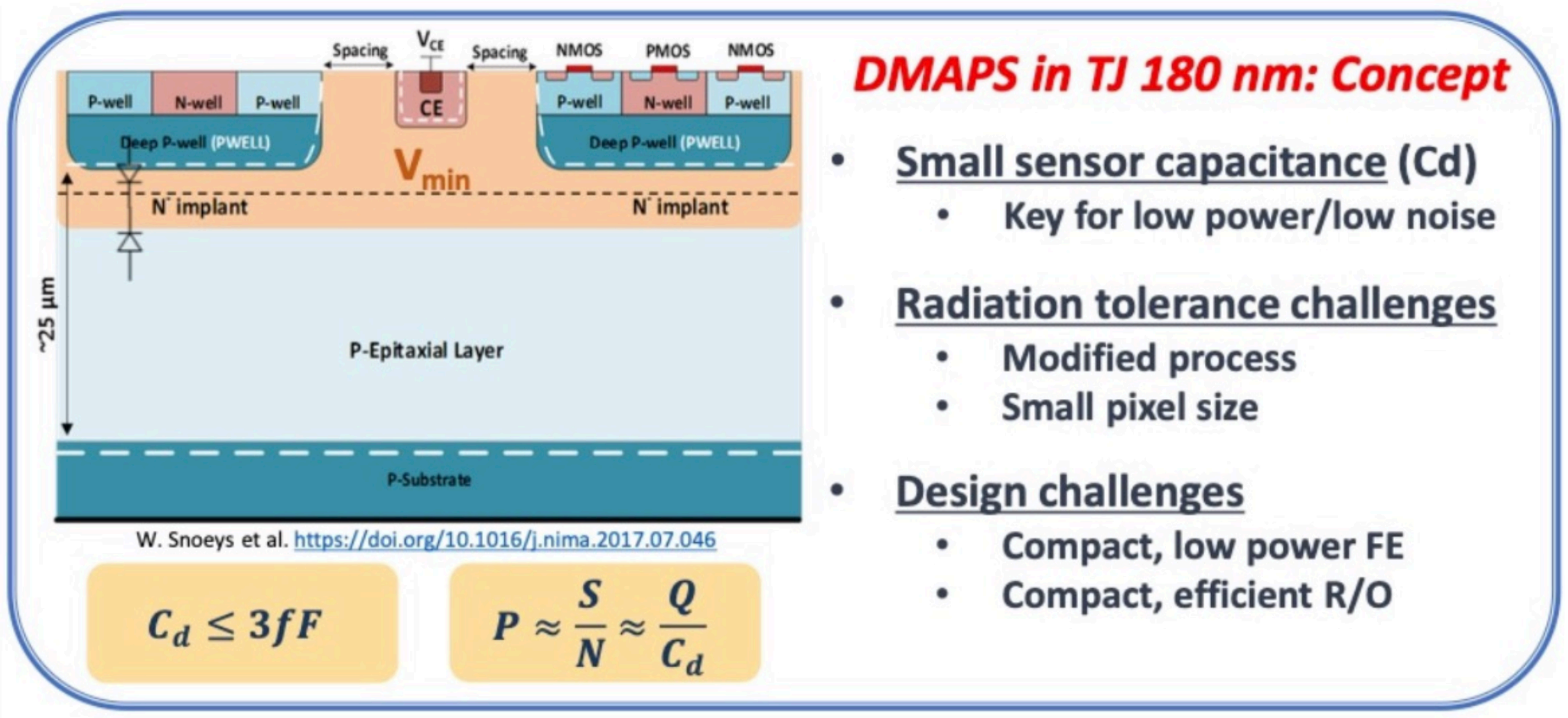
L5 length ~70 cm

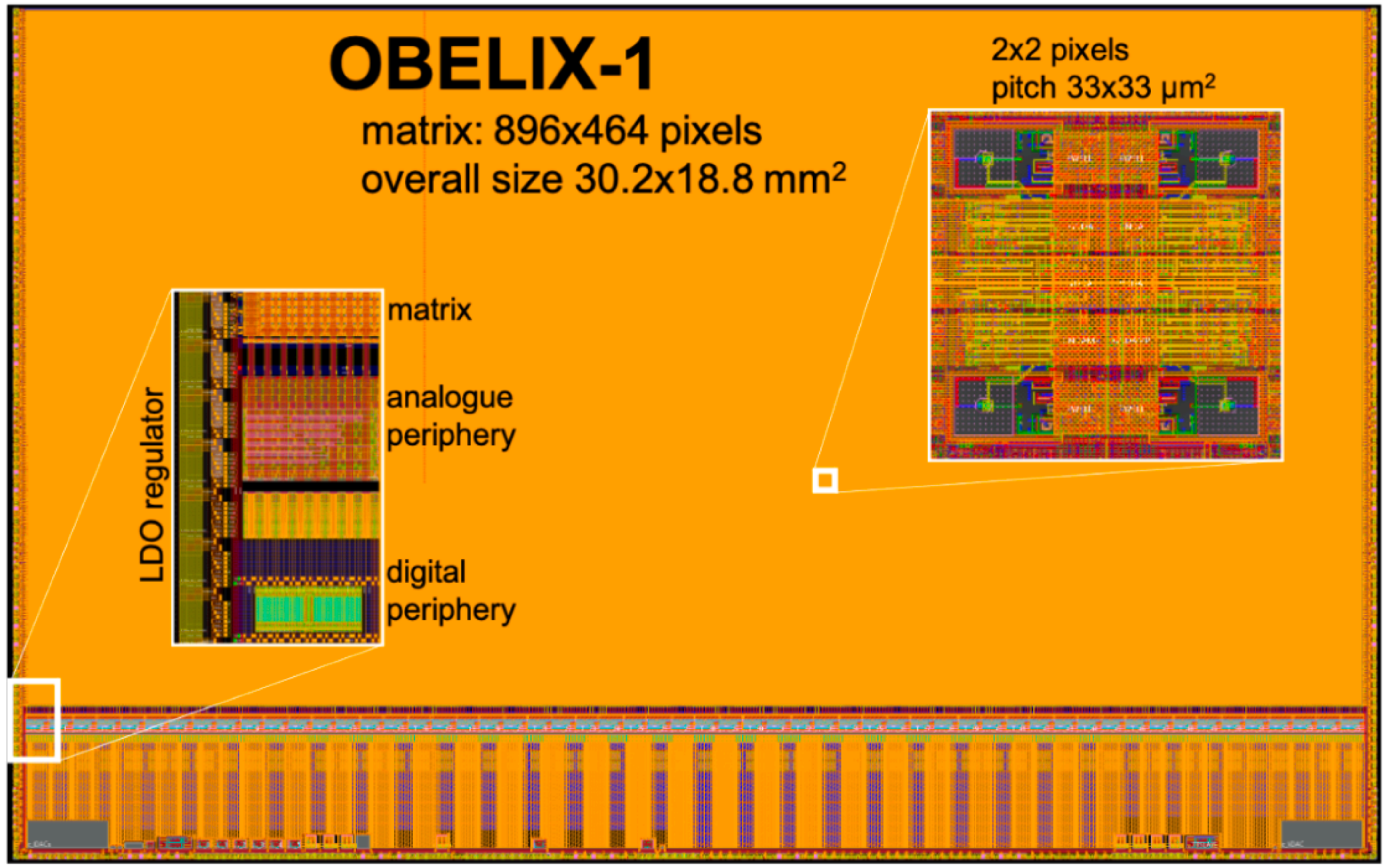
Requirements for VTX/OBELIX

- High hit efficiency at high hit rate
  - Spatial resolution < 15 μm, temporal resolution < 100 ns
  - Max. hit rate 120 MHz/cm^2
- Material budget
  - iVTX 0.2%, oVTX 0.3-0.8% of X_0
- 10 μs latency at 30 kHz for more complex Belle II trigger
- Power dissipation 200 mW/cm^2
- Total ionizing dose (TID): 1 MGy (100 Mrad), total fluence: 5×10^{14} n$_{eq}$cm^{-2}
- On chip power regulators to reduce amount on supply cables
- In oVTX
  - Hit timing capability for background reduction (oVTX)
  - Trigger capability for increased stability/ redundancy (oVTX)

The OBELIX chip

- Matrix inherited from TJ-Monopix2 developed for ATLAS (Tower 180 nm modified imaging technology)
- Dimensions adjusted to VTX geometry (464 rows and 896 columns, 29.60×15.33 mm^2 active area)
- Low dropout regulators (LDOs) to allow a wide input supply voltage range of 2 to 3 V
- Clock frequency for the timestamp and trigger unit is 21.2 MHz (timestamp length 47.2 ns)
- Trigger unit with 2-stage trigger memory (data loss of less than 0.02% at the design trigger latency of 10 μs and hit rate of 120 MHz/cm^2)
- 320 Mbit/s output





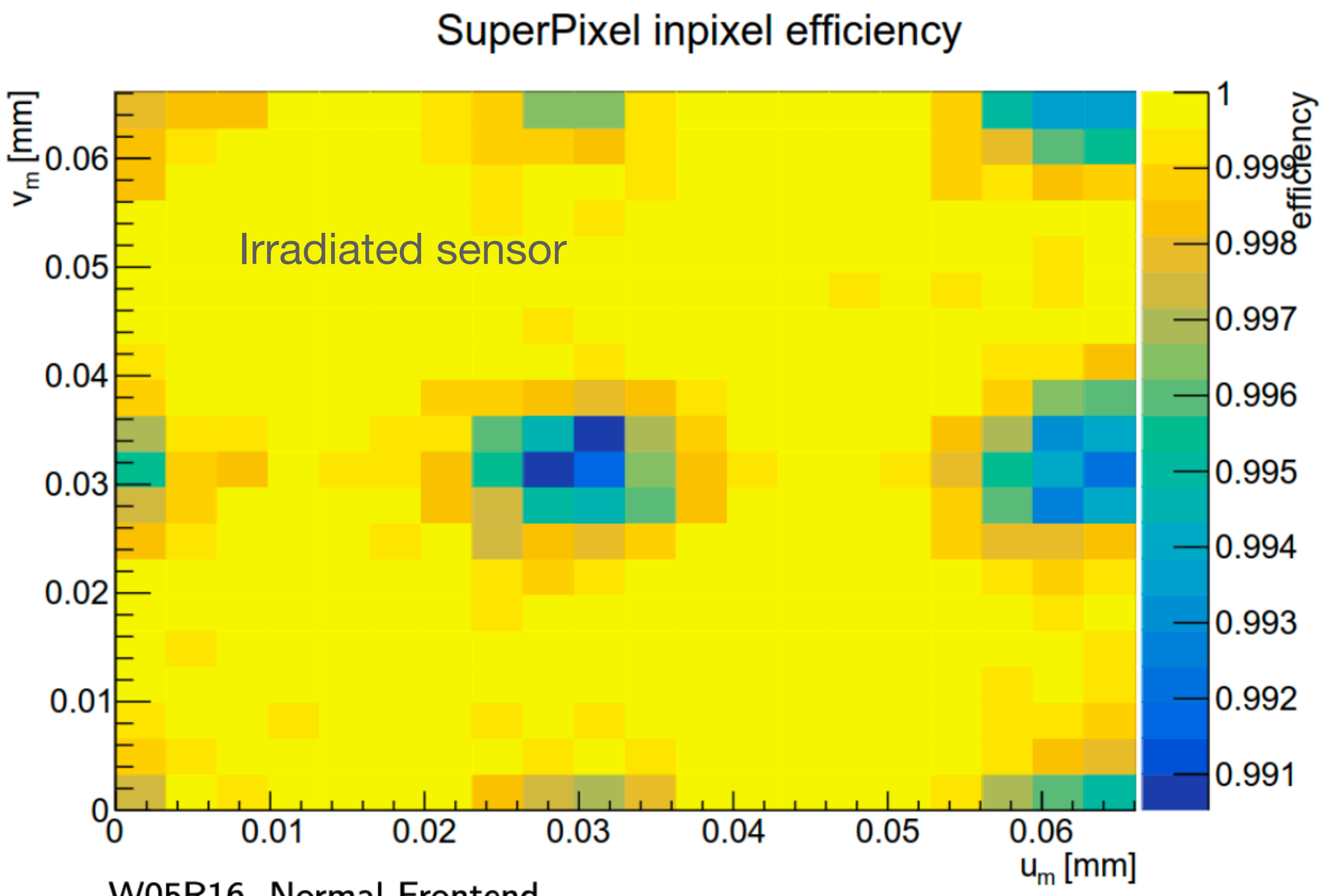
TJ-Monopix 2 characterization

2022-2024

Chip SN	Irradiation	Substrate
W02R05	None	Epi
W05R16	p^+, 5×10^{14} n_{eq}	Epi
W08R19	None	Epi
W14R12	None	Cz

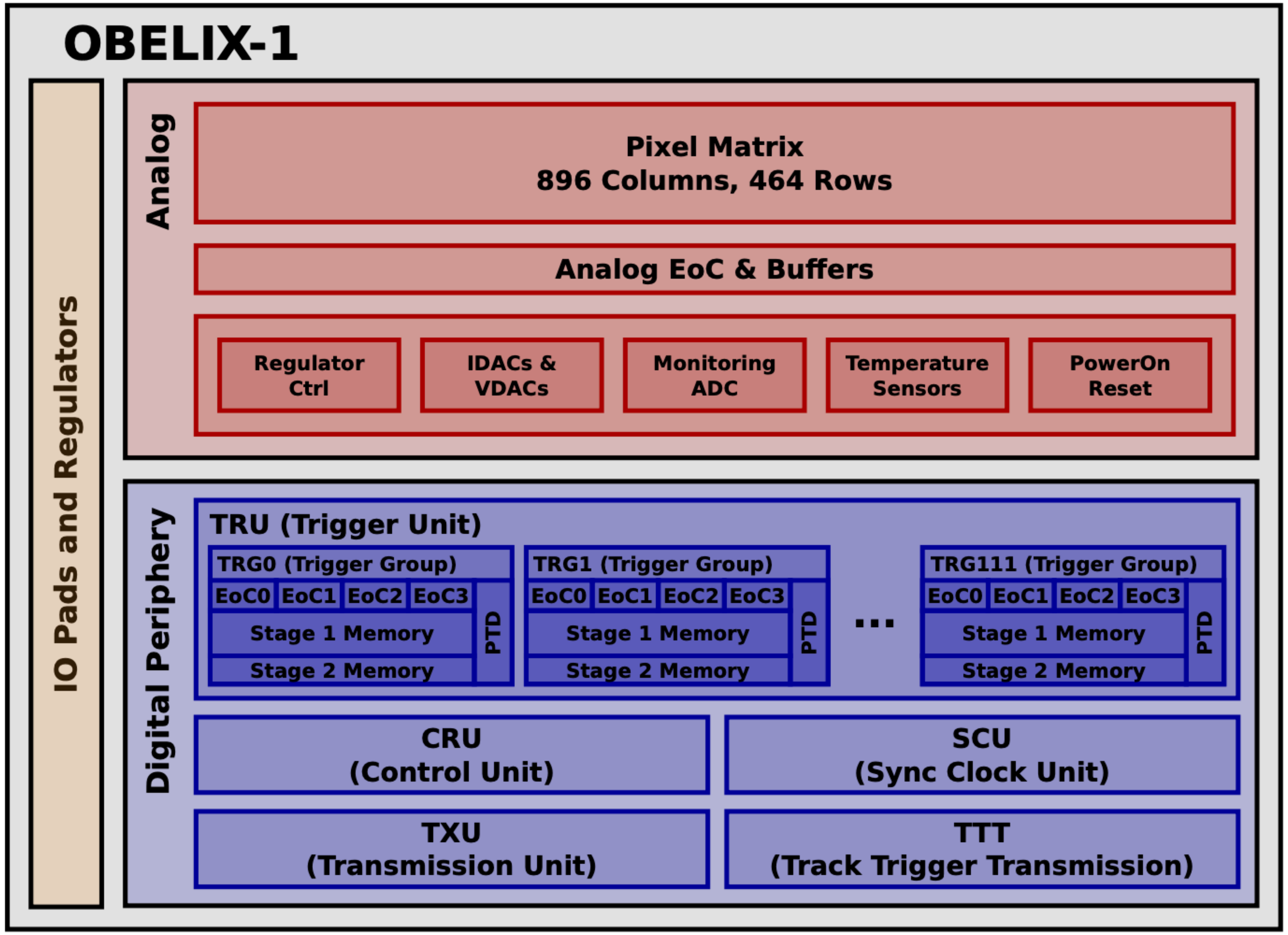
Chip SN	Frontend	Efficiency
W05R16	Normal	0.9999
	Normal Cascode	0.9979
	HV Cascode	0.9913
	HV	0.9811

- Several beam test campaigns @ DESY
(5 GeV electrons, room temperature measurements)
    - July 2022: not irradiated sensors & high threshold 500 e^- (un-tuned chips)
        - efficiency ~99%, position resolution ~9 μm
    - July 2023: low threshold 250-300 e^- & irradiated sensor 5×10^{14} n_{eq} cm^{-2}
        - confirmed good performance & high efficiency after irradiation, increasing bias
    - July 2024: repeat on irradiated sensor with high fluence & TID 1 MGy



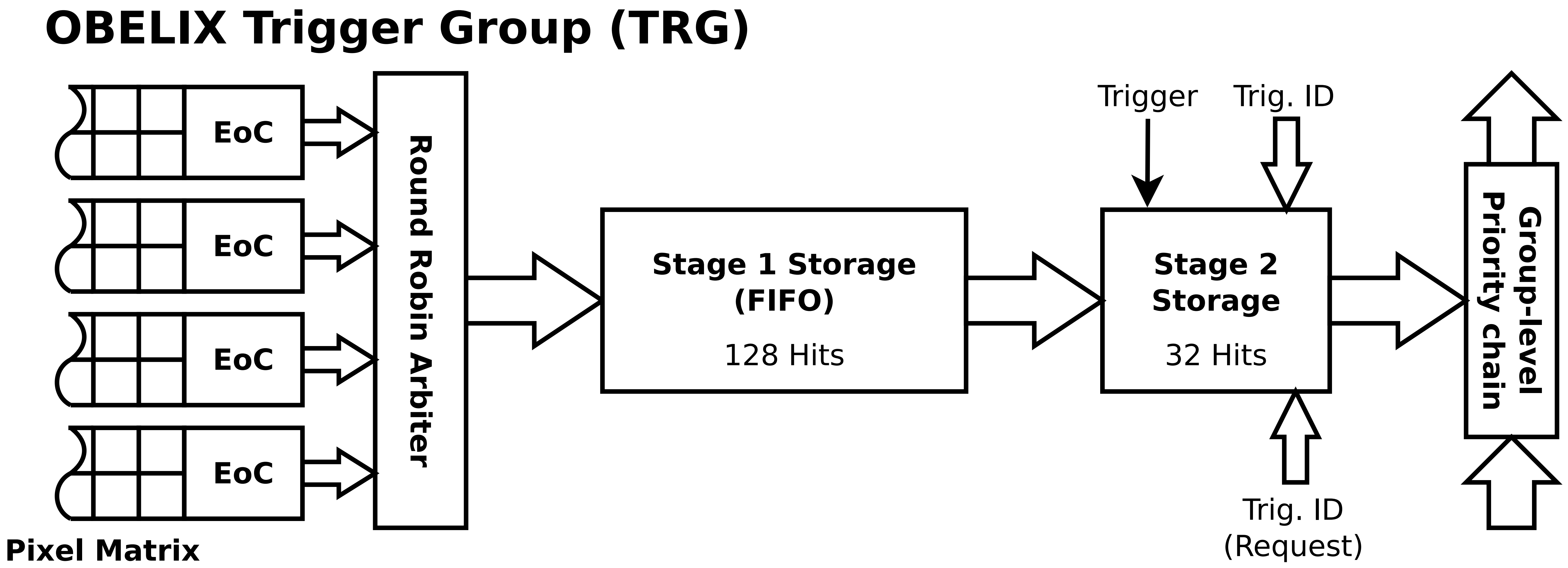
W05R16, Normal Frontend

OBELIX block diagram



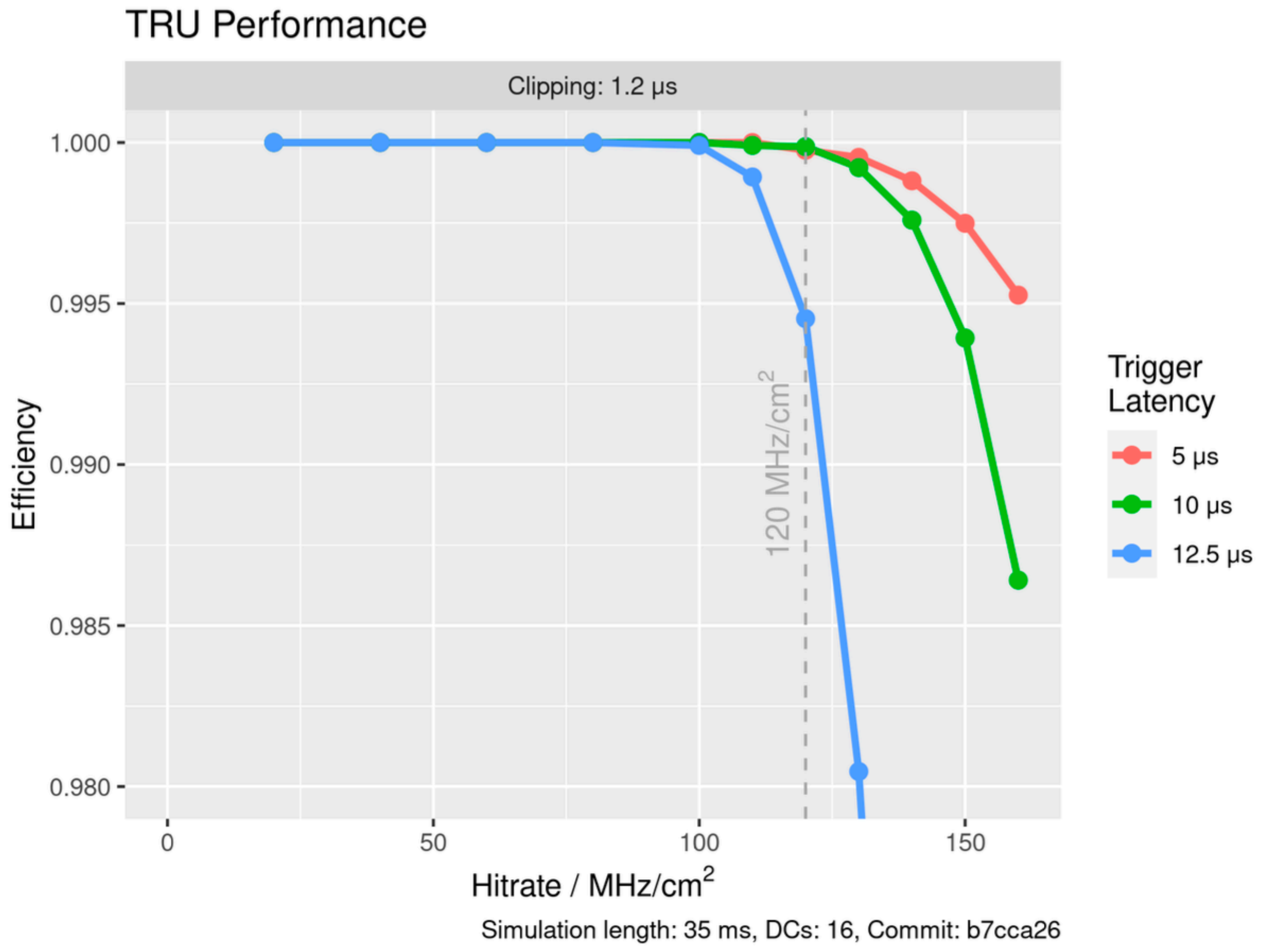
- Analog part/matrix inherited from TJ-Monopix2
  - Column drain architecture
- Power
  - On-chip LDOs
- New digital periphery
  - TRU: Pixel readout, trigger processing
  - PTD: Part of TRU for precision timing
  - TTT: Fast transmission in parallel for contribution to Belle II Trigger

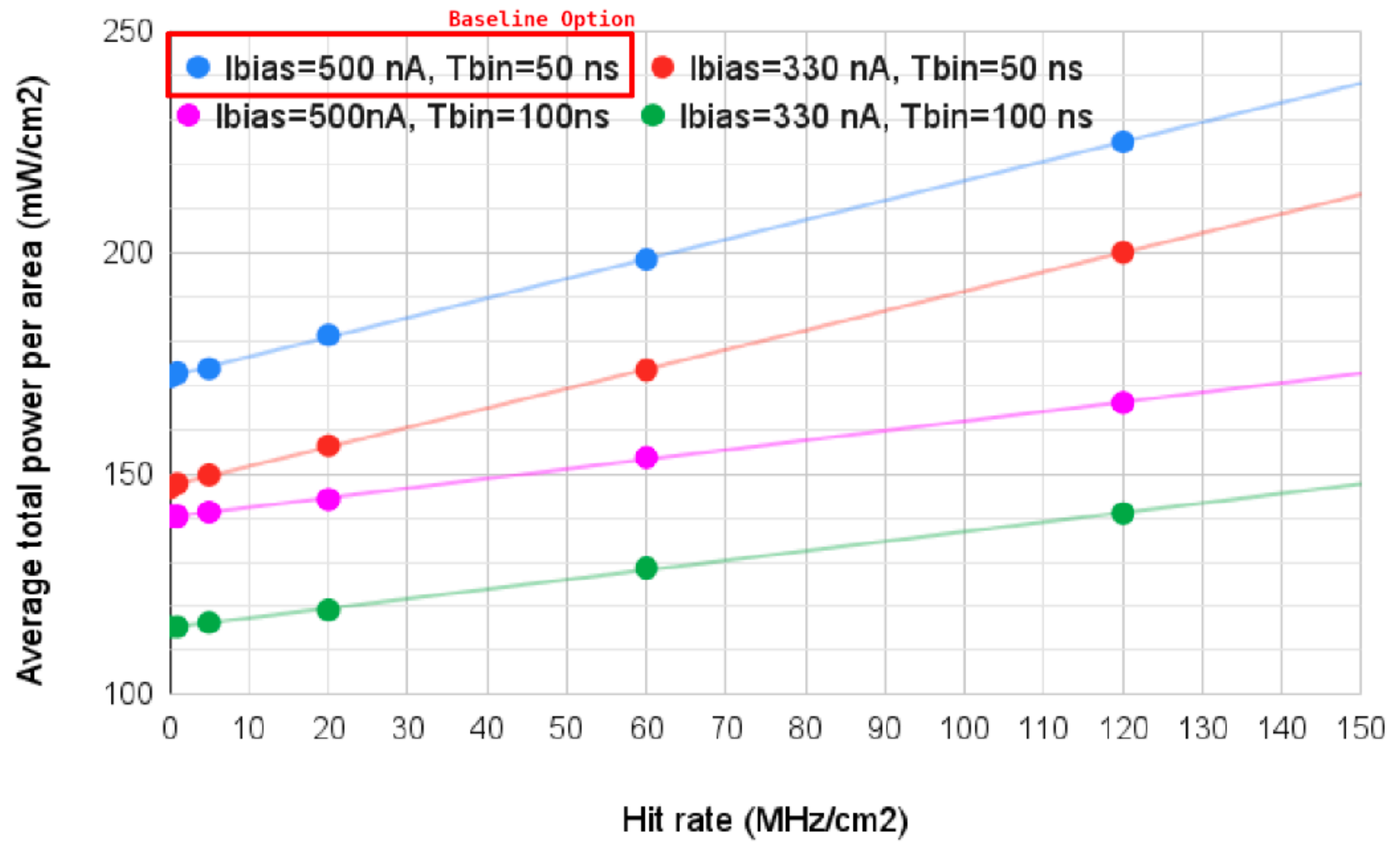
OBELIX Trigger Unit



- 112 trigger groups for 8 columns each
  - Sophisticated 2 stage memory design
    Stage 1: pre-trigger buffer SRAM, low power
    Stage 2: associative memory to match trigger, power hungry
- Buffer size optimized to achieve the target power consumption and hit rate

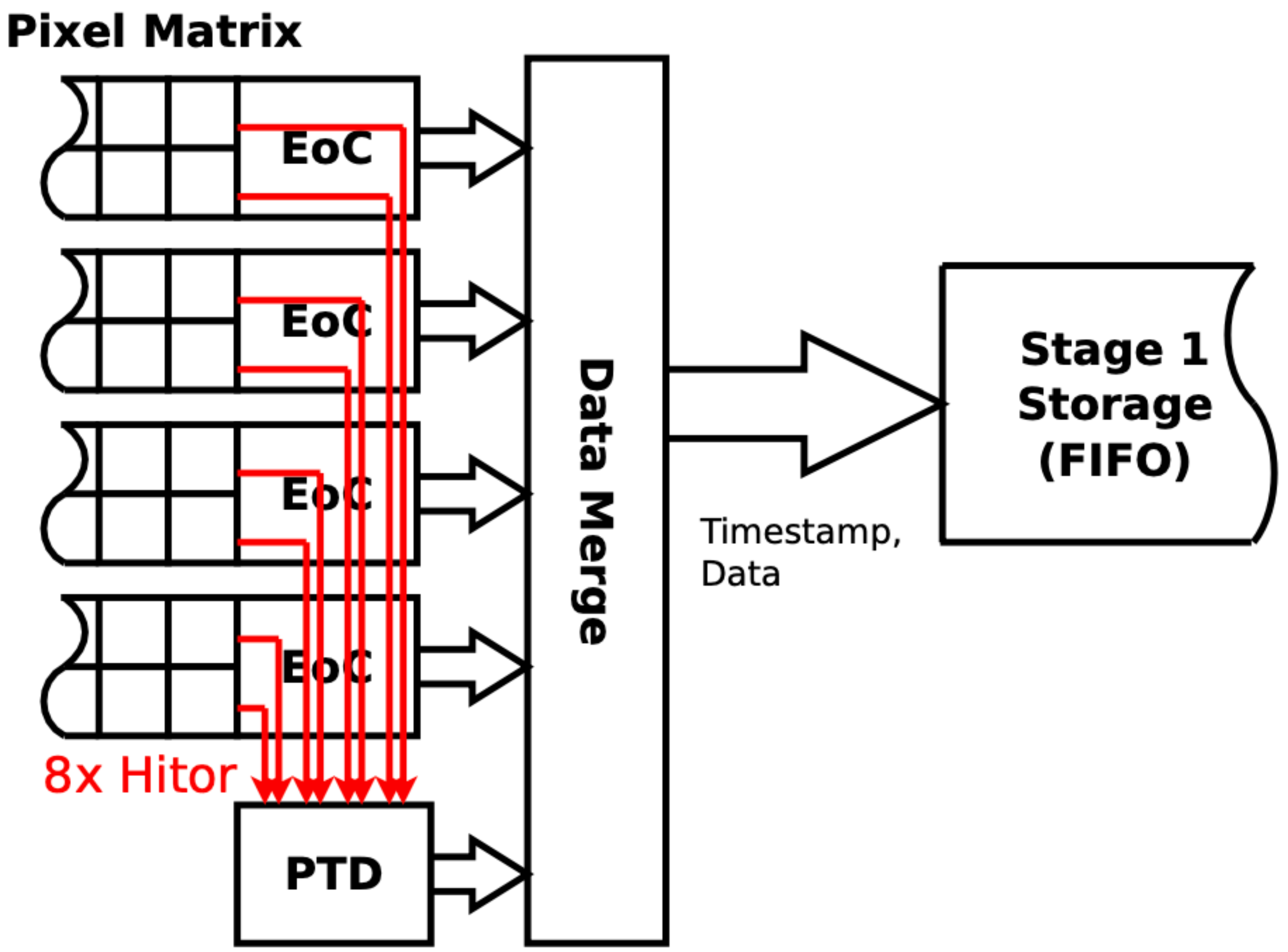
TRU: Simulation

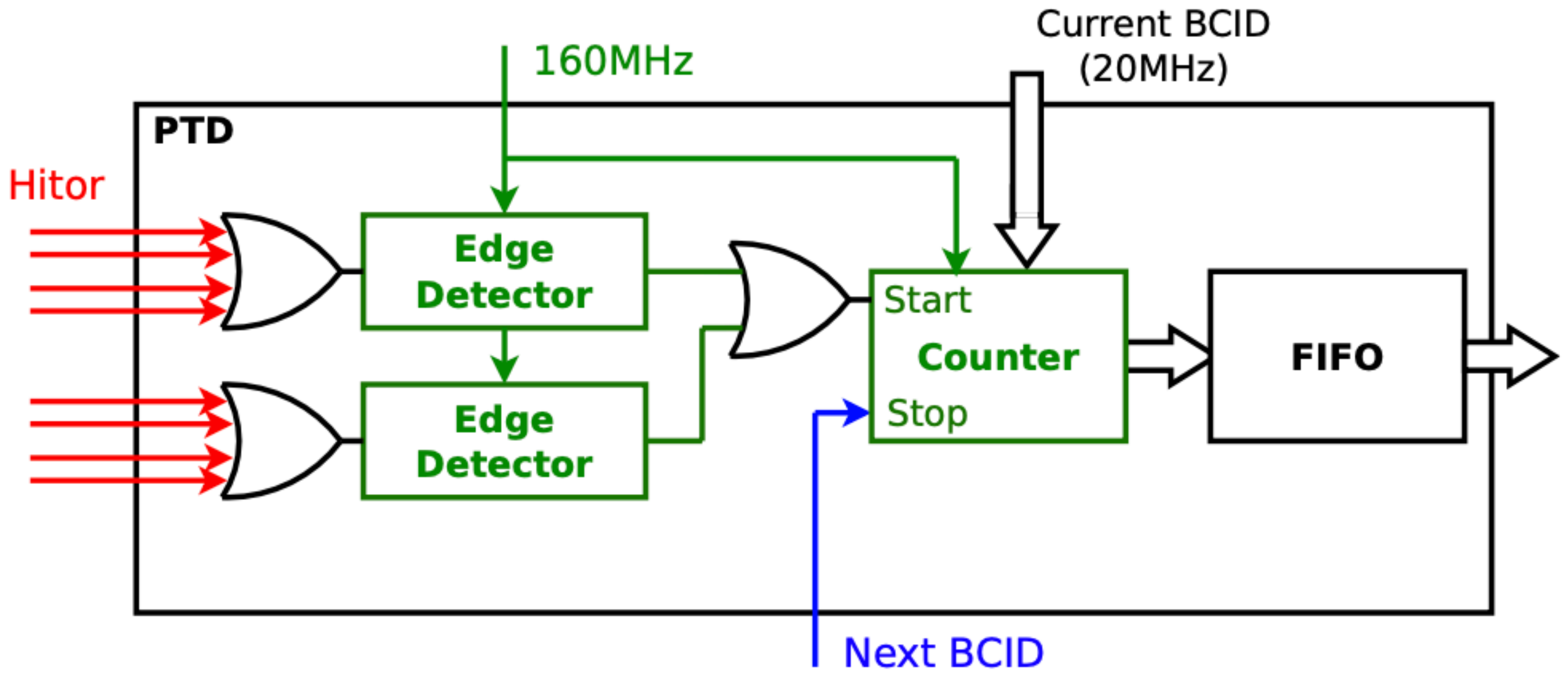




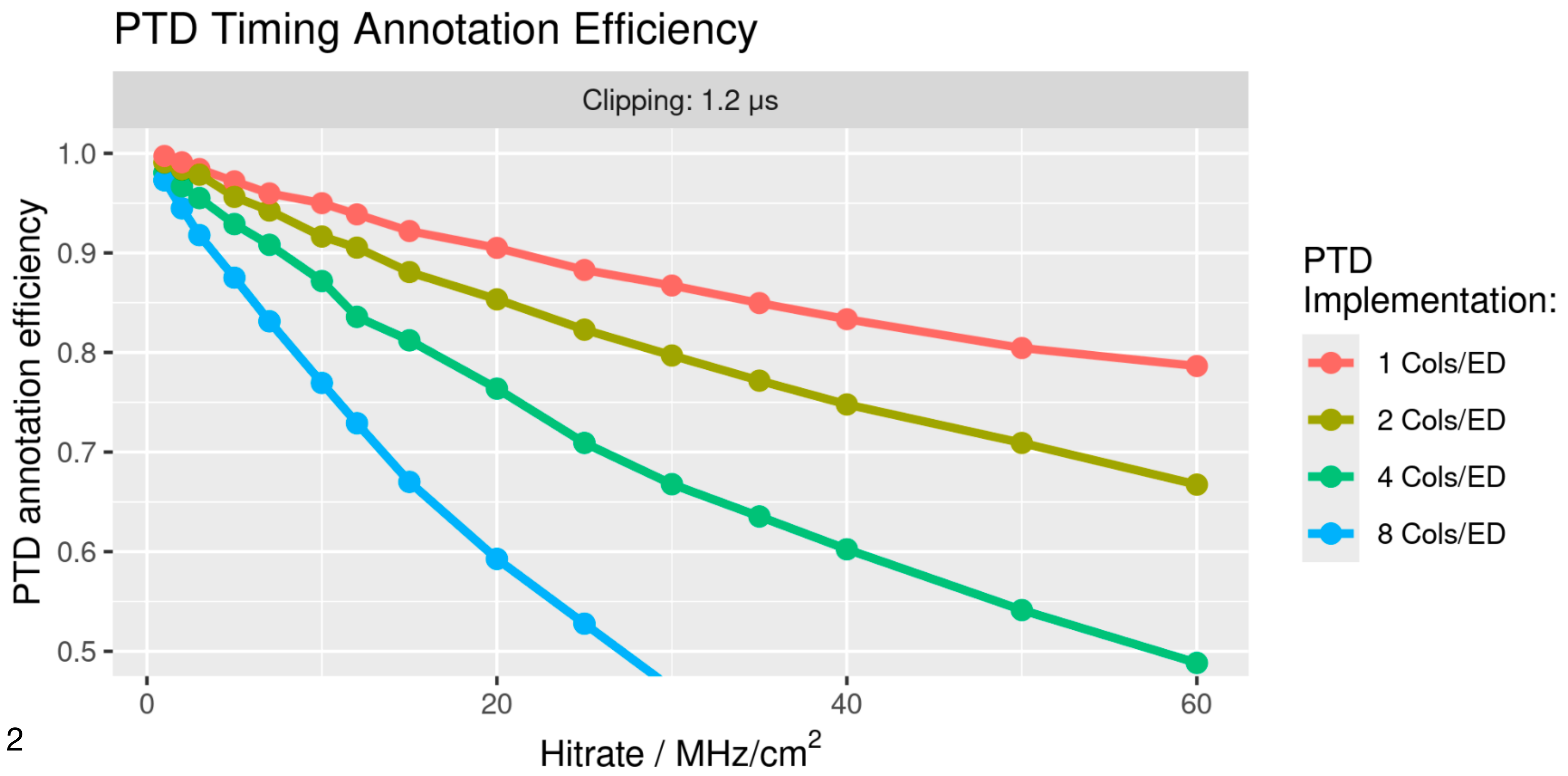
- Simulation includes: clustering & charge/ToT conversion
- Calibrated with TJ-Monopix2 results
- Power 10% above budget for 120 MHz/cm2 Clock frequency or analog bias current could be reduced?

Peripheral Time to Digital converter (PTD)



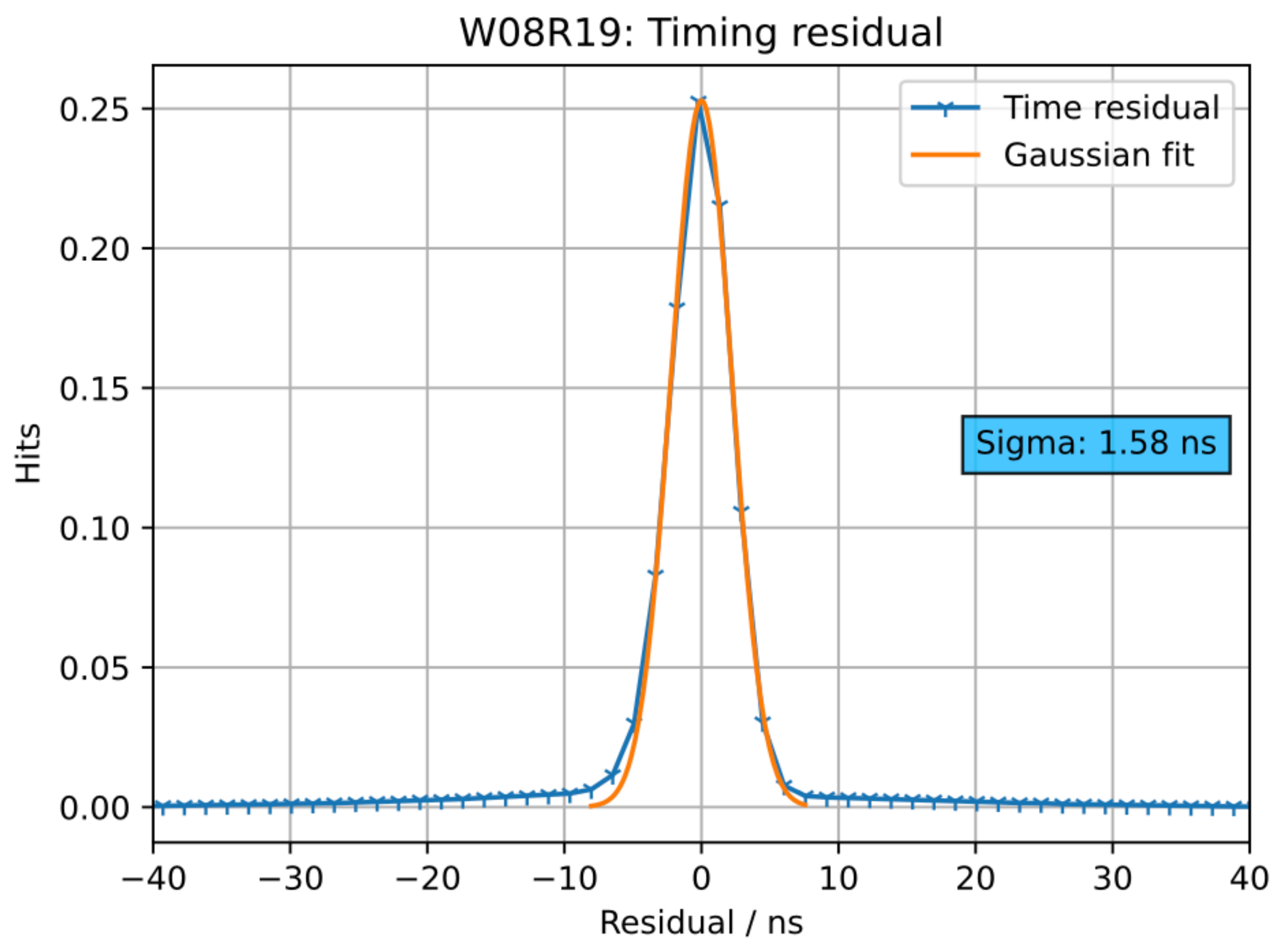


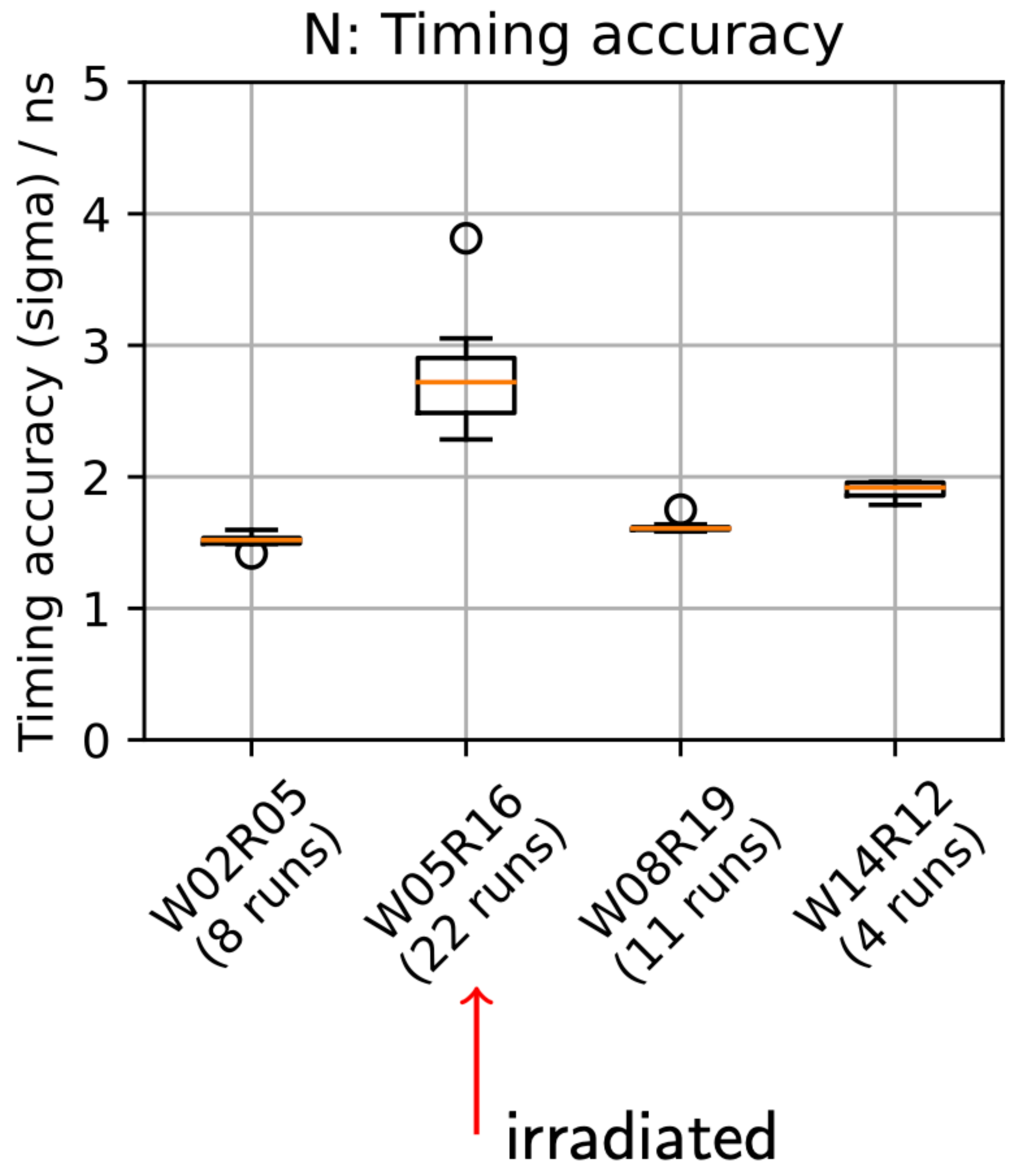
- Hitor: all comparator outputs of one column in an OR-chain (asynchronous)
  - sampling: 2.95 ns period (169.7 MHz DDR), precision timing better than timestamp (47.2 ns)
- Power hungry feature (+40 mW/cm^2 for 8 cols): disabled in iVTX
- Resolution limited by timewalk and PVT (process, voltage, temperature) variation
  - Calibration necessary



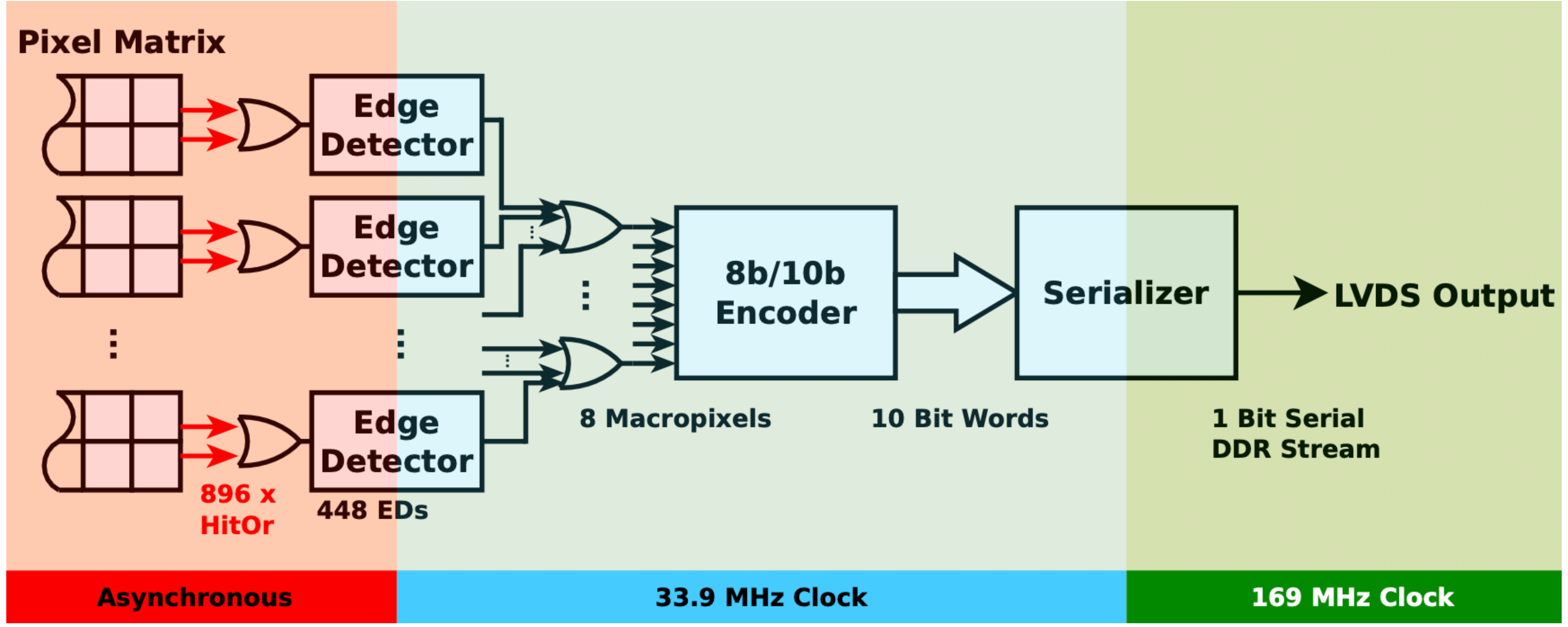
Hitor validation in testbeam

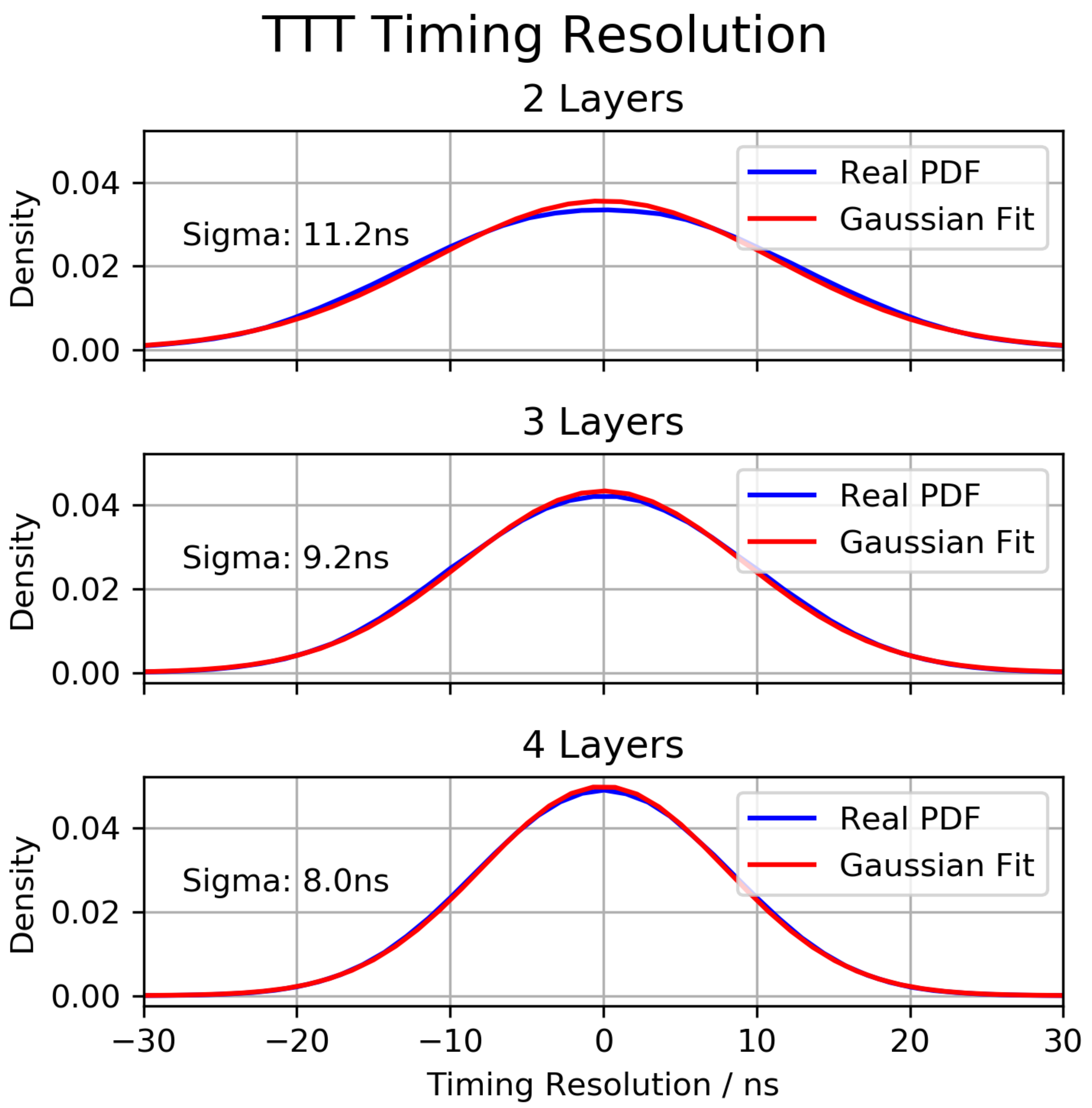
TJ-Monopix2 test, DESY, July 2023





Track Trigger Transmission (TTT)





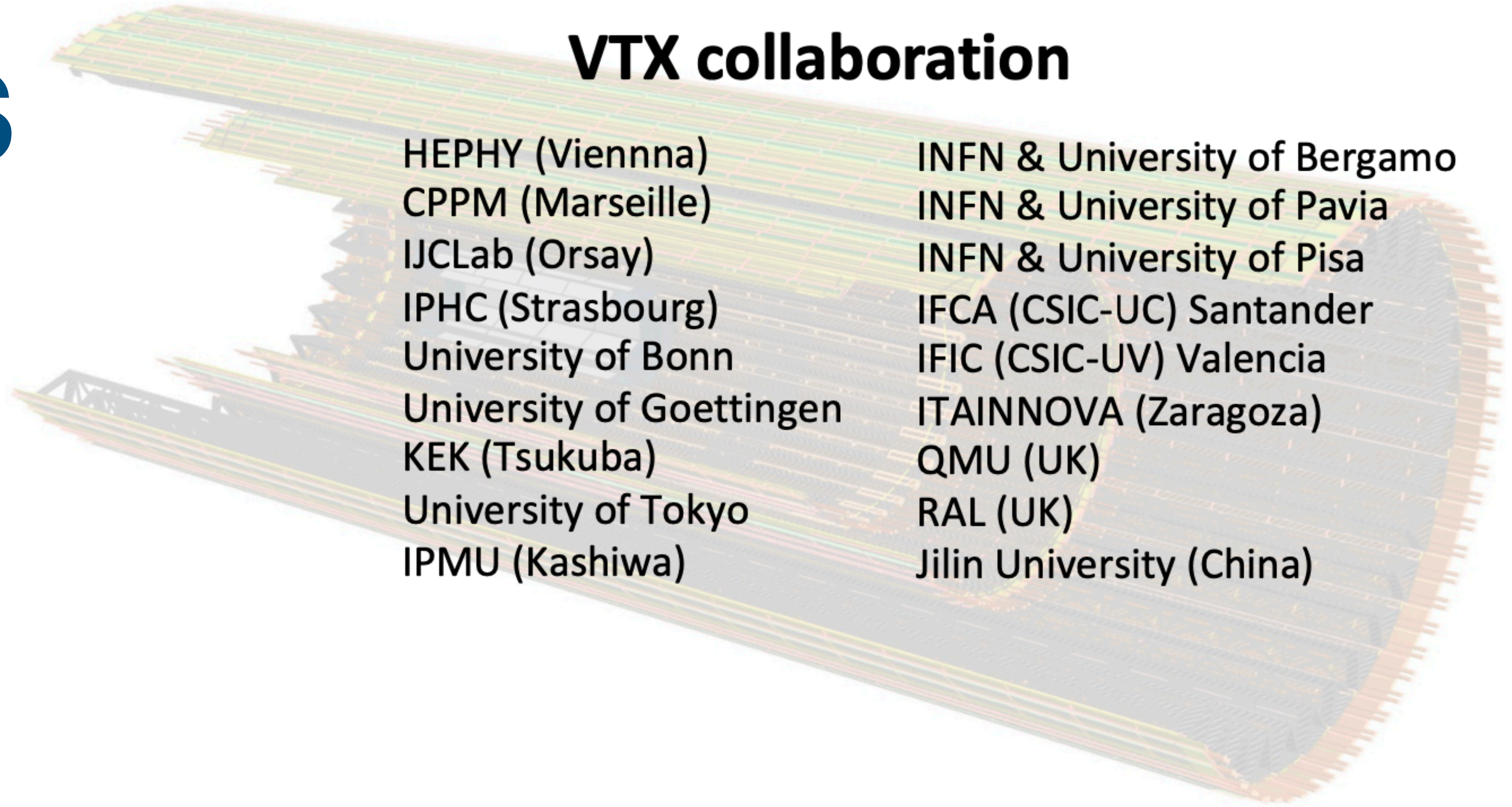
- Sensor is divided into macropixels (2 to 8 depending on wiring) that provide a fast signal (29.5 ns) through an independent data path (extra LVDS line)

OBELIX timeline

- OBELIX-1 design close to final
  - Submission planned for autumn 2024
  - Sensor delivery expected for early 2025
- OBELIX-2
  - Implementation of improvements
  - Submission early 2026 in time for a VTX delivery in ~2028

Summary and conclusions

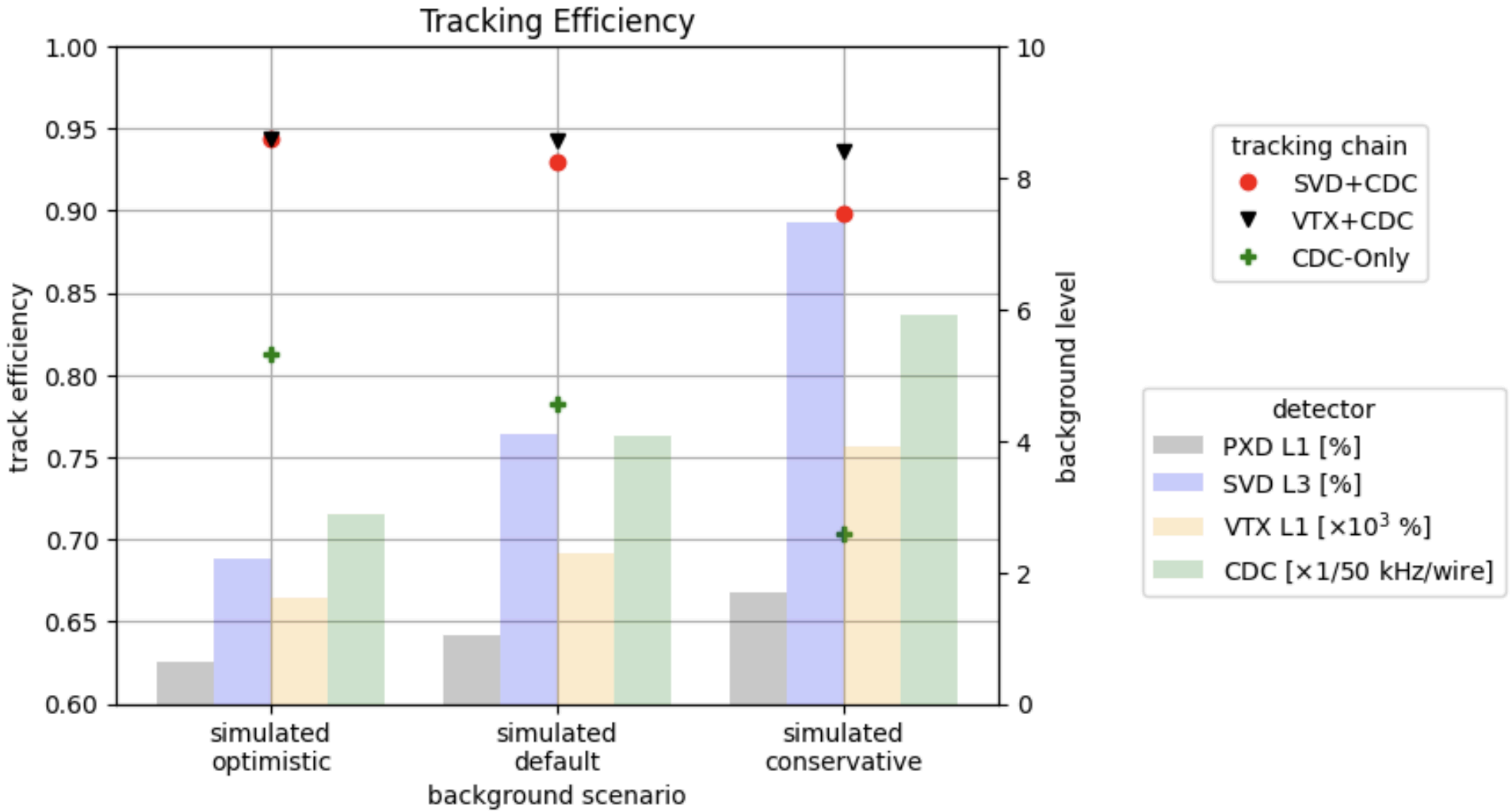
- OBELIX chip is based on TJ-Monopix2
- Additional features in OBELIX (all on-chip)
  - LDO voltage regulators
  - ADC and temperature sensors
  - Trigger logic, up to 10 μs latency at 120 MHz/cm2
  - Precision timing module
  - Fast transmission for VTX trigger
- Development and verification of the first iteration (OBELIX-1) is nearing completion



VTX collaboration

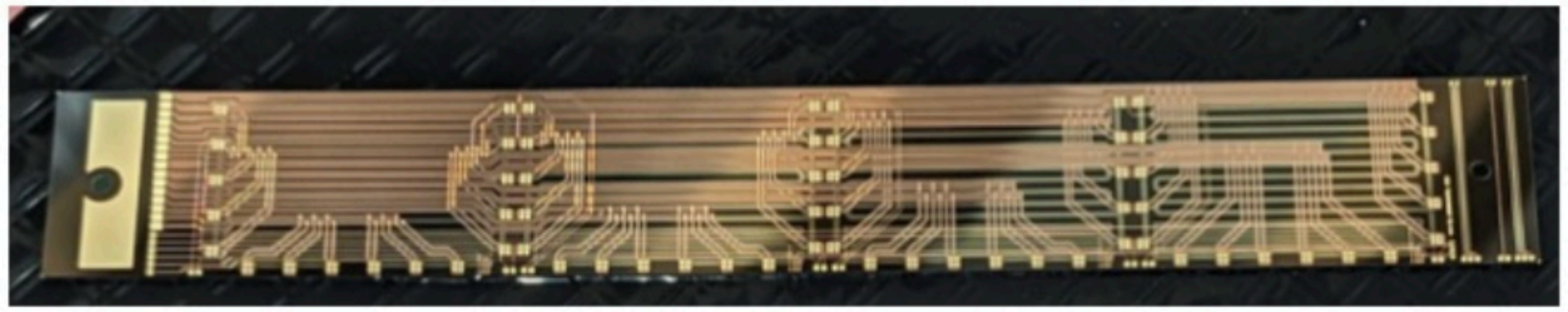
HEPHY (Viennna)
CPPM (Marseille)
IJCLab (Orsay)
IPHC (Strasbourg)
University of Bonn
University of Goettingen
KEK (Tsukuba)
University of Tokyo
IPMU (Kashiwa)
INFN & University of Bergamo
INFN & University of Pavia
INFN & University of Pisa
IFCA (CSIC-UC) Santander
IFIC (CSIC-UV) Valencia
ITAINNOVA (Zaragoza)
QMU (UK)
RAL (UK)
Jilin University (China)

Backup

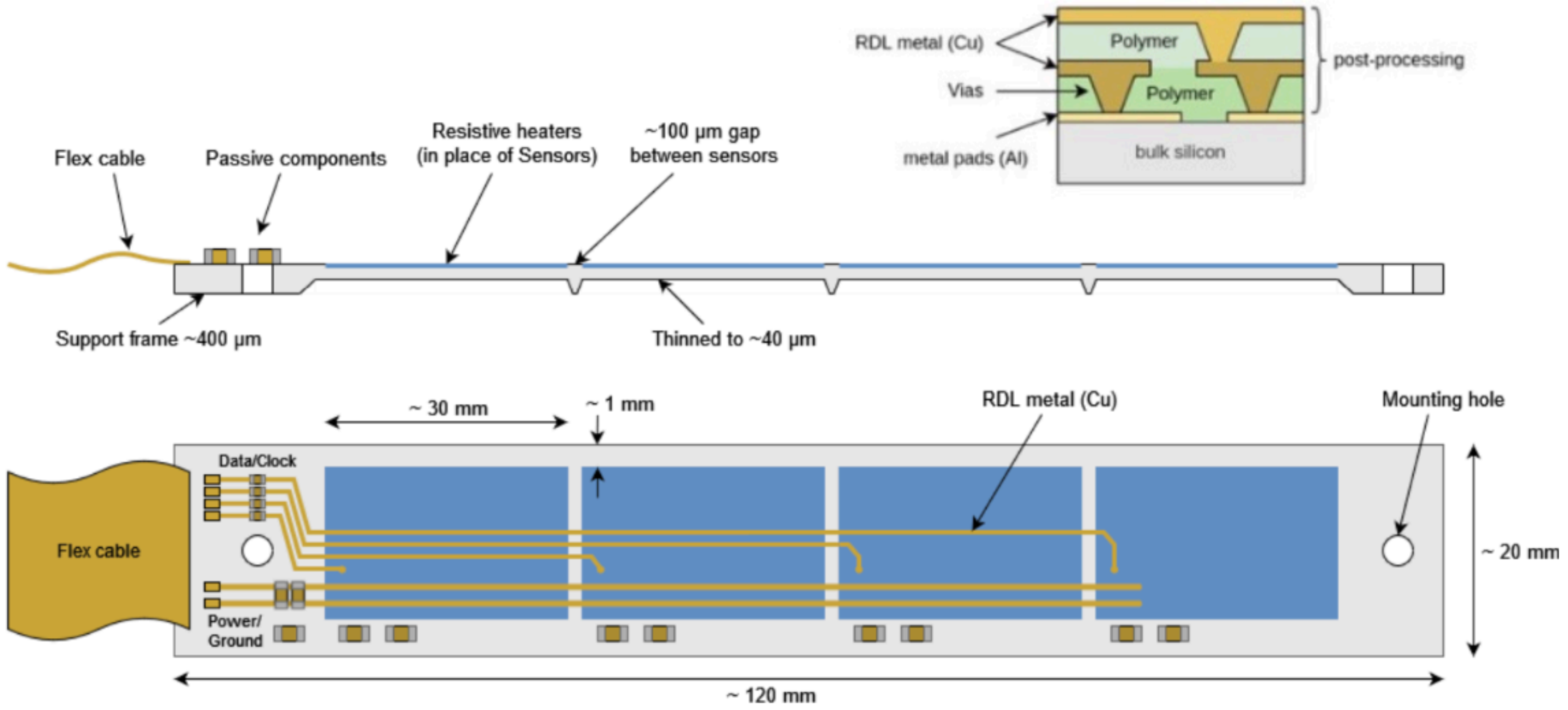

Tracking Efficiency
1.00
0.95
0.90
0.85
0.80
0.75
0.70
0.65
0.60
track efficiency
10
8
6
4
2
0
background level
simulated optimistic
simulated default
simulated conservative
background scenario
tracking chain
SVD+CDC
VTX+CDC
CDC-Only
detector
PXD L1 [%]
SVD L3 [%]
VTX L1 [×10³ %]
CDC [×1/50 kHz/wire]

iVTX

- All-silicon module < 0.2% X0
  - 4 contiguous OBELIX sensors diced as a block from the wafer, thinned to 50 um, except in some border area ~400 um thick, to ensure stiffness
  - Post-process redistribution layer for interconnection
- Prototypes:
  - First real-size ladder at IZM-Berlin with dummy Si & resistive heater to test cooling too

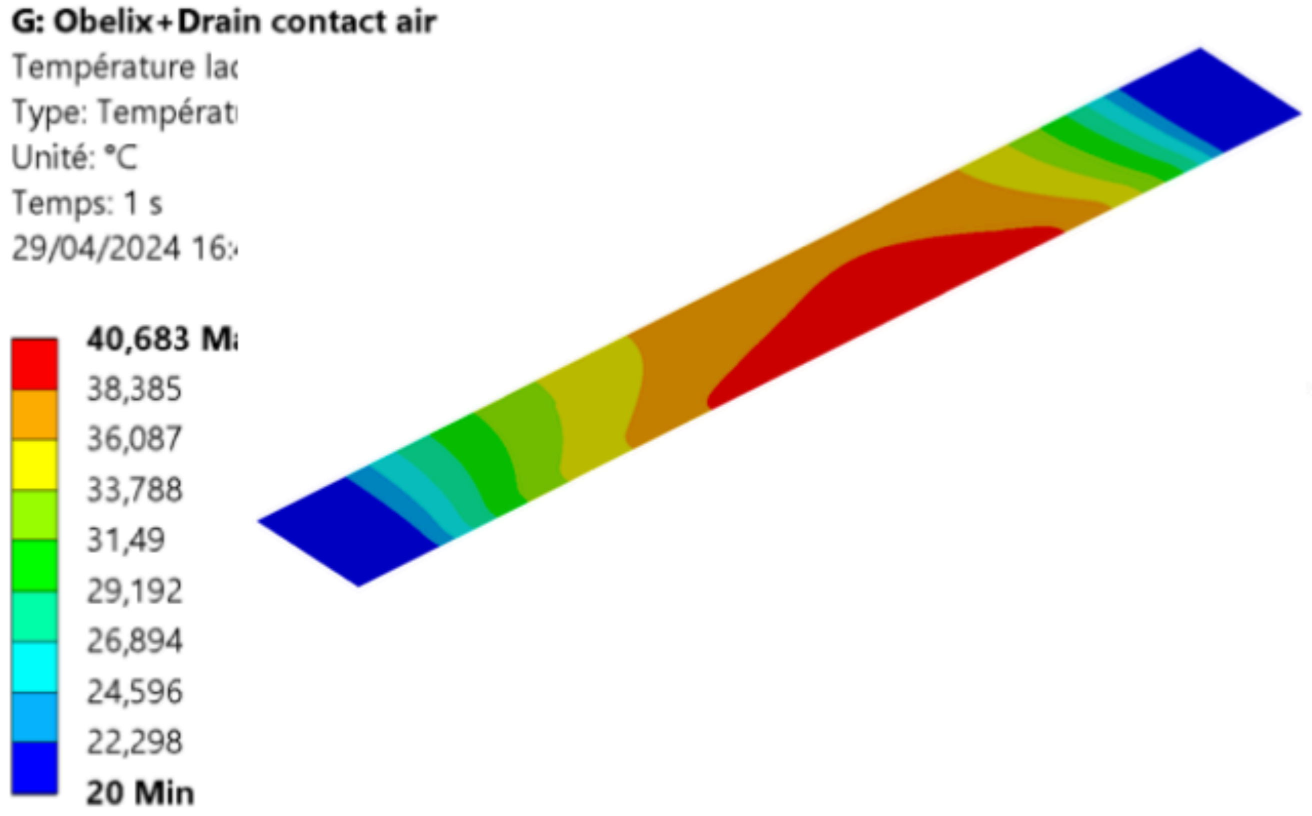


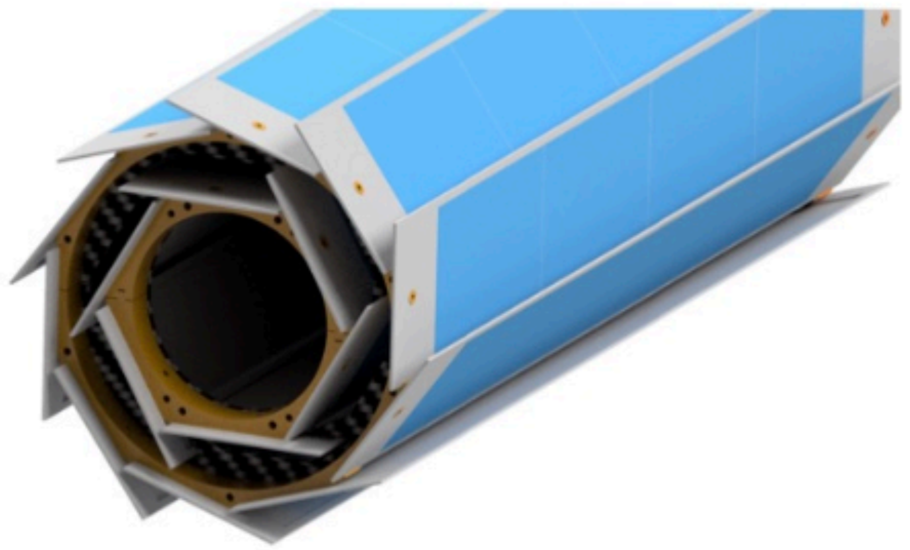
- Air cooling alone might be marginal
  - Non uniform Power: matrix 100 mW/cm^2, digital periphery ~500 mW/cm^2→ P_avg ~200 mW/cm^2
- Several options under evaluation



Preliminary: cooling simulation results

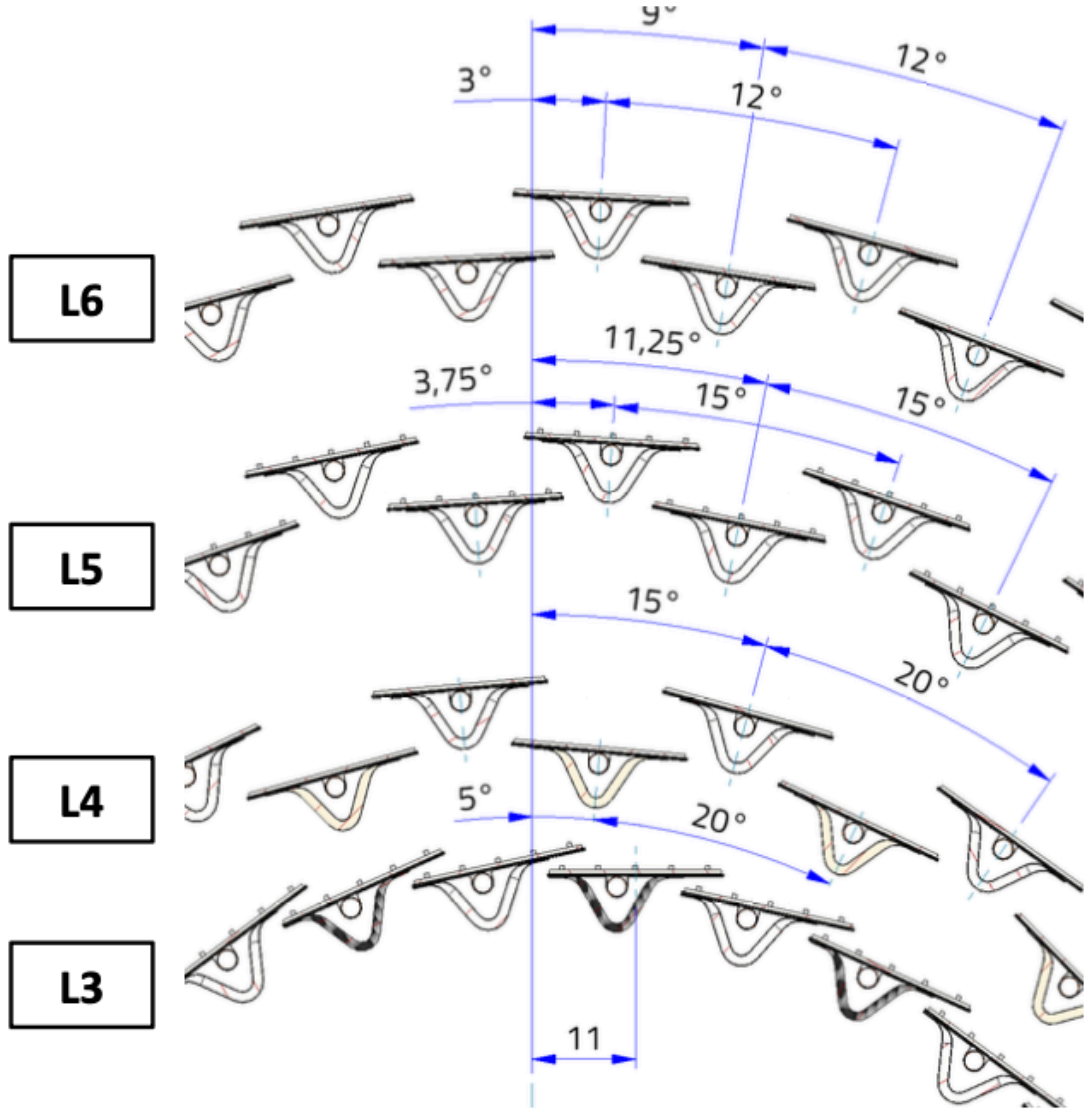
	Ladder only T max (°C)	Ladder only T range (°C)	Ladder + carbon plate T max (°C)	Ladder + carbon plate T range (°C)
Contact + air	44	22	41	18
Contact + water	66	41	34	12
Contact + air + water	39	17	30	9

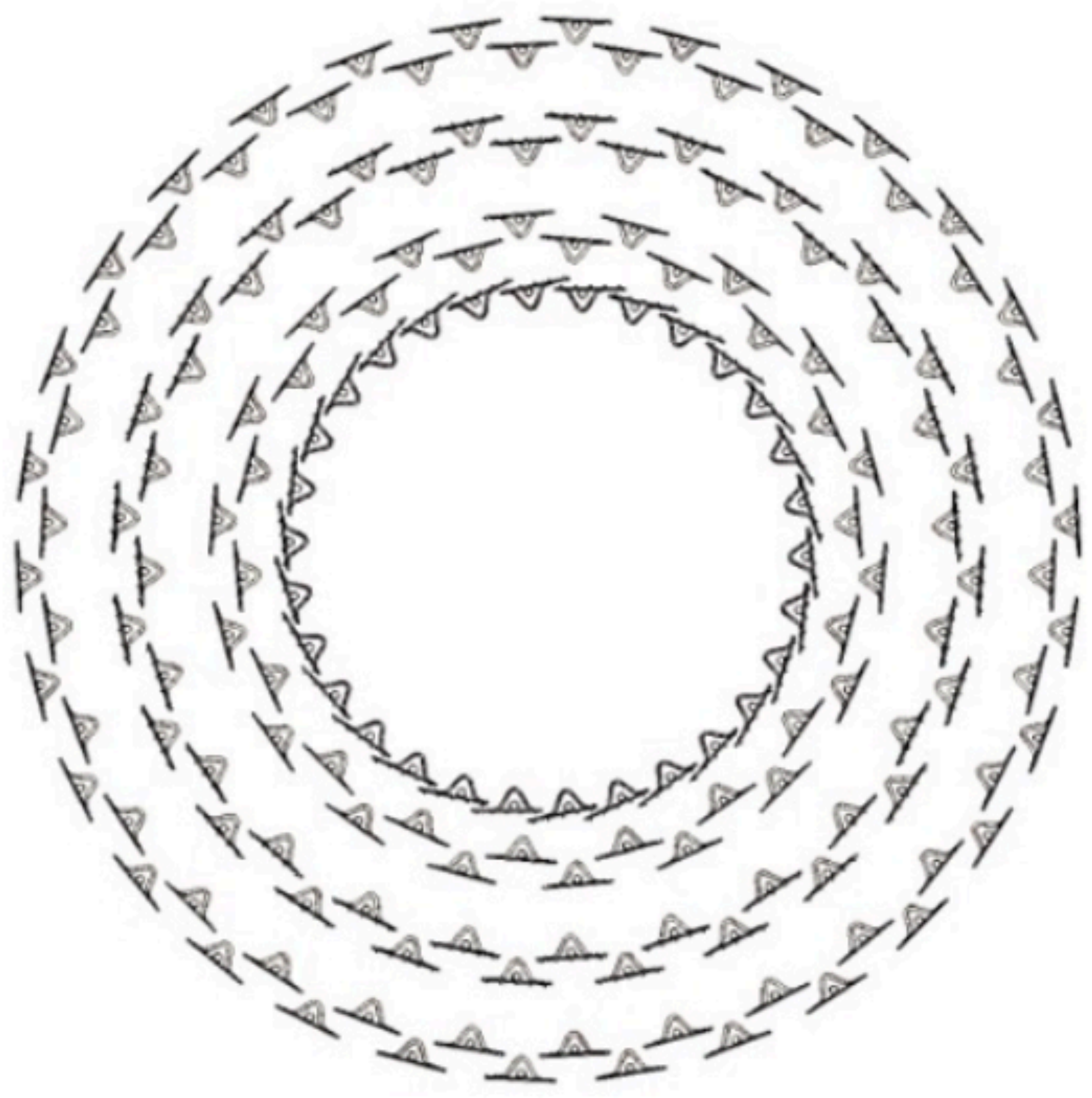




oVTX

- Ladder structure (ALICE ITS2-inspired):
  - CF support structure (Ω beam), cold-plate with pipes (2 or 1 pipe) with liquid cooling
  - Chip and Flex circuit for power & signal
- Prototypes:
  - Mechanical & thermal characterization done for the longer ladder ~70 cm (outermost layer)
- Mechanical design already advanced
  - now also exploring a 6 layers option





Modified 6 layers layout