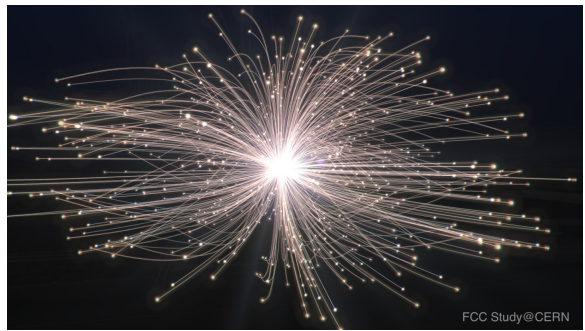
Optimisation of Silicon Tracking Systems

FCC Week 2024

Armin Ilg

University of Zürich

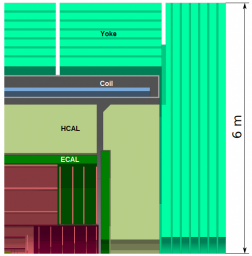
11.06.2024



University of Zurich[UZH]

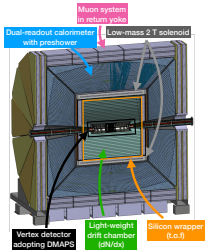
FUTURE CIRCULAR COLLIDER

FCC-ee detector *concepts*



CLD: CLIC-Like Detector [1, 2].

- ILC → CLIC → FCC-ee (→ μCol)
- **Si vertexing and tracking**
- Highly-granular ECAL and HCAL, CALICE-like
- Solenoid coil outside calorimeter system



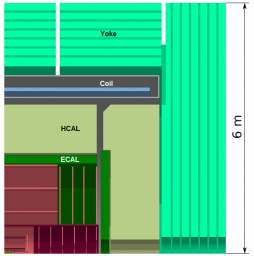
IDEA: Innovative Detector for e^+e^- Accelerators [3, 4].

- **Si vertexing**
- Drift chamber (down to 1.6% X/X0, d$N_{\text{ion.}}$/dx)
- **Si wrapper with timing**
- Dual-readout calorimeter with preshower
- Solenoid coil inside calorimeter system

ALLEGRO: A Lepton coLLider Experiment with highly GRanular calorimetry Read-Out (M. Aleksa).

- **Si vertexing** and drift chamber
- Highly granular noble liquid ECAL, Pb/W+LAr or W+LKr
- ECAL and solenoid coil in same cryostat
- CALICE-like or TileCal-like HCAL

FCC-ee detector *concepts* + variations (RICH, crystal ECAL, ...)



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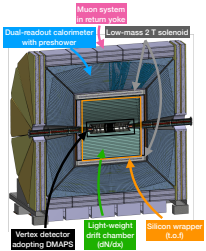

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FCC-ee vertex detector layouts

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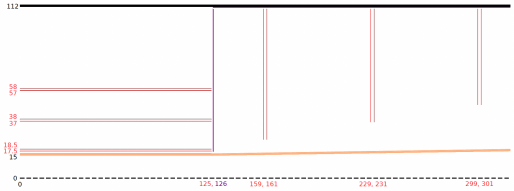
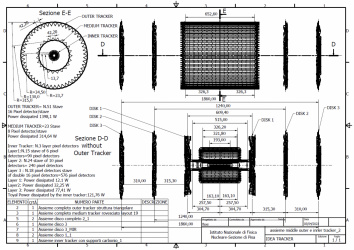
CLD → Rescaled CLICDet vertex detector



arXiv:1911.12230

- $r_{\text{min}} = 13\,\text{mm}$
- Three double-layer barrel layers and disks, 0.6–0.7%X/X_0 per double layer
- No engineering studies since CLICDet developments
- So specific sensor chosen, assume 3 μm single-point resolution

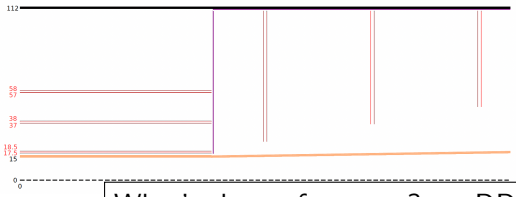
IDEA → Original FCC-ee vertex layout



- $r_{\text{min}} = 13.7\,\text{mm}$
- Three inner barrel single-layers (0.3%X/X_0), two outer barrel layers and three disks
- Engineered design (F. Palla), integrated into MDI (INFN-LNF)
- Assume ARCADIA (inner barrel) and ALTASPix3 (outer barrel, disks) sensors

FCC-ee vertex detector layouts

CLD → Rescaled CLICDet vertex detector



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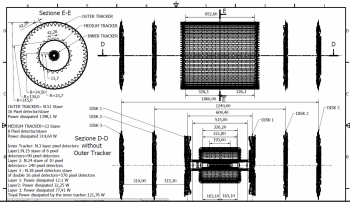

What's the performance? → DD4hep/Key4hep full simulation!

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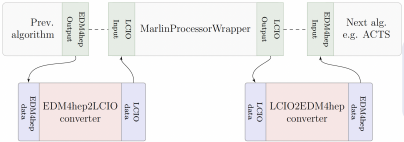
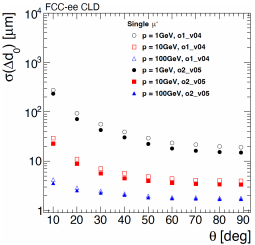
CLD vertex and tracker full simulation

Detector model in k4geo

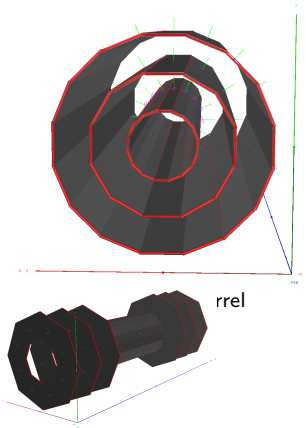
- Linear collider reconstruction (iLCSoft/CLICPerformance)
- Can generate EDM4hep output using k4MarlinWrapper



Access to all LC tools: PandoraPFA, LCFI+, etc.



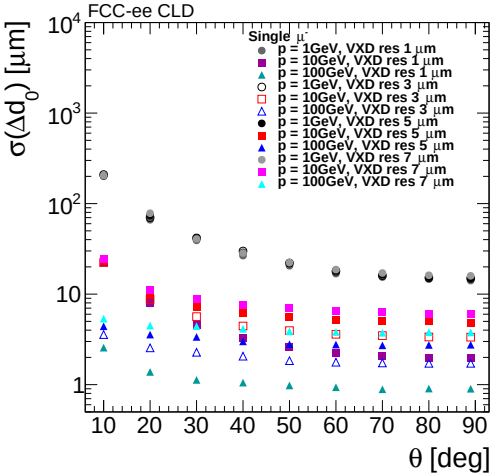
- CLD_o2_v05: Small, AlBeMet beam pipe
- G. Sadowski, 7th FCC Physics Workshop



CLD endcap and vertex barrel

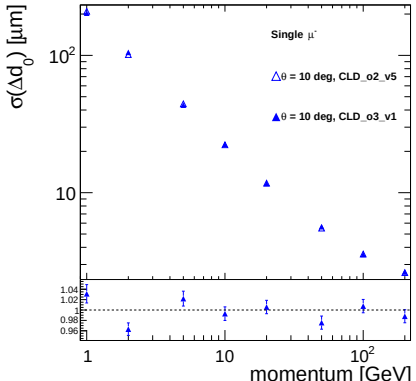
Using CLD reconstruction and k4DetPerformance for plotting!

Impact of sensor spatial resolution



ARC adapted CLD (CLD_03_v01 design)

- Reduced outer tracker radius and length
- 15–20% degradation in p_T resolution



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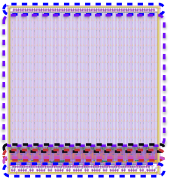
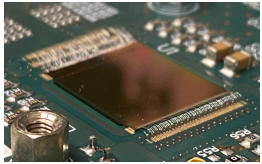
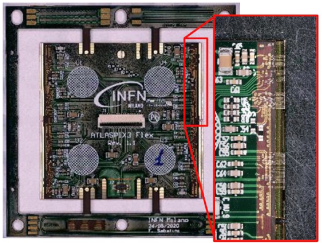
Depleted Monolithic Active Pixel Detectors

- **Inner Vertex (inspired to ARCADIA):**
  - Lfoundry 110 nm process
  - *50 µm thick, 25 µm x 25 µm*
  - Module dimensions: $8.4{\times}32\ mm^2$
  - Power density $50\ mW/cm^2$ (core $30\ mW/cm^2$)
  - **Current at 100 MHz/cm²**
- **Outer Vertex and disks (inspired to ATLASPIX3)**
  - TSI 180 nm process
  - *50 µm thick (50 µm x 150 µm)*
  - Module dimensions: $42.2{\times}40.6\ mm^2$
  - Power density: assume $100\ mW/cm^2$
  - **Up to 1.28 Gb/s downlink**



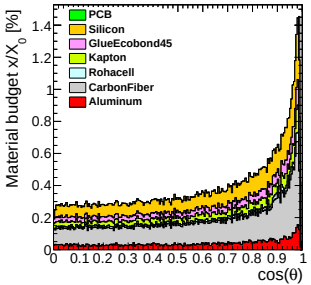


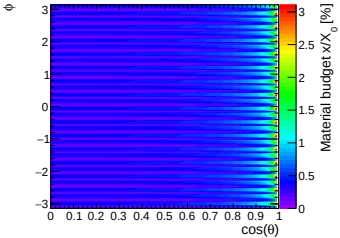


F. Palla, 2nd FCC US workshop at MIT

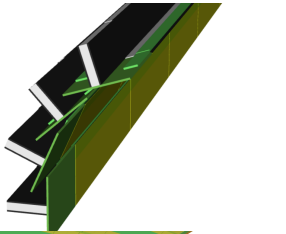
Vertex inner barrel

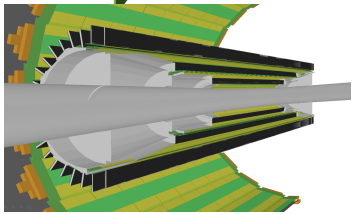
- $r_{\text{min}} = 13.7\,\text{mm}$, 2 mm to beam pipe (can we go closer?)
- Correct material stack, flexes, end-of-stave hybrid, insensitive sensor areas (2 mm)
- Proxy volume for stave holding structure
- Need to add service cones
- Material budget in line with 0.3% per layer at $\cos(\theta) = 0$ (CDR assumption)





First layer

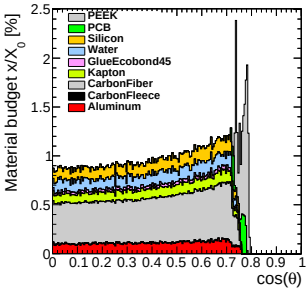


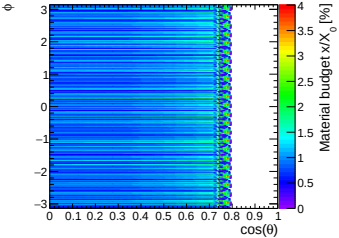


Vertex inner barrel, with support

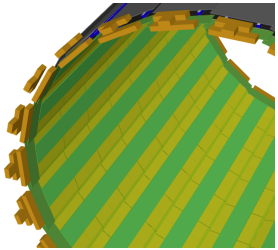
Vertex outer barrel

- Correct material stack, correct description of ATLASPix3 insensitive peripheries
- Proxy volumes for truss structure and cooling pipes
- Proxy volume for end-of-stave holder (orange, material budget contribution optimised with F. Palla)
  - → Still significant contribution

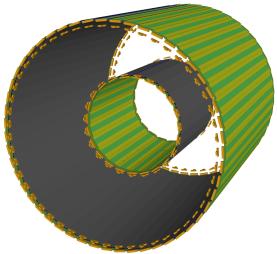




Complete outer barrel



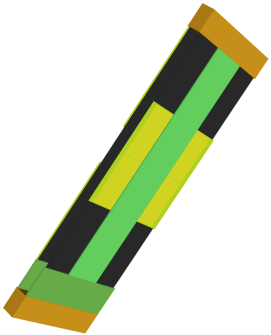
Middle tracker



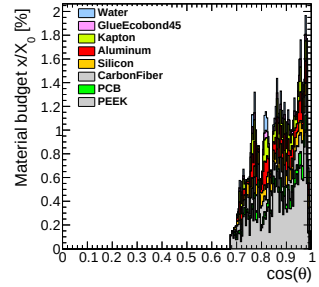
Complete vertex outer barrel system

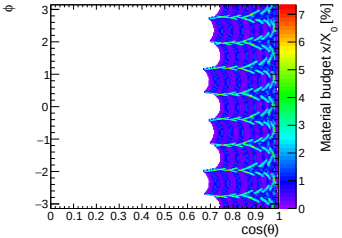
Vertex disks

- Correct placement of all modules in r and z
- Missing vertex disk global support
- Very uneven x/X_0 distribution

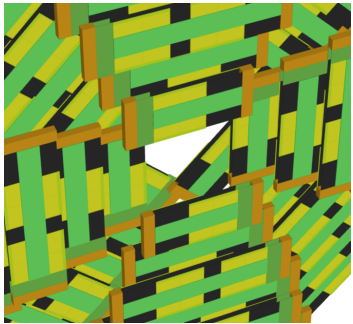


One short stave

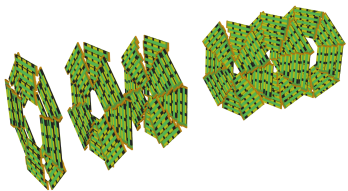




Disk 0

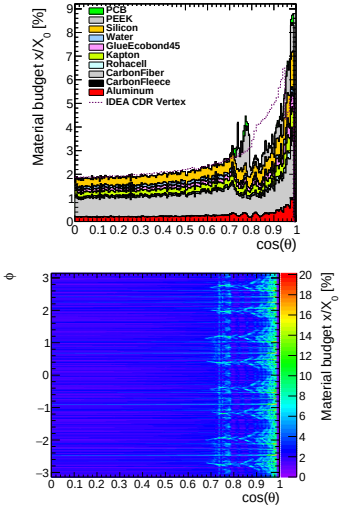


Disk 0 zoom-in



Complete vertex disks system

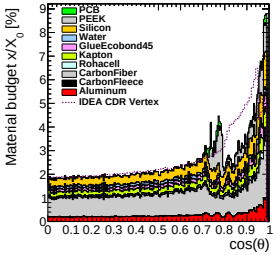
Complete system

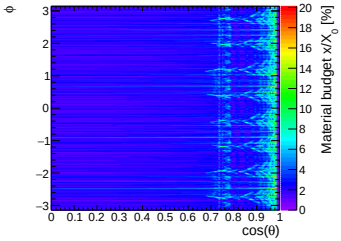


Complete vertex system

- Material budget comparable with CDR estimate
- Will make the updated version available soon
- Plan to include last missing volumes using DDCAD
- Look at all material budget evaluations as a lower limit, there's always gonna be more added! (e.g off-detector cabling)
- No drift chamber tracking available yet → instead use CLD and iLCSoft reconstruction

Complete system





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- No drift chamber tracking available yet → instead use CLD and iLCSoft reconstruction
  - Frankenstein approach: Remove CLD vertex detector (and a couple of Inner Tracker layers and disks) and instead insert IDEA vertex, run CLD reconstruction and k4DetPerformance for plotting!
  - Let's have a look!

Necessary changes

- Removing first Inner Tracker barrel layer ($r = 127\,\text{mm}$)
- Removing first and second Inner Tracker disks ($r = 79.5$ and $123.5\,\text{mm}$)
- Increase conformal tracking max. distance (CT_MAX_DIST)
- *MinClustersOnTrack* from 4 to 3 in conformal tracking in vertex barrel and disks

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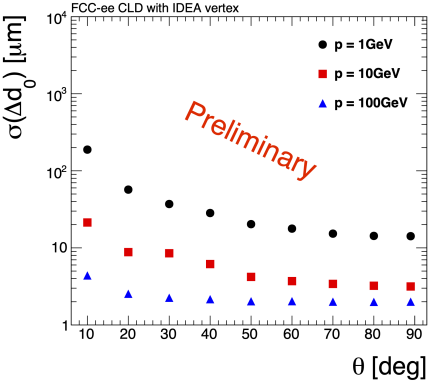
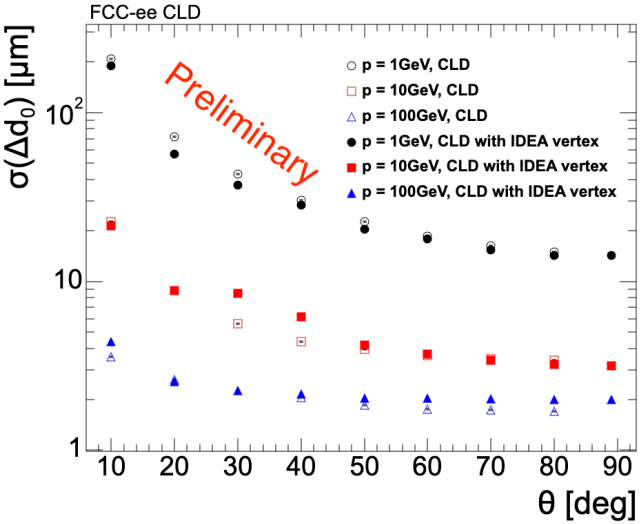


Nota bene

- No silicon wrapper
- Assume spatial resolution of $3\,\mu\text{m}$ for vertex inner barrel (same as CLD), and $14\,\mu\text{m} \times 43\,\mu\text{m}$ for outer barrel and disks (CLD: vertex endcap: $3\,\mu\text{m}$, inner tracker endcap: $5\,\mu\text{m}$ or $7 \times 90\,\mu\text{m}$)

Comparison between CLD and IDEA vertex



IDEA vertex better at lower momenta, CLD vertex better at high momenta

→ Makes sense as CLD uses double layers (with double the material budget)

Notes:

- Using CLD_o2_v05
- $\theta = 89°$ points missing for CLD
- Non-optimised reconstruction for IDEA vertex!

Other, preliminary, results in backup

Sensor-only vertex detector

DMAPS in 65 nm TPSCo process

- More logic per cm^2
- Lower power consumption $\rightarrow$ Air cooling
- Enables 12" wafers $\rightarrow$ Wafer-scale bent sensors!

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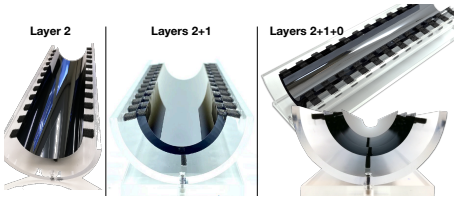
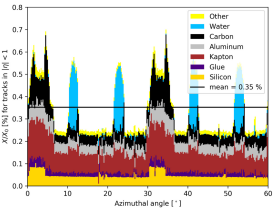
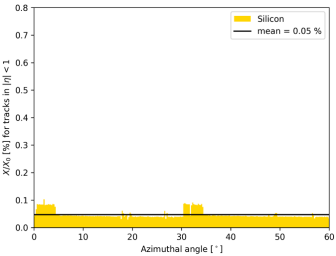
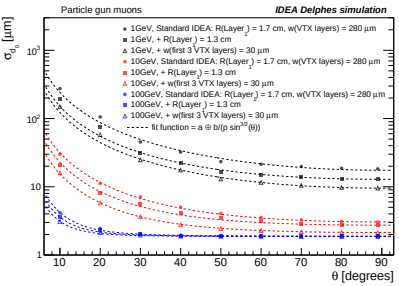


Layer assembly concept for ALICE ITS3 [5]





Material budget in ALICE ITS2 (left, [6]) and silicon only (M. Mager)



L. Freitag (BSc. thesis [7])

University of Zurich[UZH]

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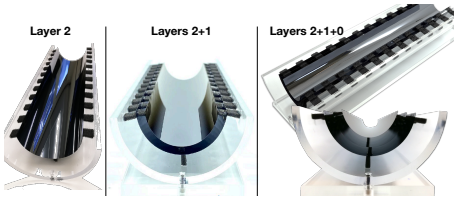
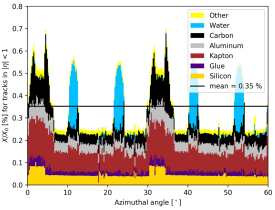
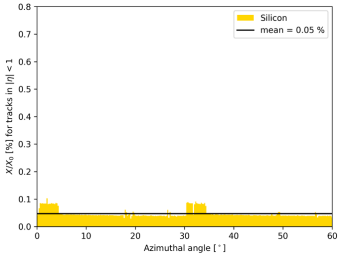
- Lower power consumption → Air cooling
- Enables 12" wafers → Wafer-scale bent sensors!

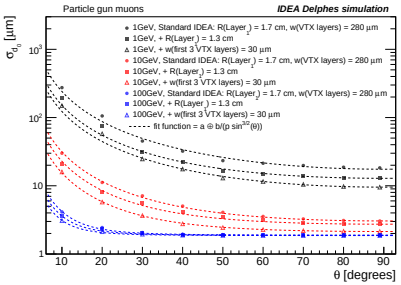


Layer assembly concept for ALICE ITS3 [5]





Material budget in ALICE ITS2 (left, [6]) and silicon only (M. Mager)



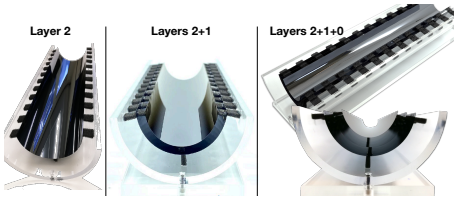
L. Freitag (BSc. thesis [7])

See also F. Palla at 2nd FCC US workshop and G. Contin's talk.

Sensor-only vertex detector

DMAPS in 65 nm TPSCo process

- More logic per cm^2
- Lower power consumption → Air cooling
- Enables 12" wafers → Wafer-scale bent sensors!



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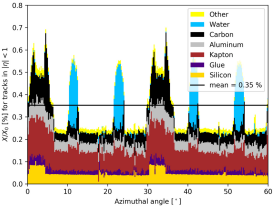

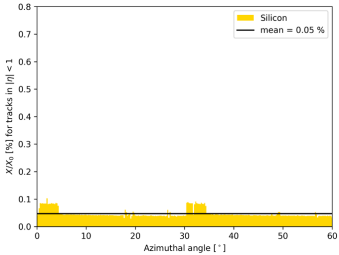

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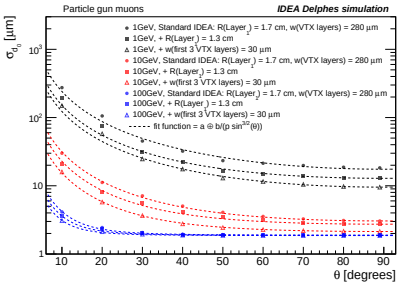


L. Freitag (BSc. thesis [7])

See also F. Palla at 2nd FCC US workshop and G. Contin's talk. How adapt to FCC-ee?

University of Zurich[UZH]

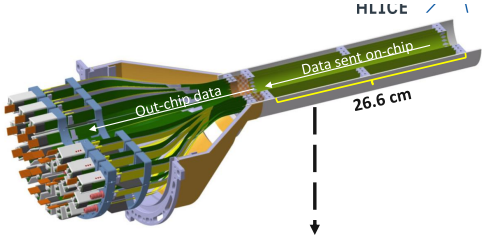
ITS3

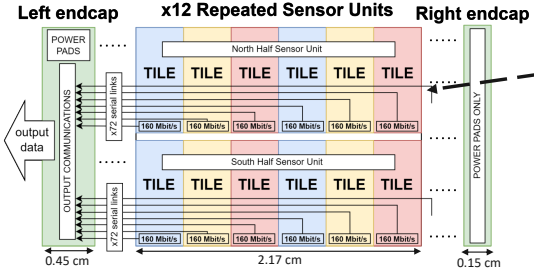
- Wafer-scale Monolithic Active Pixel Sensors (**MAPS**)
- Cylindrical sensors of radii 18/24/30 mm

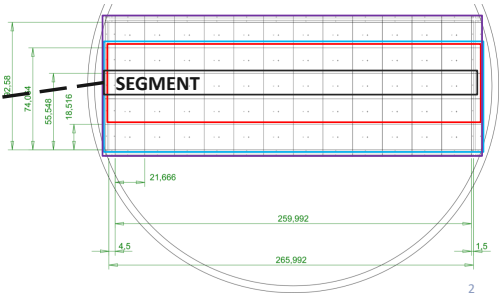
Architecture requirements (**Stitching**)

- Dies divided into 3,4 or 5 **Segments**
  - **2 endcaps** on the edges
  - **12 Repeated Sensor Units** (RSU)
    - 12 *tiles per RSU*

Data transfer on-chip to the left edge (26.6 cm)



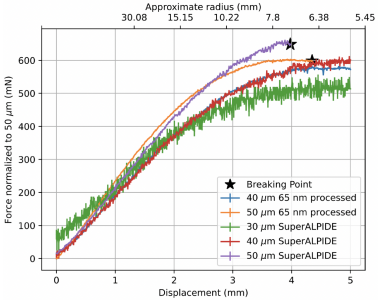




M. Rodriguez @ TWEPP 2023

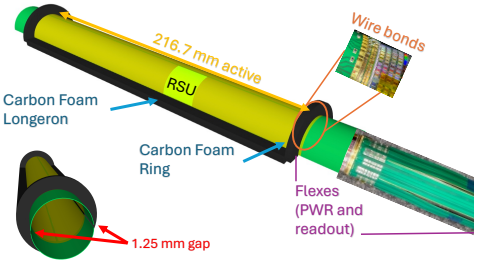
Differences between ALICE ITS3 and FCC-ee

- First layer at smaller radius, from 18 to 13.7 mm
  - → Mechanically okay, electrically to be demonstrated
  - → First layer to use just two segments
- ITS3 cables only to one side → We want to measure forward-backward asymmetries extremely precisely
  - → Read and power from both sides where possible
- Need forward coverage down to $\theta \approx 140$ mrad
  - → Multiple wafer-scale sensors in a row at larger radii
  - → Ensure flexes, cables, etc. are not in front of lumical
- Hermeticity?
  - → Cannot overlap like with staves (wire bonds from sensor end to flex)
  - → Evaluate impact of only $\sim 95\%$ coverage per layer (RSU periphery, gap between sensors)
  - → Increase number of layers from 3 to 4 to ensure at least three hits

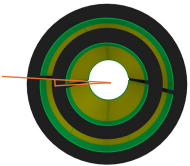


Ultra-light vertex concept: Layer 1 and 2

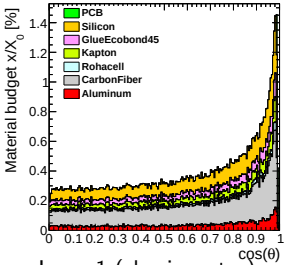
- Layer 1: 10 RSUs long $\rightarrow \theta \geq 125\,\text{mrad}$
- Layer 2: 12 RSUs (max!) $\rightarrow \theta \geq 155\,\text{mrad}$
- Gap of 1.25 mm between half-barrels, layer 2 rotated in ϕ to avoid overlap with layer 1
- Readout and power from both sides
- 50 μm of Si + 16 μm of Si-equivalent (metal layer connecting RSUs) $\rightarrow 0.075\% X/X_0$ at $cos(\theta) = 0$. Factor 4 improvement!



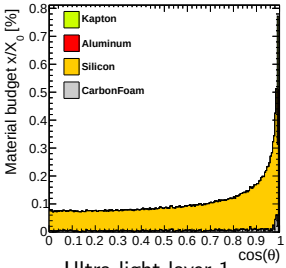
Layer 1 layout



Layer 1+2



Layer 1 (classic vertex)



Ultra-light layer 1

Ultra-light vertex detector concept: Layer 3 and 4

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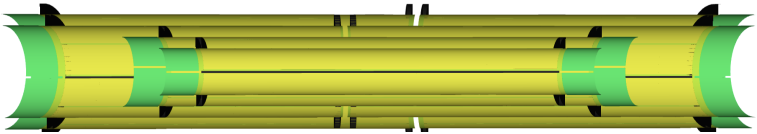
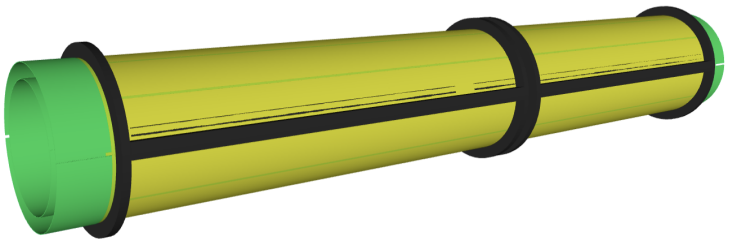
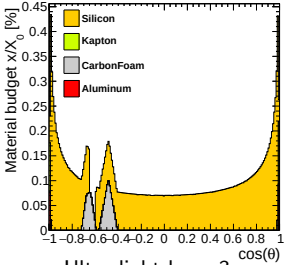
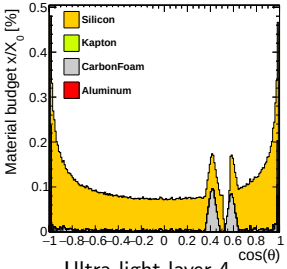
- Two sensors per side, readout only on sides, power on sides and center (power wire)
- Asymmetric design: 8 (10) RSUs on +z (-z) side for layer 3, inverted for layer 4, to cover gap at $z = 0$





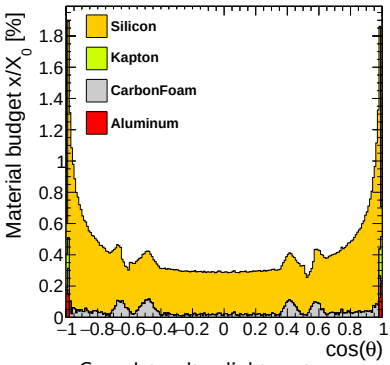


Ultra-light layer 3

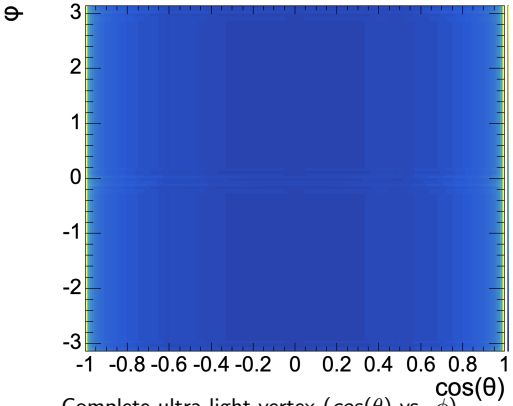


Ultra-light layer 4

Ultra-light vertex concept: Discussion



Complete ultra-light vertex



Complete ultra-light vertex ($cos(\theta)$ vs. ϕ)

- Same material budget as one layer (!) of normal IDEA vertex, more uniformly in ϕ
- Compromise hermeticity (or radius of first hit) with reduced material budget
- Need to add new sensitive surface to DD4hep (cylinder segment) to estimate vertexing performance using CLD reconstruction

IDEA silicon wrapper: Reminder

A last hurrah of the tracking system before Coulomb scattering takes over

- Momentum resolution thanks to long lever arm
- Extend tracker coverage
- Precise and stable ruler for acceptance definition

Possible technologies:

- DMAPS
- LGADs
- Microstrips
- ...

Needs to be added to DD4hep detector description as well!

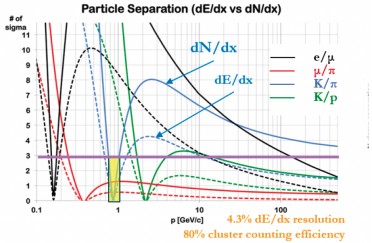
Barrel

Layer	R [mm]	L [mm]	Si eq. thick. [µm]	X0[%]	Pixel size [mm²]	area [cm²]
1	2040	±2400	450	0.5	0.05×100	616K
2	2060	±2400	450	0.5	0.05×100	620K

Endcap

Disk	R^{in} [mm]	R^{out} [mm]	z [mm]	Si eq. thick. [µm]	X0[%]	Pixel size [mm²]
1	350	2020	±2300	450	0.5	0.05×100
2	354	2020	±2320	450	0.5	0.05×100

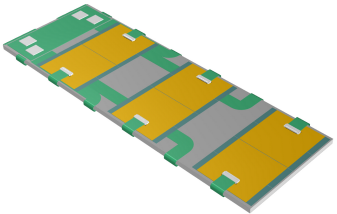
(fcc-ee-detector-full-sim.docs.cern.ch)



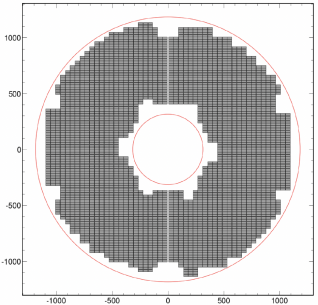
Slide following A. Andreazza FCC Week 2021

IDEA silicon wrapper: What was assumed so far

- Assume total of $\approx 1\% X/X_0$ in barrel and disks
- Hermeticity
  - Decided to increase disk r_{out} from 2020 to 2040 mm
  - Two barrel layers and two disks, to have at least one silicon hit, but most of the cases we have two silicon hits
- Total area: $\simeq 30\,\text{m}^2$ per barrel layer, $\simeq 13\,\text{m}^2$ per disk $\rightarrow$ $112\,\text{m}^2$ to cover
- Sensor thickness: $50\,\mu$m, resolutions: pitch $0.05 \times 1\,\text{mm}^2$ and 40 ps per hit, don't care about specific sensor technology
  - Assume ATLASPix3-sized modules ($42.2 \times 40.6\,\text{mm}^2$) to construct tiles with 6, 12 or 24 modules each
- Disk design inspired by CMS endcap timing layer



Tile proposed for CEPC [8, 9]



CMS ETL layout [10]

IDEA silicon wrapper: What is there

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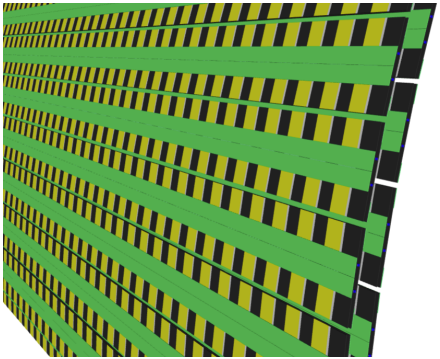
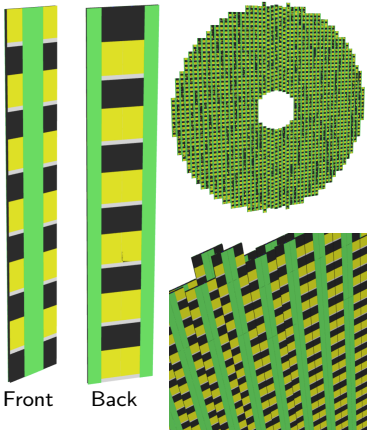
Barrel



Two layers to cover gaps

Disks



Front Back

Tiles of 6, 12 and 24 modules, total of 30432 modules, 51 m^2 of Si

Layer of 151 staves with $129 \cdot 2$ modules $\rightarrow$ total of 77916 modules, 132 mm^2 of Si

Since Annecy: Made construction faster, and added a simplified version (30 s to load geometry)

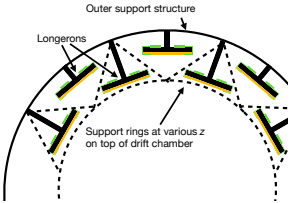
IDEA silicon wrapper: What is to do

General:

- use only one disk/barrel layer, with overlapping modules to ensure hermeticity $\rightarrow \geq 1$ hit
  - $\rightarrow$ Require 30 ps time resolution
- Optimise disk z positioning and/or barrel length
  - $\rightarrow$ No gap between disk and barrel (consider drift chamber services!)

Barrel: Fine resolution in ϕ for momentum measurement

- Long longerons attached to support rings on DC, using a ferris wheel-like structure
  - $\rightarrow$ Sensors facing IP, cables and cooling (pipes or micro-channel cooling plate) on top



Disks: Fine resolution in r for θ measurement

- D-shaped half-rings $\rightarrow$ Mounted as two separate components (disk cannot be one piece)
- Aim to mount onto sides of DC, but need to leave gap to guide DC cables out
  - $\rightarrow$ Use a stilt structure attached to drift chamber, onto which rings are attached

IDEAs:

- Aggregation of signal, opto-el. conversion and serial-powering on tile/along longeron
- Wireless data transmission from barrel centre and disk centre outwards?

Conclusions

CLD vertex and tracker

- Adaptions to accomodate ARC leave IP resolution unchanged, 15–20% worse p_T resolution, would be recovered by moving from 2 T to 3 T magnetic field

IDEA vertex

- Reasonable d_0 performance of IDEA vertex using CLD detector and reconstruction
- Additions such as cones for air cooling and services needed, but mostly outside of acceptance

IDEA silicon wrapper

- Worked on simplified version of silicon wrapper, sufficient for first studies
- Working on adaptions to move to a single-layer design

Ultra-light vertex detector concept

- Conceptual design, adapted from ALICE ITS3 to FCC-ee
- Compromise hermeticity (or radius of first hit) with reduced material budget
- Evaluate performance similarly to IDEA vertex

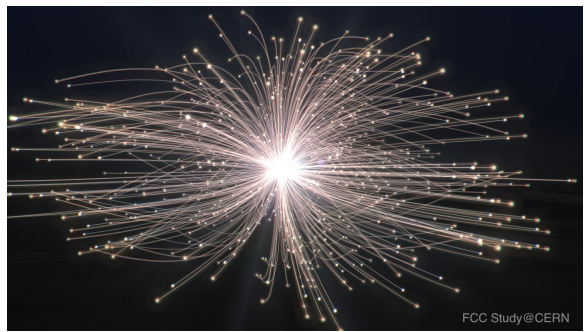
TDAQ Occupancy studies at FCC-ee (vertex detectors)

FCC Week 2024

Armin Ilg

University of Zürich

11.06.2024



University of Zurich[UZH]

FUTURE CIRCULAR COLLIDER

Incoherent pair production in vertex detector

Can we run FCC-ee experiments without a trigger, to get rid of the associated uncertainties?

The problem is incoherent pair production in first vertex layer
In 2019, in CLD vertex, a maximal occupancy of 70×10^{-6} per bunch crossing was found using GuineaPig simulation

- Assuming cluster size of 5, safety factor of 3
- $25 \times 25\,\mu\text{m}^2$ pixels

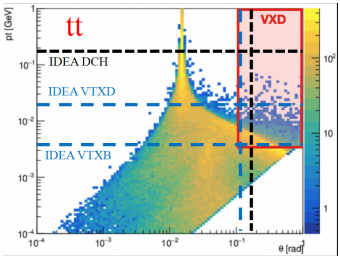
$\rightarrow$ Doesn't seem like a lot, but assuming bunch spacing of 20 ns at Z pole, results in $560\,\text{MHz/cm}^2$

- See also F. Bedeschi's talk in Annecy and A. Ciarma's talk on Thursday

Let's look at first vertex inner barrel layer of IDEA vertex detector!

Table 2: Number of pairs produced per bunch crossing (BX) at the four working points, and maximum occupancy measured in the barrel and endcaps of the vertex detector and tracker (respectively VXDB, VXDE, TRKB, TRKE).

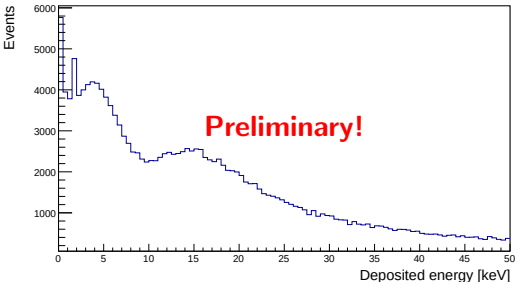
		Z	WW	ZH	$\mathrm{t\bar{t}}$
1	Pairs/BX	1300	1800	2700	3300
10^{-6}	O_{max}(VXDB)	70	280	410	1150
10^{-6}	O_{max}(VXDE)	23	95	140	220
10^{-6}	O_{max}(TRKB)	9	20	38	40
10^{-6}	O_{max}(TRKE)	110	150	230	290

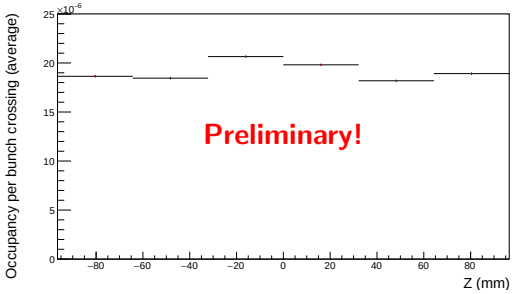


A. Ciarma

Occupancies in IDEA vertex detector

- GuineaPig files with incoherent pair production from 4000 bunch crossings at Z pole (thanks @A. Ciarma!)
  - Using V23 lattice, with bunch population of 1.7×10^{11} (pre mid-term report)
- Paraffin-cooled AlBeMet beam pipe (not CAD beam pipe), first layer at $r = 13.7\,\text{mm}$, $25\,\mu\text{m}$ pitch pixels, cluster size of 5, safety factor of 3
- Cut at $E_{\text{dep}} \geq 1.8\,\text{keV}$, equivalent to 500 electrons

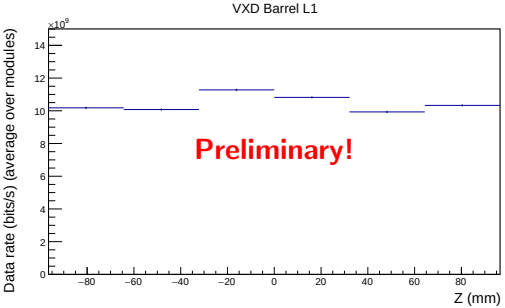




Lower occupancy than in previous study (70×10^{-6}), see hit rate of up to $170\,\text{MHz/cm}^2$

Data rate in IDEA vertex detector

- Without trigger: Assume 32 bits transferred per pixel (10+8 needed for ARCADIA), could be reduced if on-chip center of gravity is reconstructed

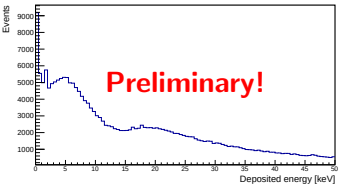


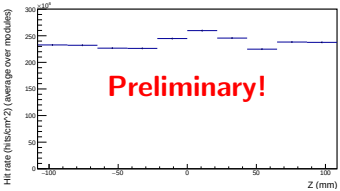
- Quite regular along z
- Recall safety factor of 3, cluster size of 5
- Will need to check impact of V24 lattice (with 2.14×10^{11} bunch intensity, see F. Zimmermann's slides) $\rightarrow$ Details on lattice versions in backup

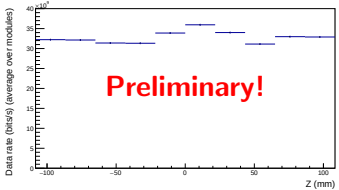
$\rightarrow$ Need to continue these studies!

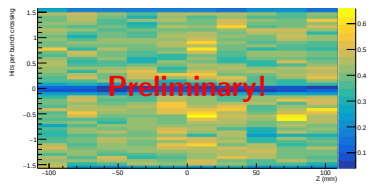
$\rightarrow$ Triggerless readout for the moment seems neither impossible nor straightforward

Occupancies in ultra-light IDEA vertex detector (first layer)









- Quite regular occupancy in z and around ϕ (consider holes in coverage at $\phi = 0, \pi$)
- Higher data rate per module mostly comes from larger area per module ($\sim$ factor 2)
- Hit rate of $\mathcal{O}(250\,\mathrm{MHz/cm^2})$

Conclusions

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Incoherent pair production background in IDEA vertex

- Decreased occupancies in vertex coming from lattice used
- Further studies needed
  - → Use mid-term report lattice
  - → What is the impact of an increased threshold on physics?
  - → Can part of the background be cut away on-detector e.g. using cluster size? (need silicon digitisation with clustering algorithm in Key4hep)

Detector optimisation: Smallest possible systematic uncertainties in detector

- Uncertainty coming from using a trigger
- Uncertainty coming from material budget
- Uncertainty coming from spatial resolution

→ Smaller pixels, larger cluster sizes, trigger-less readout and on-detector processing lead to more power consumption → More cooling → More material budget → Uncertainty!

→ Need to consider all aspects simultaneously!

Thanks!

References I

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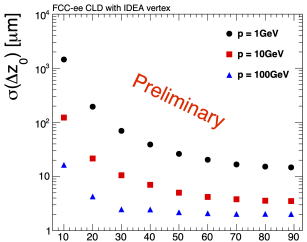
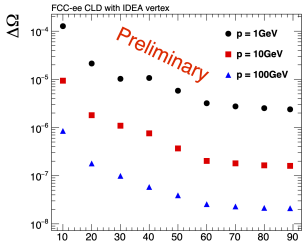
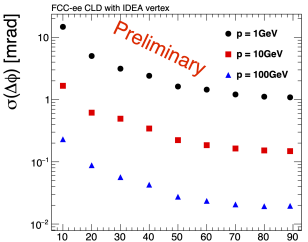
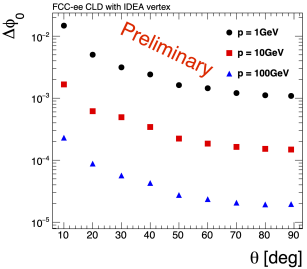
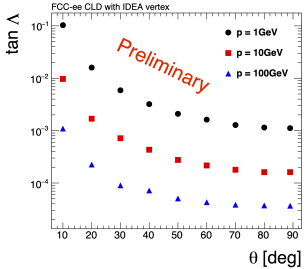
Further performance plots

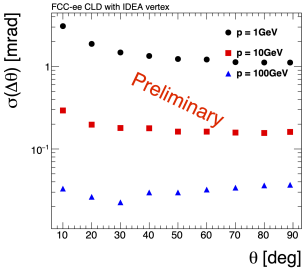










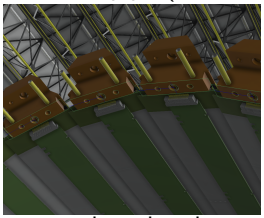


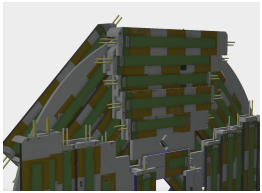
Lattice versions for vertex background studies

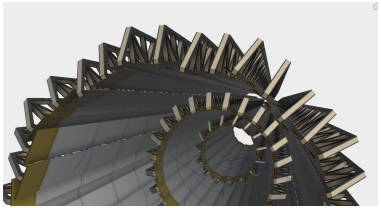
Study	Lattice	Bunch population [10^{11}]	Bunch spacing [ns]
CLD study	VXX	X.X	30
Det. concept last week	V22	2.4	19.2
This work	V23	1.7	19.2
To do (mid-term)	V24	2.14	25

IDEA vertex detector: Design

Vertex detector by INFN Pisa (more details in F. Palla's talk at 2nd FCC US Workshop), support tube by INFN-LNF, holding lumical, vertex and beam pipe (more on MDI in M. Boscolo's talk)

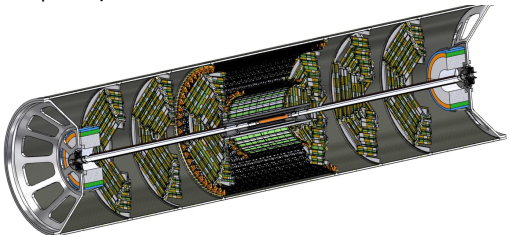






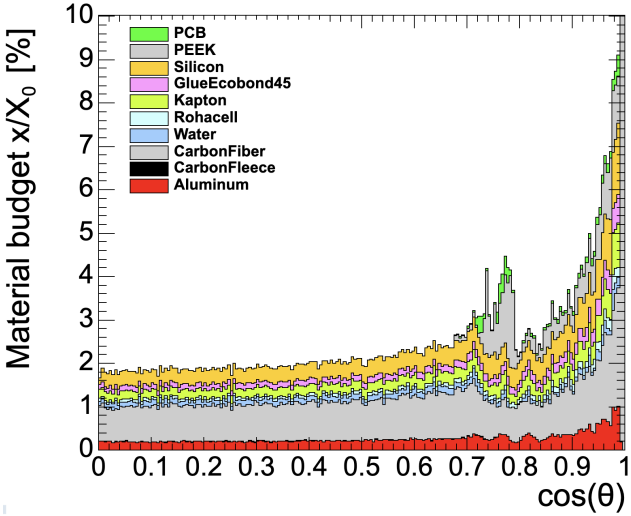
Vertex outer barrel and vertex disks using quad ATLASPix3 DMAPS with $150 \times 50\,\mu\text{m}^2$ pixels, water-cooled

Vertex inner barrel consisting of staves of dual ARCADIA DMAPS, with pixels of $25 \times 25\,\mu\text{m}^2$ ($\sim 3\,\mu$m single point resolution), air-cooled



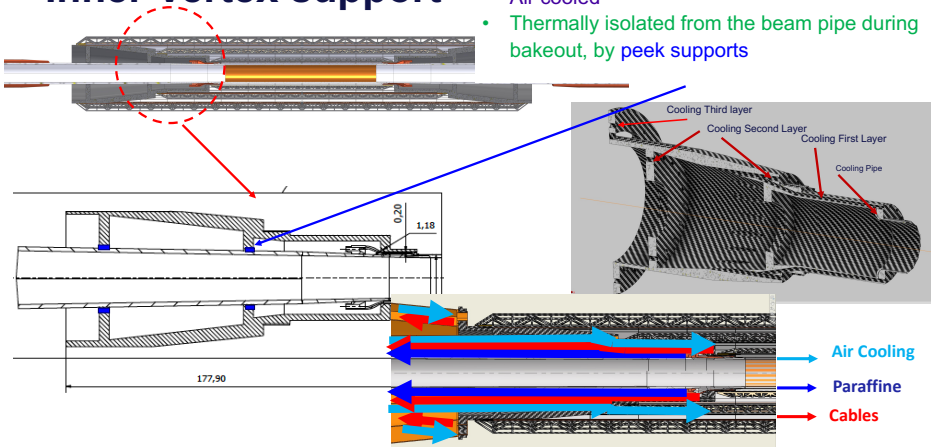
Material budget: Vertex inner barrel support

Only contribution in last two bins



Inner Vertex support

- Anchored to the conical chamber
- Air cooled
- Thermally isolated from the beam pipe during bakeout, by peek supports



F. Palla, 2nd FCC US Workshop

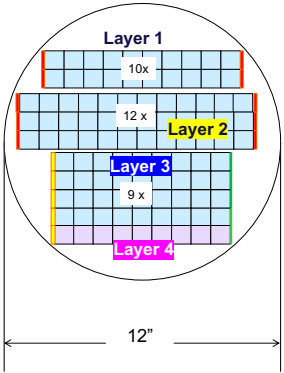
Data rates issues *(see F. Bedeschi talk at 7th FCC Workshop)*

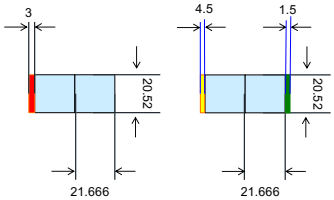
- **Largest data rates occur at the Z energy**
- **Expected data rates per BX/module [cluster size 5]**
  - From machine backgrounds (Incoherent pair creation – safety factor of 3) ~ 19 hits/BX/module
  - From collisions (200 kHz) ~ average ~<1 hit/BX/module
- **Inner layer ~400 MHz/cm^2 → ~25 Gb/s per module**
  - might be reduced if cluster size is only 2 – as measured for many MAPS
  - *ALICE3 hit rate ~100 MHz/cm^2 (pixel size 10μm x 10μm)*
  - 2nd layer ~10x less data volume
- **Triggered readout**: for 200 kHz the data bandwidth per module, rate is only 150 Mb/s
  - Impact on physics?

- **All these depend on pixel pitch, thickness, R/O architecture, bias voltage.**
  - For a review see M. Winter talk at March 11 meeting

F. Palla, 2nd FCC US Workshop

Same reticle for all layers





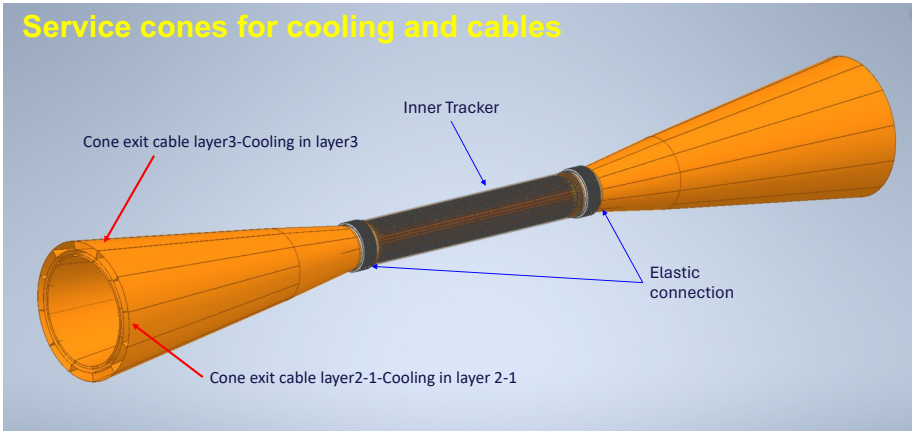
Layer	Radius (mm)
1	13.7
2	20.23
3	26.76
4	33.3

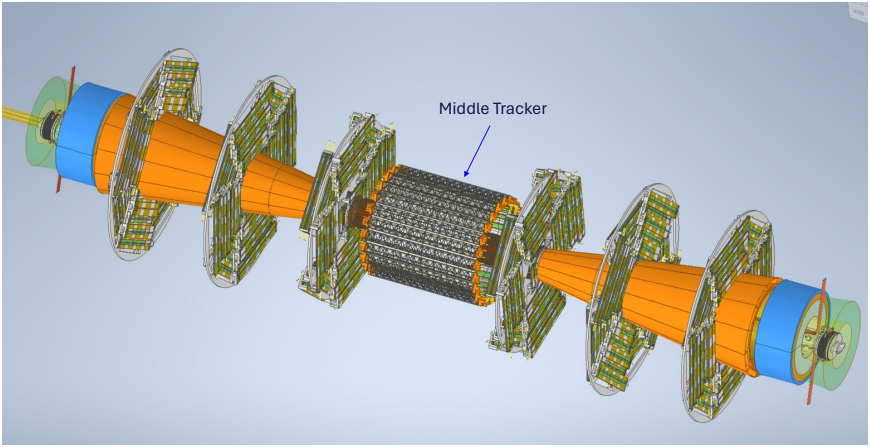
	Power density [mW cm^{-2}]		
	Expected 25 °C	Max 25 °C	Max 45 °C
Left End Cap (LEC)		791	
Active area (RSU)	28	44	62
Pixel matrix	15	32	51
Biasing	168	168	168
Readout peripheries	432	457	496
Data backbone	719	719	719

Power dissipation in ITS3
(not necessarily the same for FCC-ee)

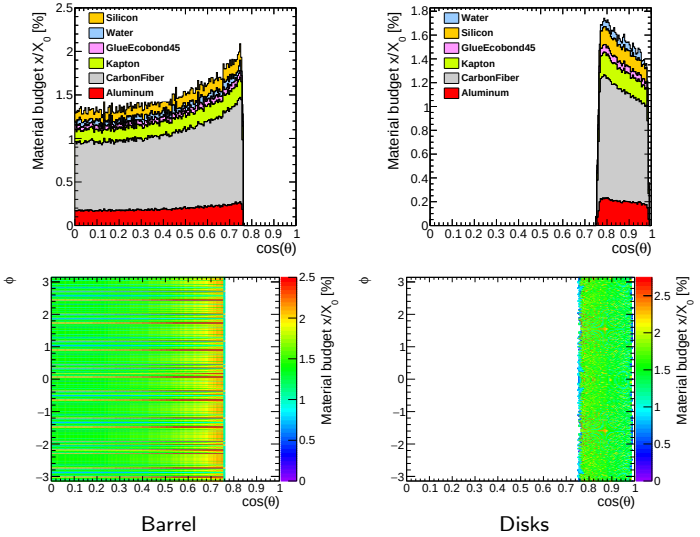
- RSU~ 50 mW/cm^2 (depends on Temp.)
- LEC ~ 700 mW/cm^2

Service cones for cooling and cables



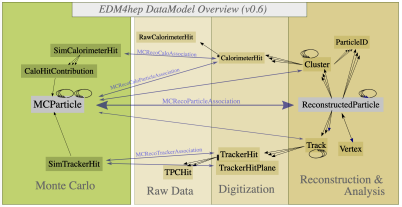
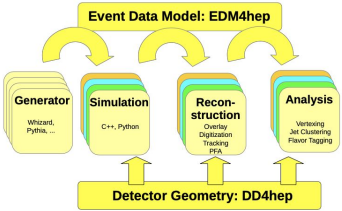
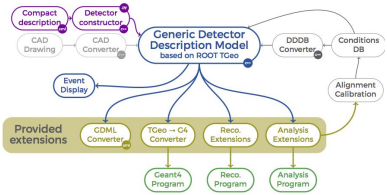

Middle Tracker

IDEA Silicon Wrapper material budget



- Flex and cooling pipes (same as in vertex outer barrel and disk), 50 μm silicon, 1.4 mm of carbon fibre
- Adjust material budget when engineered design becomes available

The common software vision: Key4hep

Key4hep is a huge ecosystem of software packages adopted by all future collider projects, complete workflow from generator to analysis

- Event data model: EDM4hep for exchange among framework components
  - Podio as underlying tool, for different collision environments
  - Including truth information
- Data processing framework: Gaudi
- Geometry description: DD4hep, ability to include CAD files
- Package manager: Spack: `source /cvmfs/sw.hsf.org/Key4hep/setup.sh`