Inspiration from instrumentation for the FCC

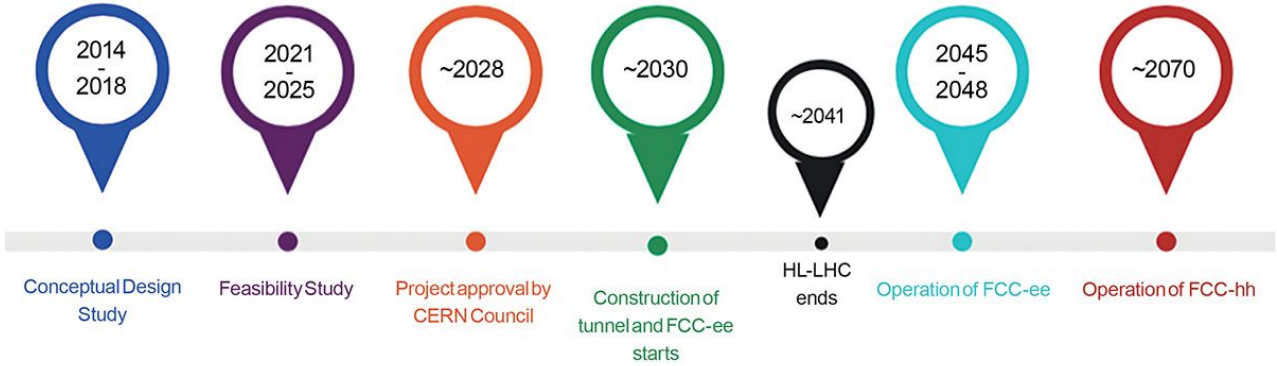
P.A. (Sander) Breur for SLAC TID Instrumentation

June 12, 2024

SLAC NATIONAL ACCELERATOR LABORATORY

Stanford University | U.S. DEPARTMENT OF ENERGY

Timeline: Who will do science with the technology of the FCCee?



Source: Fabiola Gianotti

Me?

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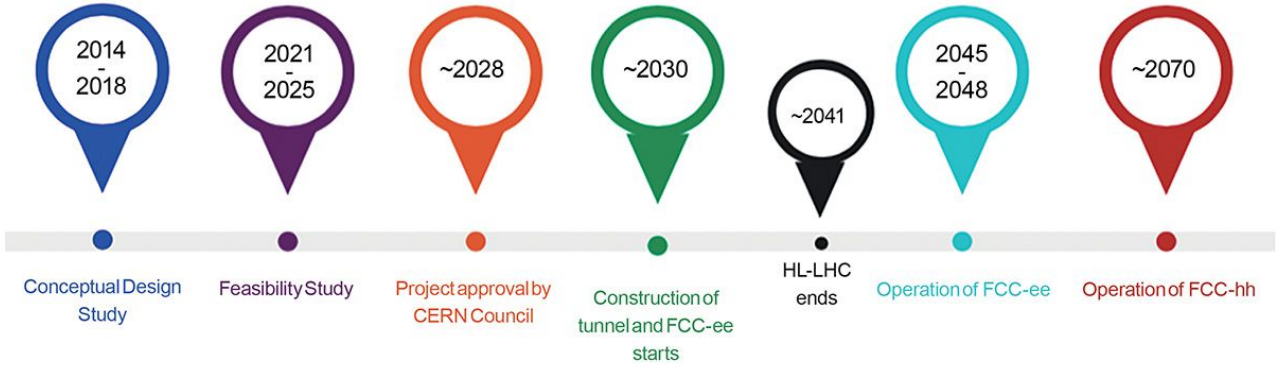

Me: Born in 1984, Current life expectancy 86 years. 1984+86 is 2070…

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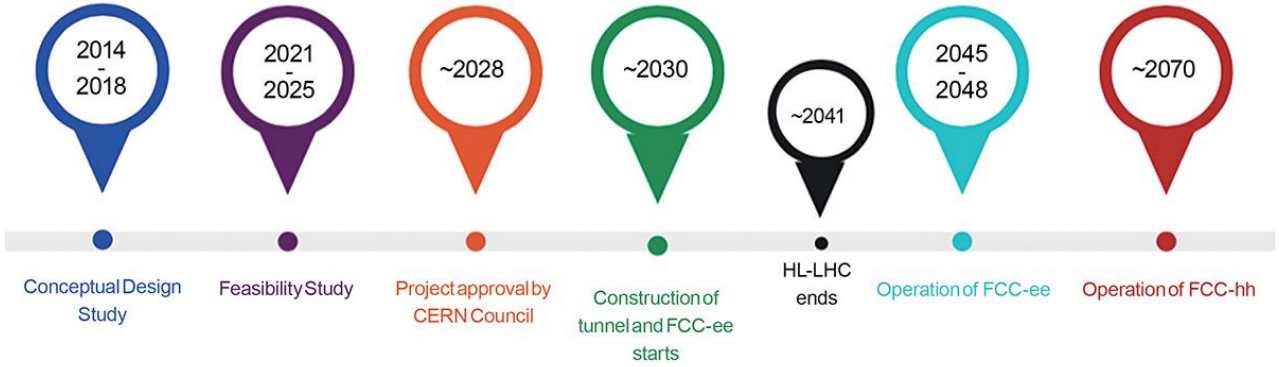

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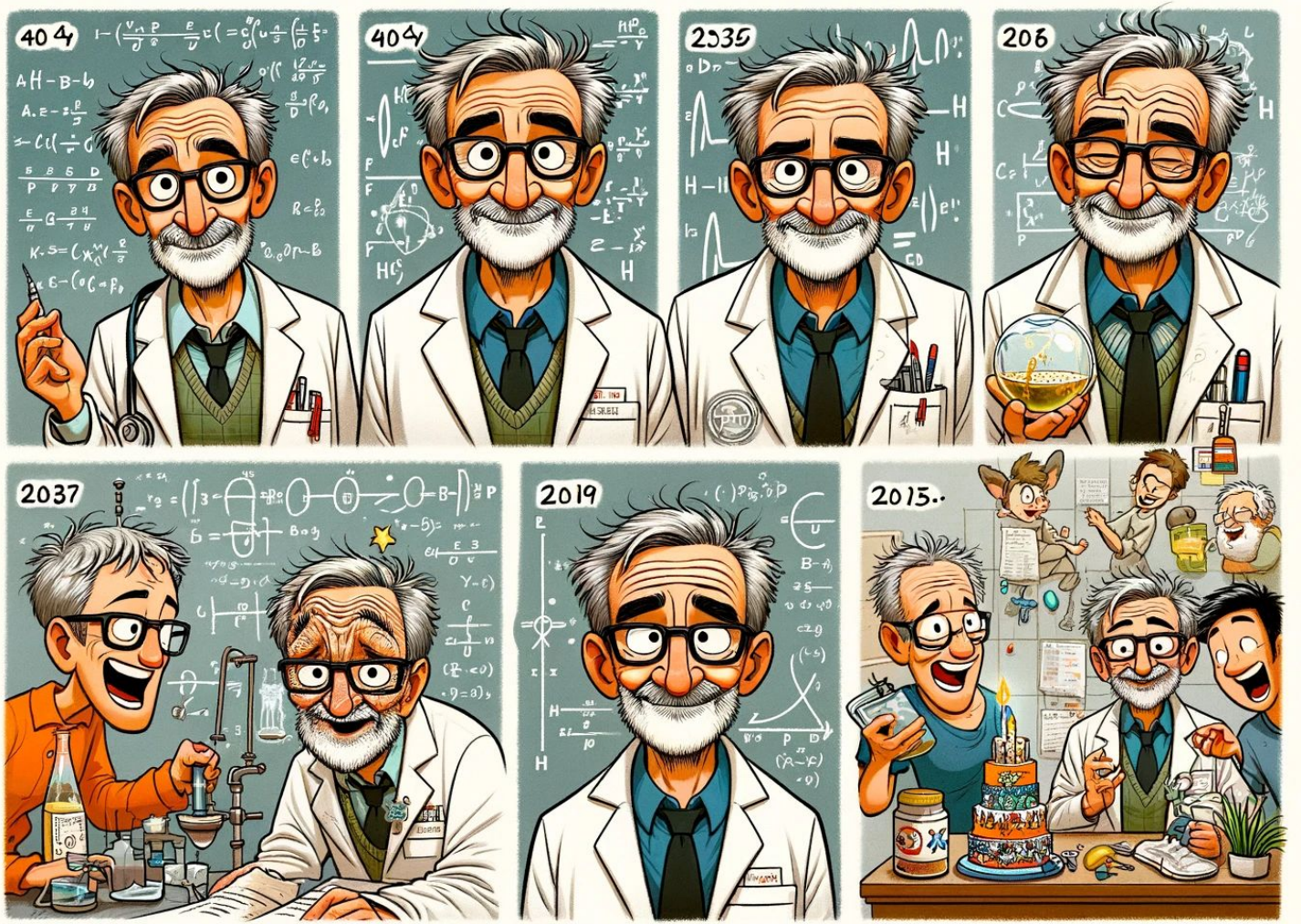
Anyone in this room with a permanent position?

Source: ChatGPT 4o, 6/11/24



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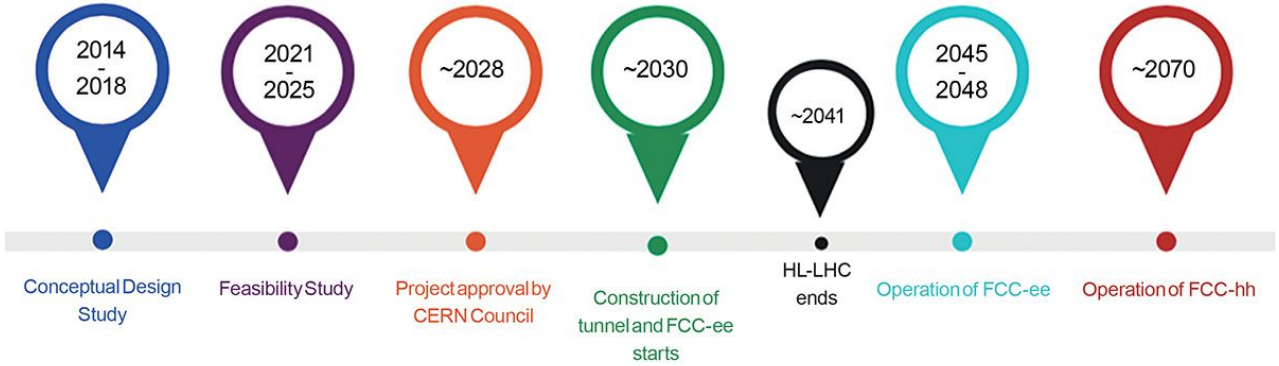
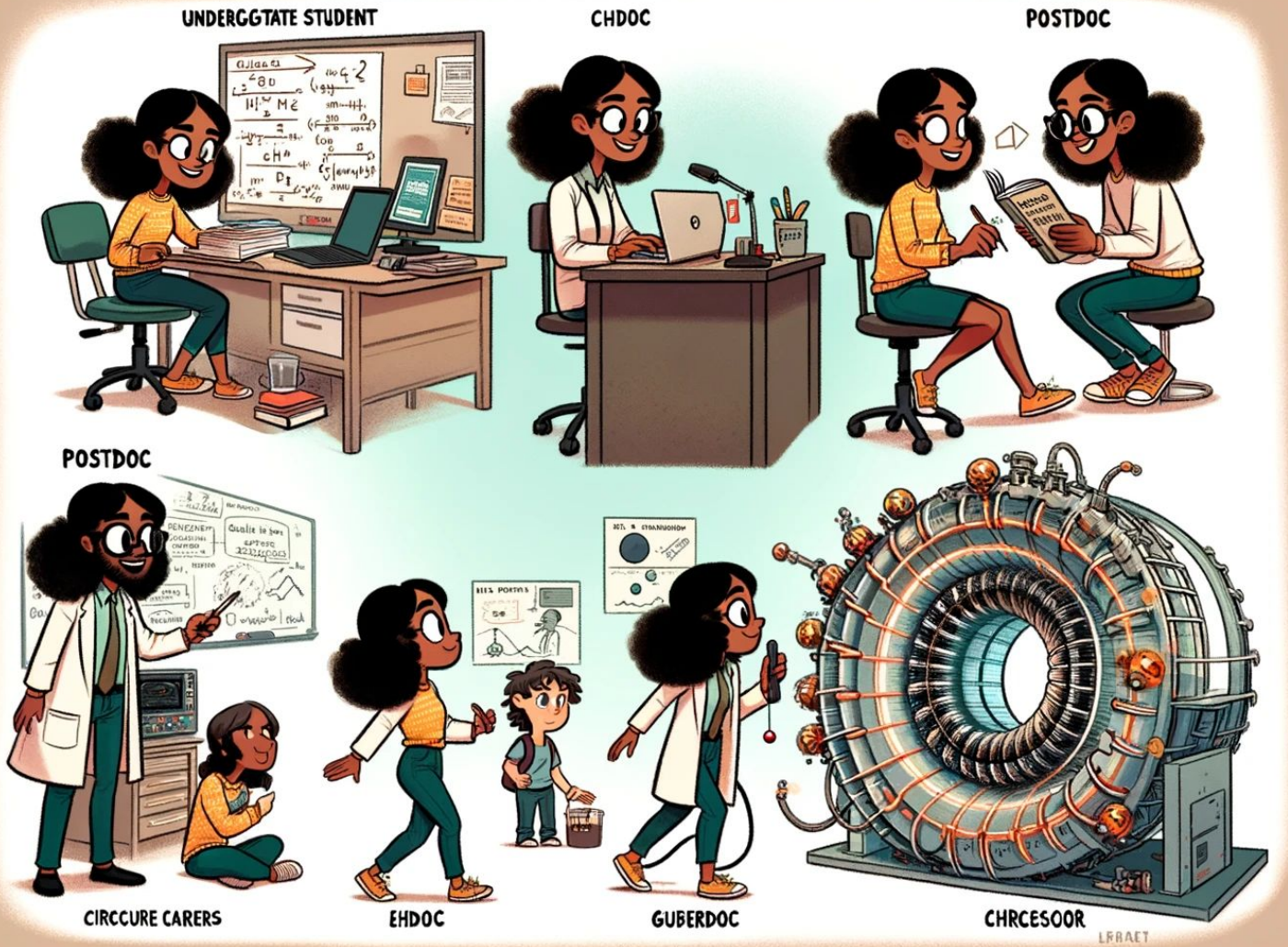


Me: Born in 1984, Current life expectancy 86 years. 1984+86 is 2070…

Anyone in this room with a permanent position? Probably not…

Any undergrads in the room?



Source: ChatGPT 4o, 6/11/24

My goal of today?

To **inspire** more undergrads to join us working towards the FCCee

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By showing technology that you can **work on right now**

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By showing technology that you can **work on right now**

In a way that hopefully **keeps your attention** away from your phone and laptop for 13 more minutes ;)

So what will I talk about today?

- Two sensors: MAPS & LGAD
- One ASIC for fast timing
- ML on ASIC in embedded FPGA
- Open-source libraries for trigger and DAQ hardware

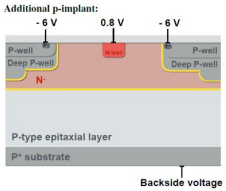
Sensor technologies: MAPS for tracking & calorimeter systems

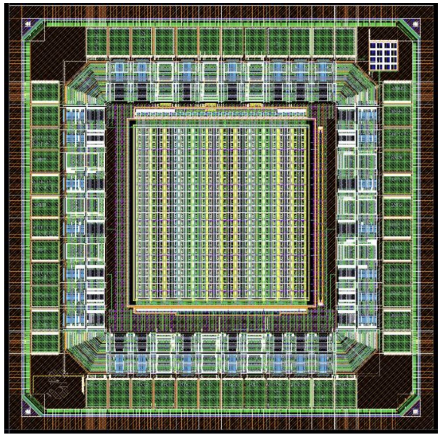
- **Co-design** approach: close interaction between physics studies and technology R&D.
- Novel CMOS process for MAPS has recently become available, CERN (WP1.2 Collaboration) provides access to scientific community: TowerJazz-Panasonic (TPSCO) **65 nm CMOS** imaging process with modified implants
- Builds on sensor optimization done for the TJ180 process, **excellent charge collection efficiency and low capacitance**
- Increased density for circuits: **Higher spatial resolution, better timing performance at same power consumption**.
- **Supports stitching**: enable wafer-scale MAPS potential to greatly reduce costs of future experiments

For more on possible MAPS application in FCC see e.g.:

- ➔ ***MAPS-based tracker developments from ITS3 towards FCCee*** *Giacomo Contin (Tu)*
- ➔ ***Optimization of Si tracking systems*** *Armin Ilg (Tu)*
- ➔ ***The Silicon Vertex Tracker of the ePIC Detector at the Electron-Ion Collider*** *Nicole Apadula (Th)*

See our CPAD 2023 presentation for more details:





Layout of SLAC prototype for WP1.2 2022 shared submission on TowerSemi 65nm

R&D right now: NAnosecond Pixel for large Area sensors (NAPA)

Approach:

- Engaged with the scientific community to share know-how
- Focus on long-term R&D, targeting simultaneously:
  - **Power consumption** compatible with large area and **low material budget**
  - Fault-tolerant circuit strategies for **wafer-scale MAPS**
  - **~ns timing resolution**

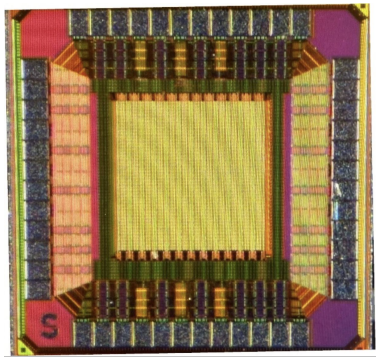
Highlights:

- Designed pixel architecture with **binary readout** optimized for colliders
- Submitted a small pixel matrix for fabrication on **CERN WP1.2 shared run** (25x25um pixel, 25x25 pixels, 5x5mm)

Next steps:

- **Measure performance** of 1st SLAC prototype on TJ65nm (2023/2024).
- **New design** combining O(ns) timing precision and low-power (2024/2025).
- Stretch Goals: design of a wafer-scale ASIC (2025/2026, design only)

➔ *Interested? Collaborate with:*
Caterina Vernieri and Lorenzo Rota



Picture of NAPA-p1 prototype from WP1.2 shared submission

	Specification	Simulated NAPA-p1	
Time resolution	1 ns-rms	0.4 ns-rms	✓
Spatial Resolution	7 μm	7 μm	✓
Noise	< 30 e-rms	13 e-rms	✓
Minimum Threshold	200 e-	~ 80 e-	✓
Average Power density	< 20 mW/cm^2	0.1 mW/cm^2 for 1% duty cucle	✓

LGAD: 3D Integrated Sensing Solutions

For more on possible LGAD application in FCC see e.g.:

- ➔ ***Investigation of low gain avalanche detectors exposed to proton fluences beyond 10^15 neq/cm2 and gamma dose up to 2.2 MGy*** *Josef Daniel Sorenson (Th)*
- ➔ ***High radiation resistance LGAD designs*** *Dr Simone Michele Mazza (Th)*
- ➔ **The Development of Silicon Carbide Low Gain Avalanche Detector** Tao Yang (Th)

Project

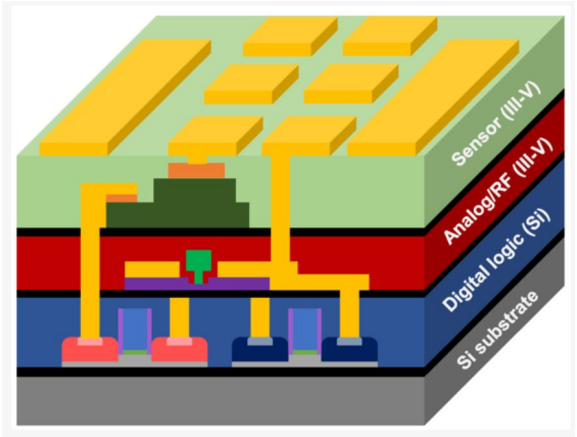
- 2-year project funded by proposal to DOE "Accelerate Innovations in Emerging Technologies" call (**SLAC, FNL, LLNL collaboration**)

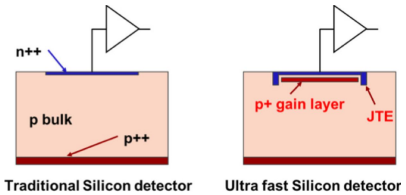
Objective:

- Develop technology to enable large-scale particle detectors to **simultaneously** achieve **10 µm position resolution** and **10 ps precision timing**, with low-power consumption and high throughput rates.

Goals:

- LGAD Development: Design and manufacture LGADs compatible with 12" foundry process, because **28nm CMOS** is fabricated on **12" wafers**
- ASIC design: Develop ASIC designs to meet aggressive power and timing requirements on 28nm CMOS for HEP applications
- Develop **3D integration capability**





[1] N. Cartiglia et al. LGAD designs for Future Particle Trackers, https://doi.org/10.1016/j.nima.2020.164383
[2] Jeong, J.; Geum, D.-M.; Kim, S. Heterogeneous and Monolithic 3D Integration Technology for Mixed-Signal ICs. *Electronics* **2022**, *11*, 3013. https://doi.org/10.3390/electronics11193013

R&D right now: LGAD & 3D Integrated Sensing Solutions

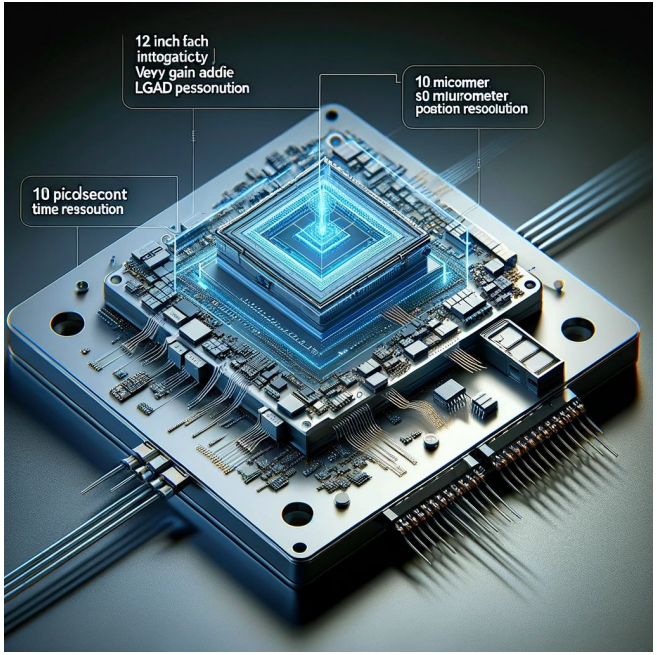
2024 R&D runs:

Using the 28nm CMOS foundry process: The 28 nm CMOS process has emerged as the technology of choice for the next decade of developments in HEP read-out circuits:

- LGAD sensors first run in 2024: **50x50um** and 100x100um pixels, **AC coupled** + deep-junction versions
- ASIC submitted: SLAC TDC with **~6ps resolution** with Front-End from FNAL

Next steps:

- 3D integration (TSV) to offer potential for more functionality per pixel, improvement in speed, power consumptions, smart read-out



ChatGPT 4o Interpretation of 3D integration of sensor and ASIC

Interested? Collaborate with: Julie Segal and Chris Kenny

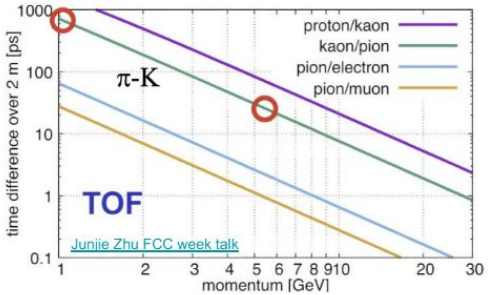
Front end: 4D tracking via <10ps TDC in ASIC

For more on possible fast timing applications in FCC see e.g.:

➔ ***Fast timing possibilities at FCC-ee*** *Matthew Gignac (Tu)*

Fast timing?

If you are interested in distinguishing pi-K at low momentum, then your LGAD sensor also needs **ultrafast readout**

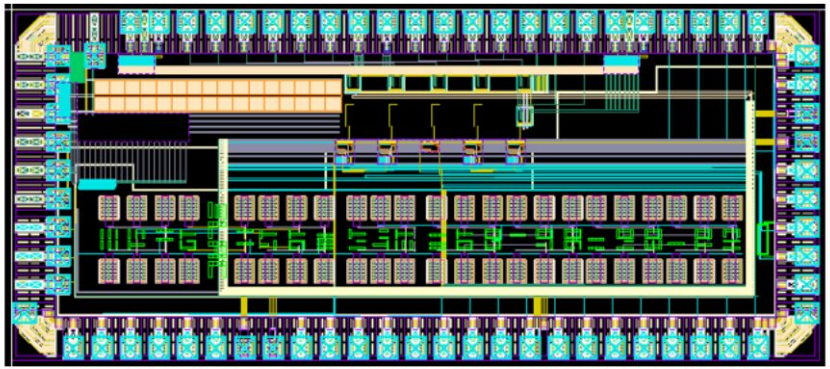


Source: *Matthew Gignac*

Approach:

Our **ASIC team** is creating sub 10 picosecond TDC's

In January 2024: **28nm prototype** submitted with **design of 6.25ps TOA** and 50 ps TOT.



Interested? Collaborate with:
Bojan Markovic and Ariel Schwartzman

Distributed computing: ML on ASIC - FABulous (Open source)

Problem: Data rate

Our approach:

Embedded **FPGA on ASIC** gives low latency and configurability

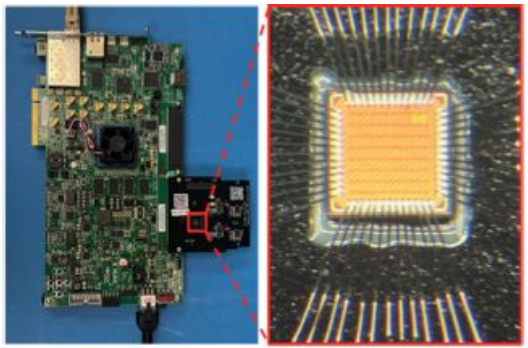
Create open source framework and test on **28 nm** CMOS technology

In **Feb. 2024 achieved first proof-of-concept** configuration of toy eFPGA with track classifier Boosted Decision Tree (BDT) with 100% accuracy to quantized software result!

FABULOUS
eFPGAs made easy

https://fabulous.readthedocs.io/en/latest/

Read the paper '*Embedded FPGA Developments in 130nm and 28nm CMOS for Machine Learning in Particle Detector Readout*' here



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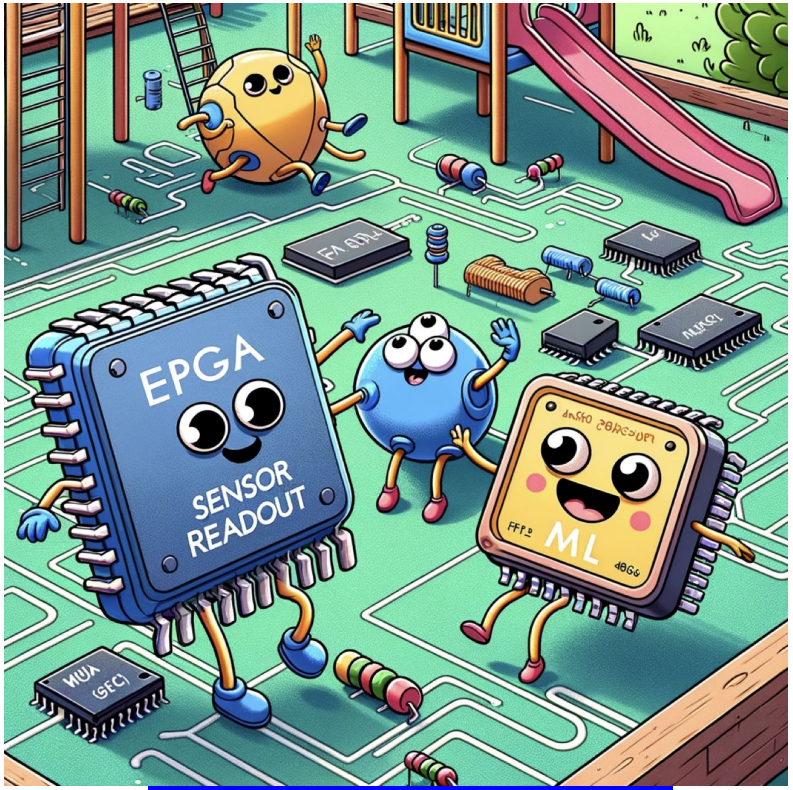
Next steps: FABulous

- Codesign* a higher-performance 28nm eFPGA to create a viable readout option for detector concepts in the 5-10 year timescale

- R&D to use eFPGA to interconnect analog compute resources (cryogenic and rad hard)

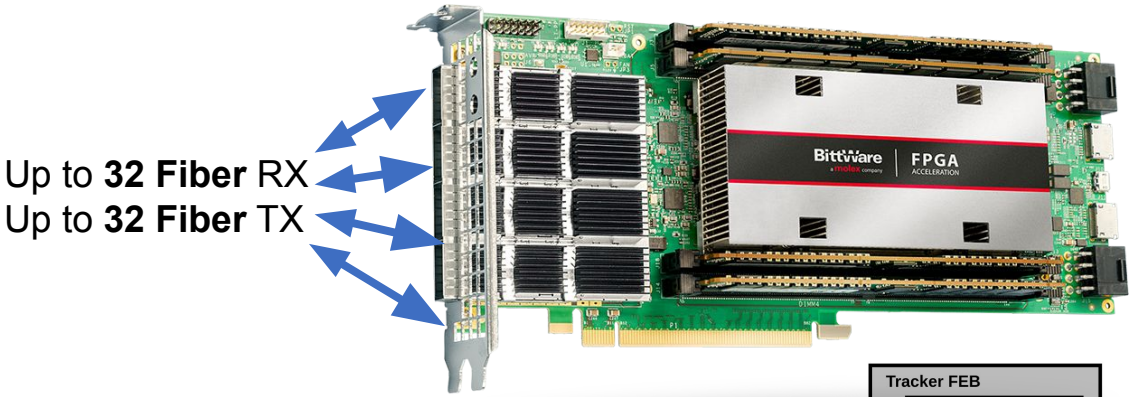
Interested? Collaborate with:
Larry Ruckman and Julia Gonski



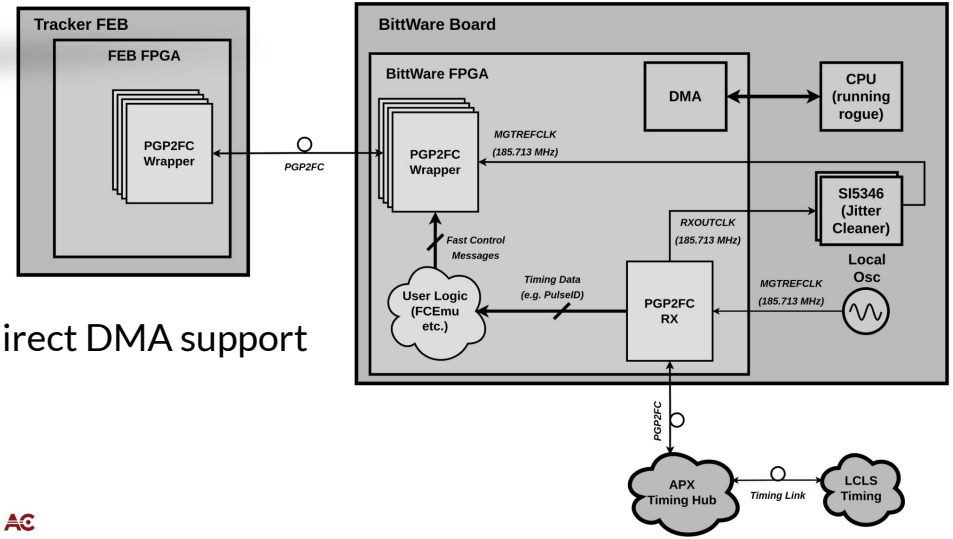
chatGPT Generated Image

* SLAC, LBNL, Stanford University

Trigger and DAQ: Commercial PCIE Based Readout & Triggering



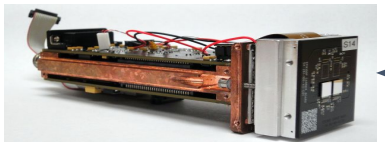
- **Current efforts** in LDMX and nEXO
  - Both are triggered systems
  - Ring buffers in PCIE/Host memory
- **Trigger logic** resides in **bitware card**
- Online compression in FPGA using HLS
- SLAC **developed DMA engine**
  - Support direct to GPU and PCIE - PCIE direct DMA support
- Supports **high bandwidth** and **high frame rate**

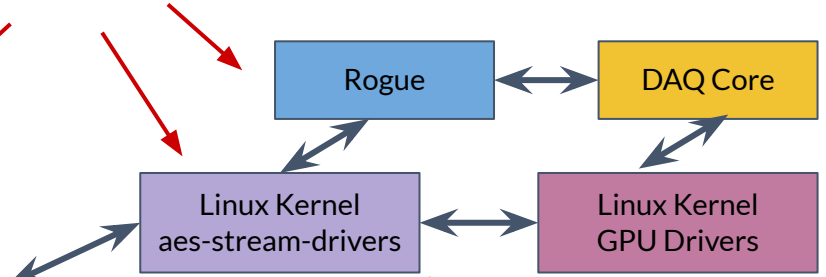


SLAC Is Committed To Portable Open Source Libraries Allows IP To Bridge Generational Hardware Platforms

- Reliable UDP (RUDP) Network offload engine to **support network attached devices** (NAT)
- High bandwidth synchronous (timing & trigger delivery) & asynchronous **fiber protocols** for front end readout (PGP2,PGP4)
- **SLAC Ultimate RTL Framework (*SURF*)**:
  - Open source VHDL/Verilog framework for **rapid FPGA/ASIC development** using common generic, extensible libraries
  - ***Ruckus***: Open source build system
- Open source **DMA engine** & associated driver for high bandwidth & high rate DMA transfer
  - Works both in amd64 & Zynq (SOC + RFSOC) platforms
  - Zero copy user space buffer mapping
  - Direct to GPU data transfer support
- ***Rogue***: Open source **Python/C++ hardware abstraction software** for rapid readout development & test stand support
  - Easily integrated into back end DAQ systems
  - **Balanced python** (ease of use) and **C++** (high bandwidth & high event rate) implementation

https://github.com/slaclab/surf
https://github.com/slaclab/ruckus
https://github.com/slaclab/rogue





Direct to GPU DMA support in open source DMA Engine & Driver

Interested?
Collaborate with: Ryan Herbst

Summary and conclusion

Source: Joanne Hewett

- One way to **inspire** the **next generation of scientists and engineers** to work on the FCC right now, is to do **instrumentation R&D** right now
- Snowmass and P5 were clear in their call for **more instrumentation R&D funding**. Especially for the US this is critical.
- To inevitably **change** from **our current demographics**, to one that is more in line with our society, we will need to be very **open and accepting**, without prejudice [DEIA: 2209.12377, 2203.08748]
- So let's invest in **FCC specific summer schools** and **intern positions**, **increase cross-pollination** between **universities** and the **national labs** via RDC R&D and keep asking our **early career scientists** to speak up and step up

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