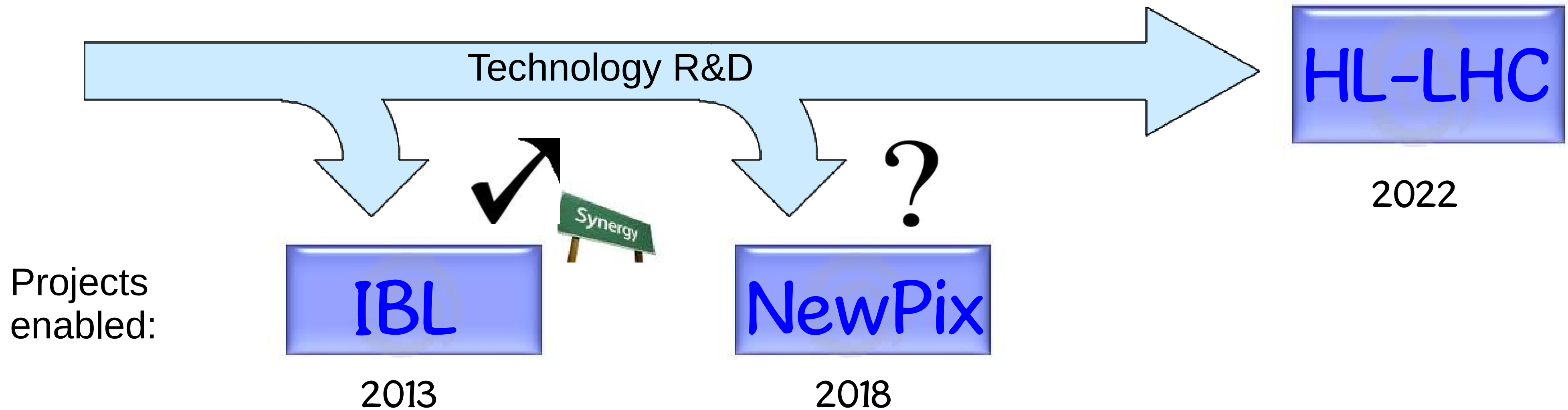
ATLAS Pixel Upgrades

DPF Meeting
Aug. 9, 2011

Introduction

- “The goal is a massless, cheap, infinite granularity, 100% hermetic and efficient, infinite bandwidth, long lifetime detector”
- The pixel detectors in operation today are great, but not that
  - Not because we did not think of it
  - We did the best we could with the existing technology at the time
- Focus of pixel detector community with ATLAS has since been on development of new technology
  - Will review some of these developments
- First ATLAS upgrade project applying newly developed technology is the Insertable B-Layer (IBL)
- Will also discuss <u>possible</u> future upgrades

ATLAS pixel roadmap



- R&D goals:
  - Lower mass and power
  - Lower cost
  - Higher rate and radiation

R&D *inspired* by HL-LHC environment- not narrowly constrained by rigid specifications.

FE-I3

FE-I4

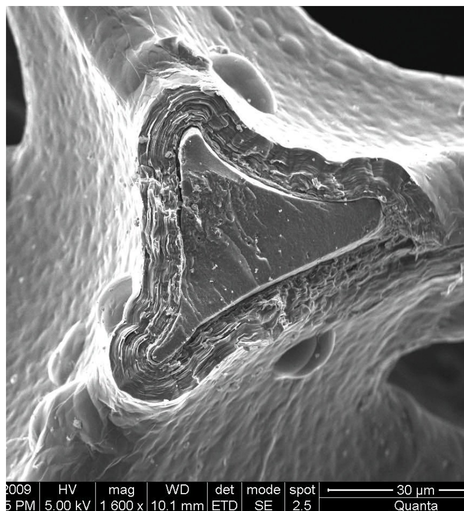
FE-I4

- FE-I4A, fabricated summer 2010
- FE-I4B, about to be submitted for fabrication
  - Production version for IBL upgrade
- FE-I4C, future revision for 4-chip outer modules

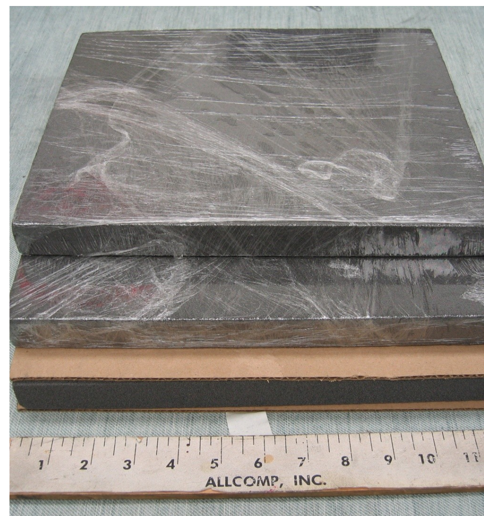
- FE-I4 chip features / innovations:
  - Largest footprint possible to reduce system cost- important for large area upgrades
    - 26,880 pixels 50μm x 250μm
  - Local digital storage architecture enables much higher rate than present chips, and with low power
  - Integrated voltage regulators and a first x2 DC-DC converter
    - Regulators have shunt mode to enable serial connection
  - High level functionality- serial command driven and 8b10b encoded framed output
    - No additional control chips needed
  - 130nm CMOS process enables high radiation tolerance- tested to 250 Mrad

Thermally Conductive carbon foam

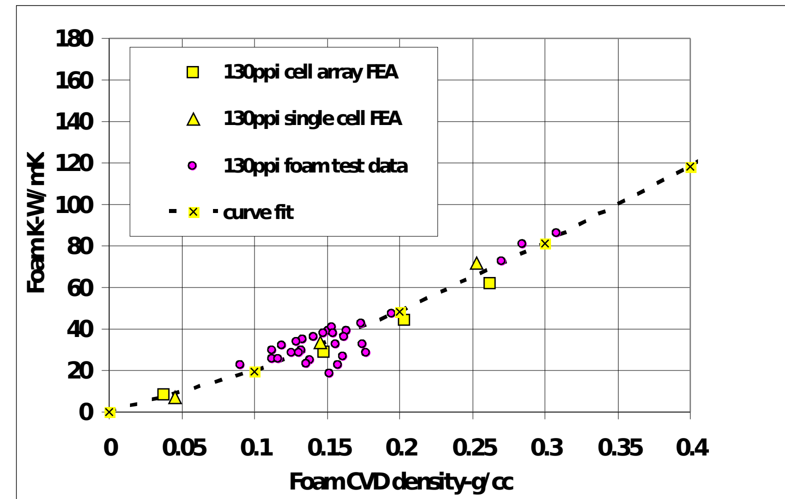
- A new type of all-carbon foam has been developed for silicon pixel and silicon strip mechanical/cooling local supports
- Readily machinable. High thermal conductivity. Low radiation length.
- Baseline now for ATLAS IBL, pixel local supports for Phase I and Phase II. Candidate for strip local supports.
- Reliability validated after extensive thermal cycling and up to 1 Grad
- Development by Allcomp, Inc. with SBIR support



Micrograph showing open cell structure After treatment



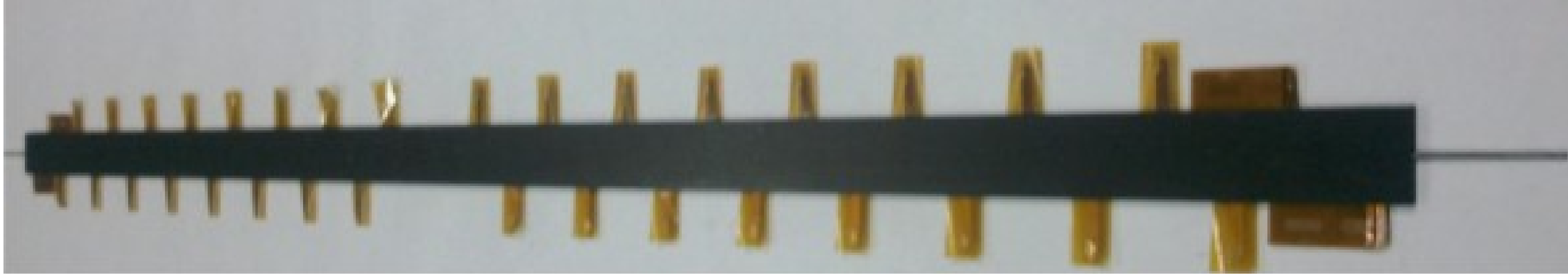
Produced in blocks

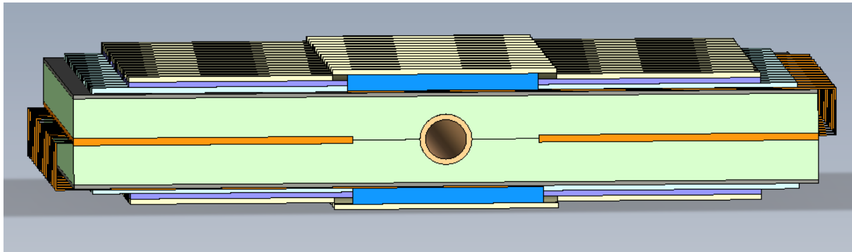


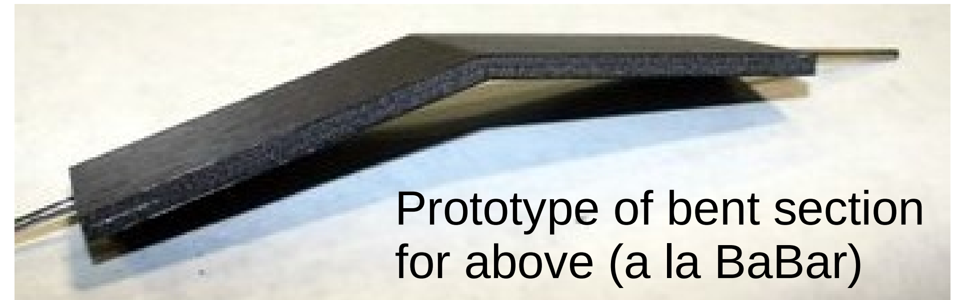
Thermal conductivity vs. density

New electro-mechanical integrated structures

Integrated stave prototype with embedded cables (1.4m long)







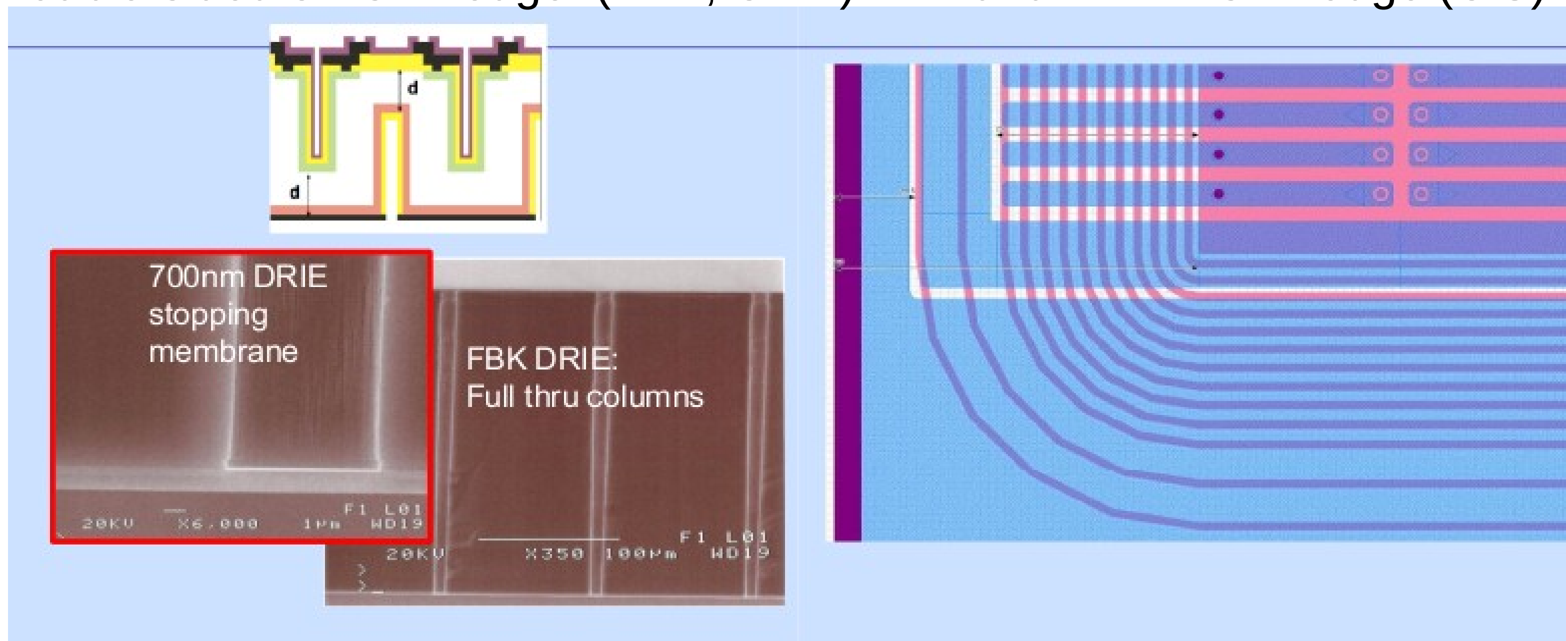
Prototype of bent section for above (a la BaBar)

I-beam prototype for inner 2 layers (shared support structure a la Alice)

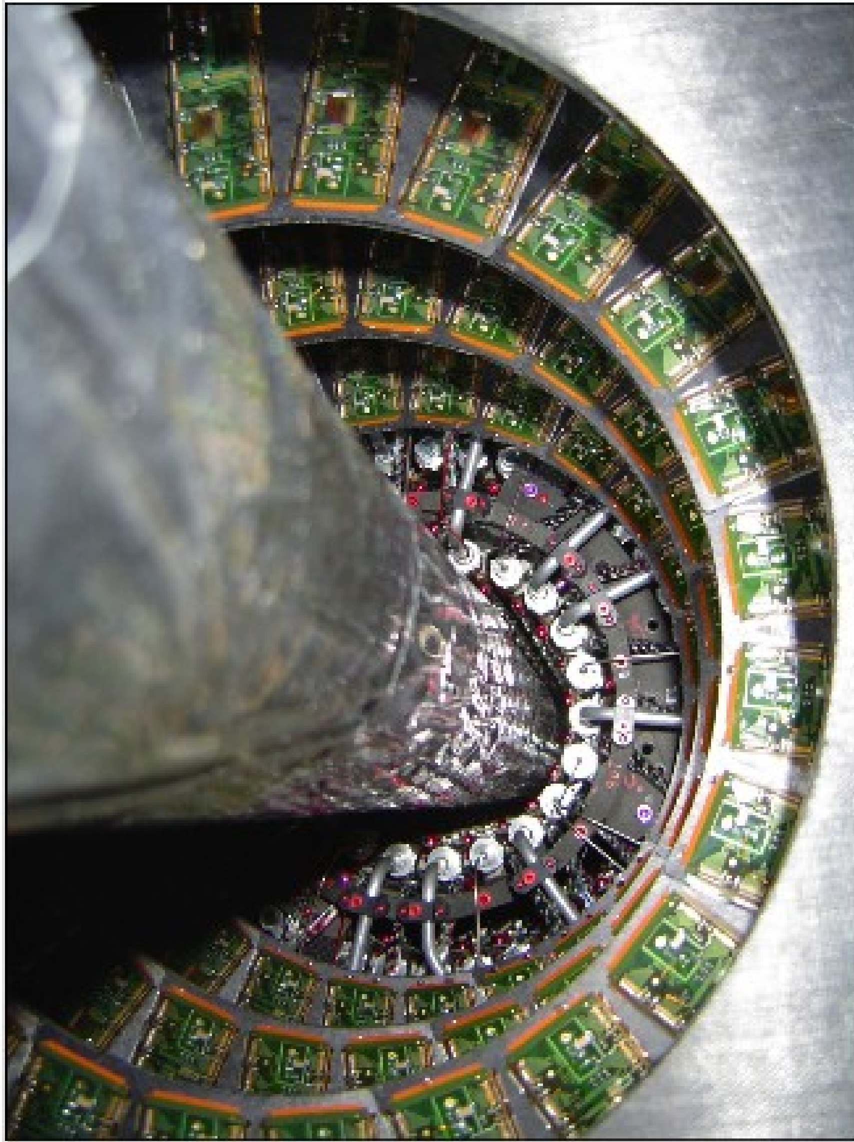
Sensors

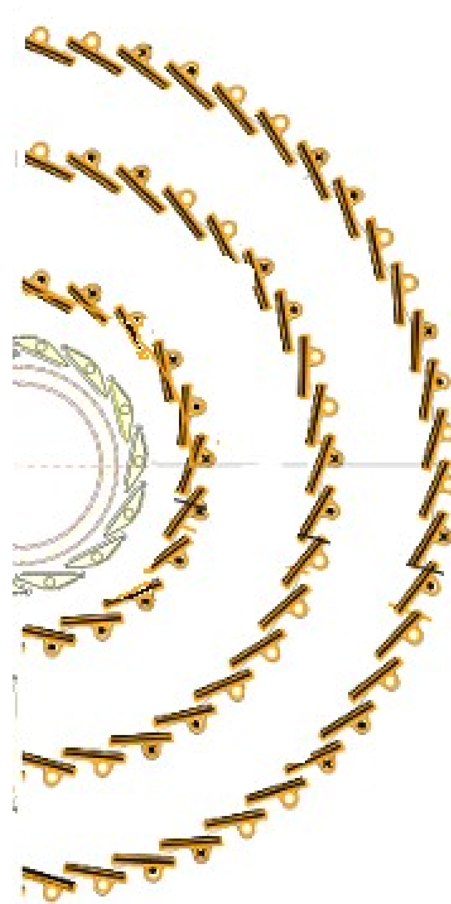
- Pixel sensor development greatly advanced by IBL project
- Sensors compatible with FE-I4 produced in diamond, silicon 3D, and several planar flavors, including p-on-n on 6 inch wafers.
- While IBL will only use a small number of sensors in the end, R&D and other projects will benefit from advances

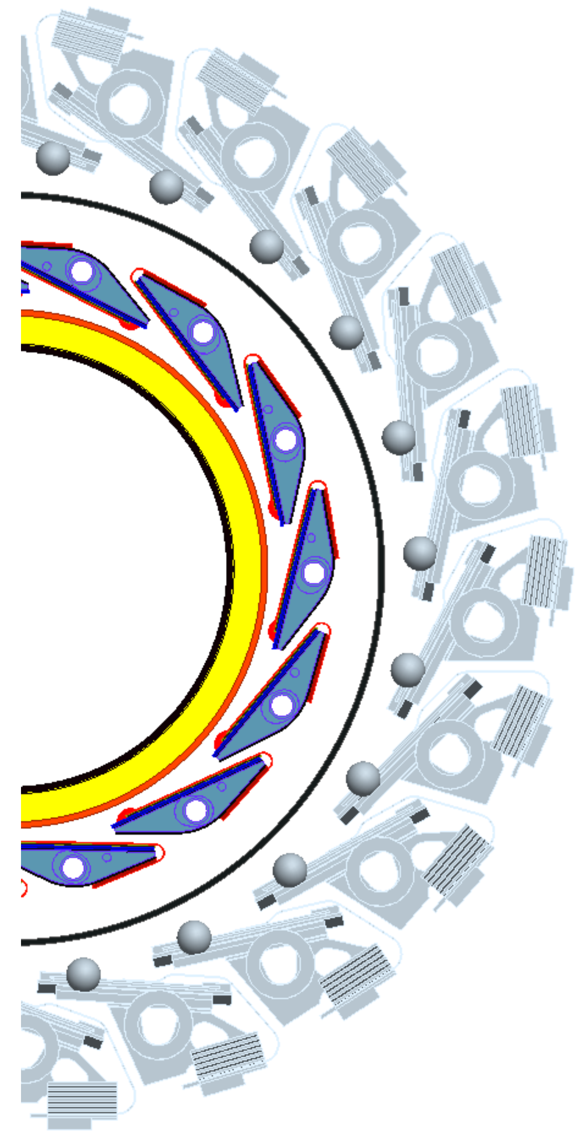
Double-sided 3D slim edge (FBK, CNM) Planar n-in-n slim edge (CiS)



Insertable B Layer (IBL)

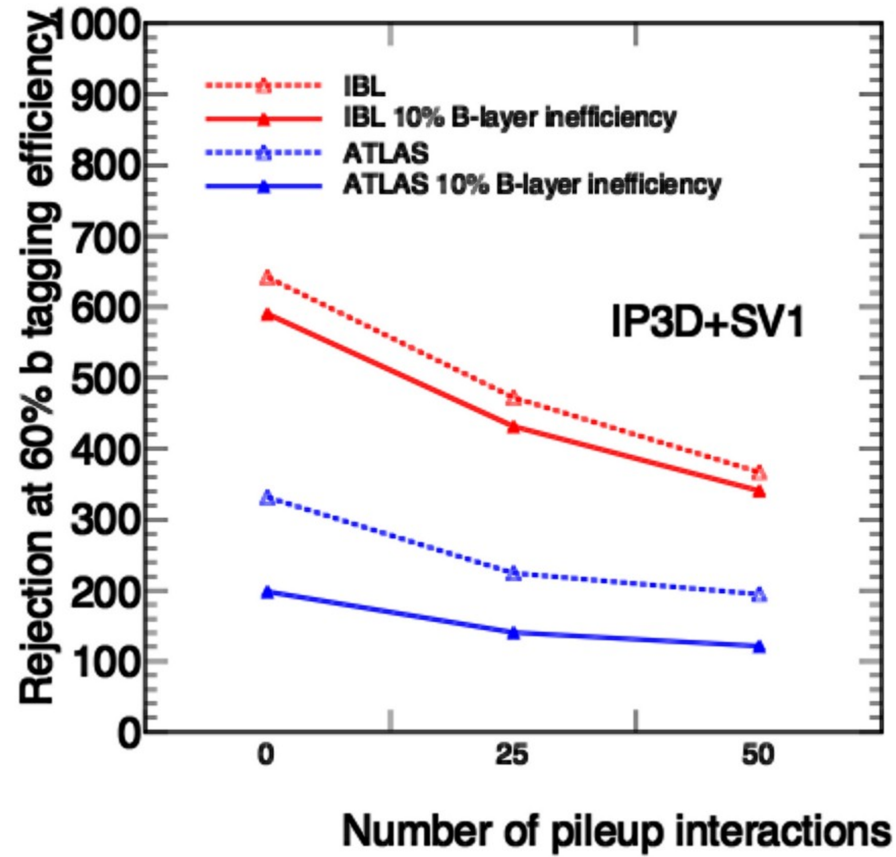






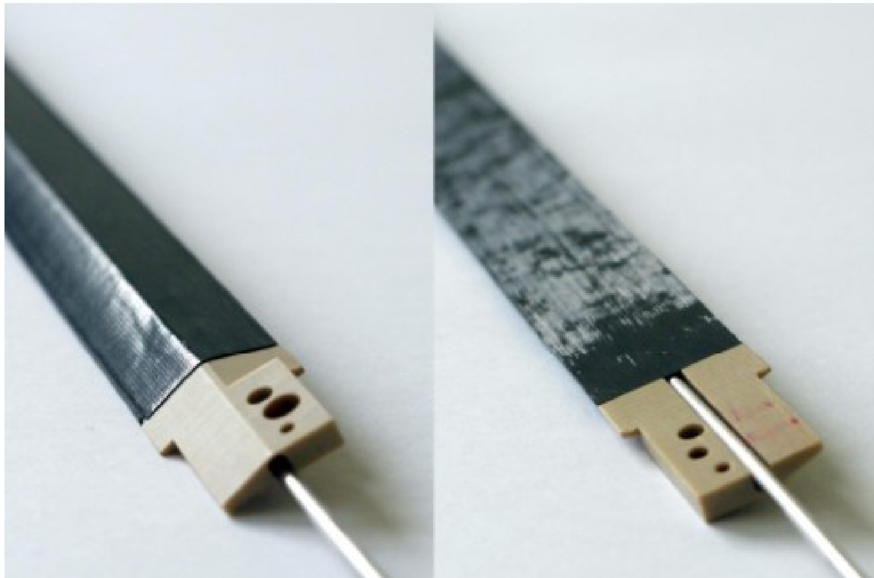
IBL advantage

Selected plot
From TDR



IBL Status

- Stave mechanics final. Focus on building pre-production prototypes
- Sensor fabrication in progress
- Production readout chip submission imminent
- Life size installation mock-up advanced
- Full size CO2 cooling plant being commissioned on surface
- System test including services this fall.

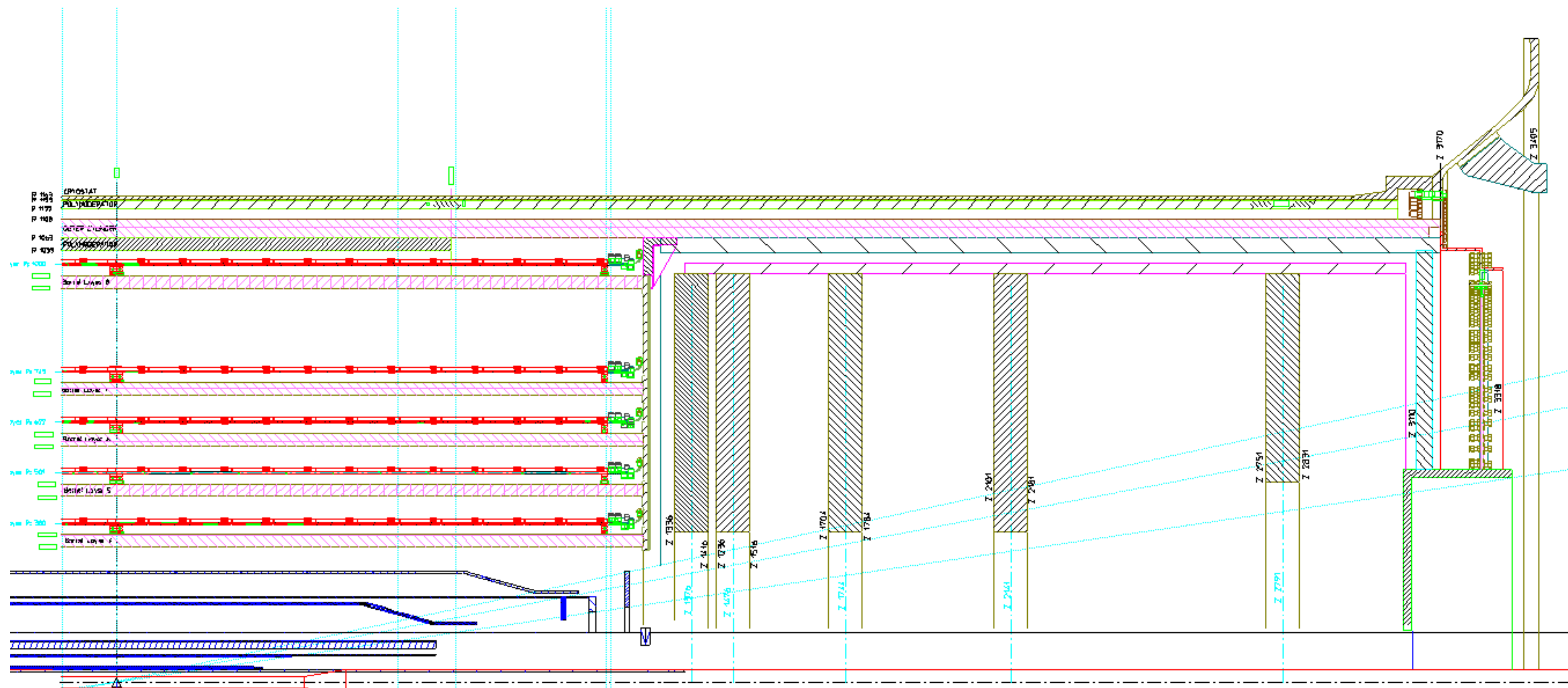


the final stave design is:

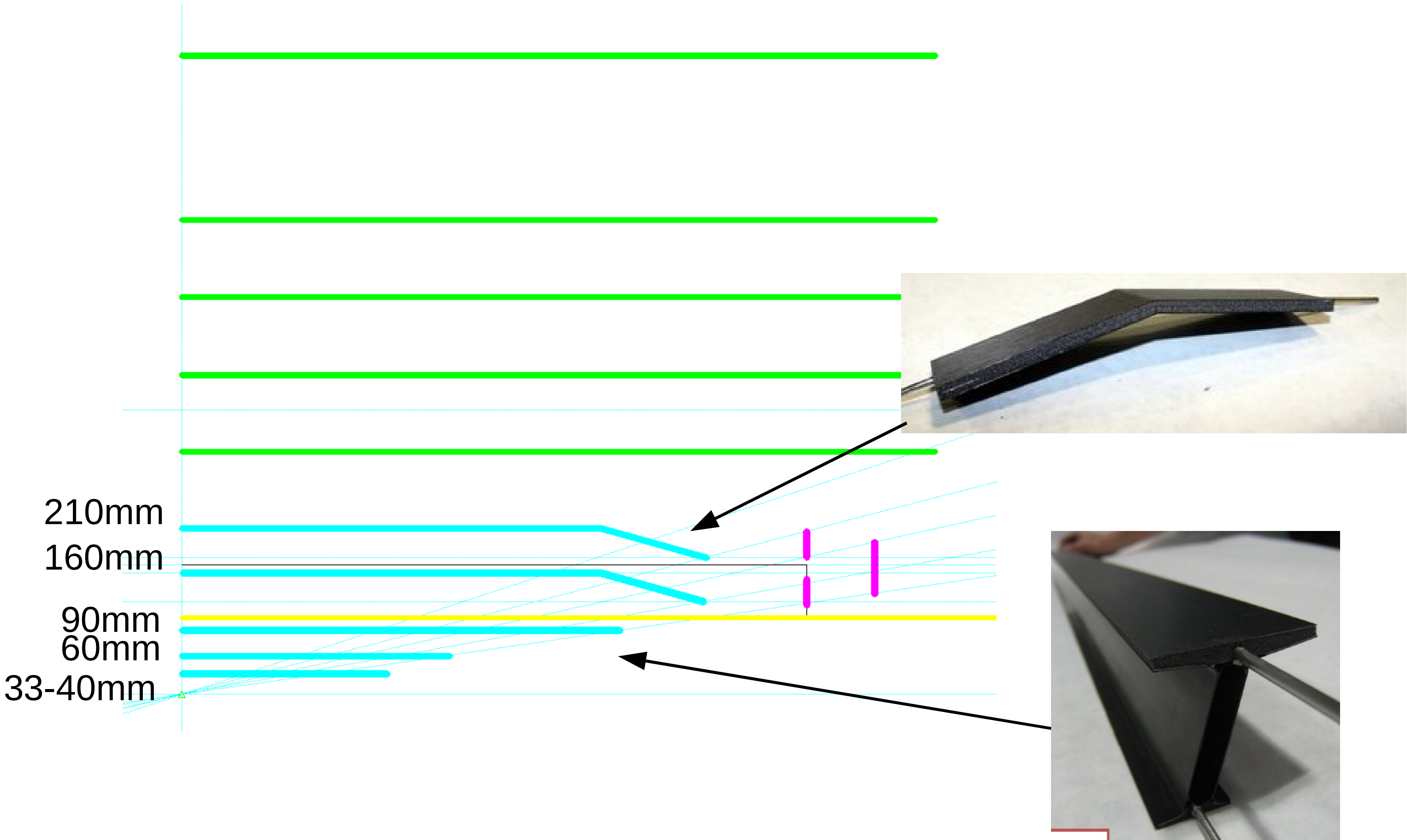
- Pipe ID 1.5 mm
- 3 layer (0/90/0) face plate
- EOS and Central Peek supports
- Flex fully glued on the Omega
- Short stave for loading (1300 mm long) which permit loading @ UniGe

New tracker for High Luminosity LHC

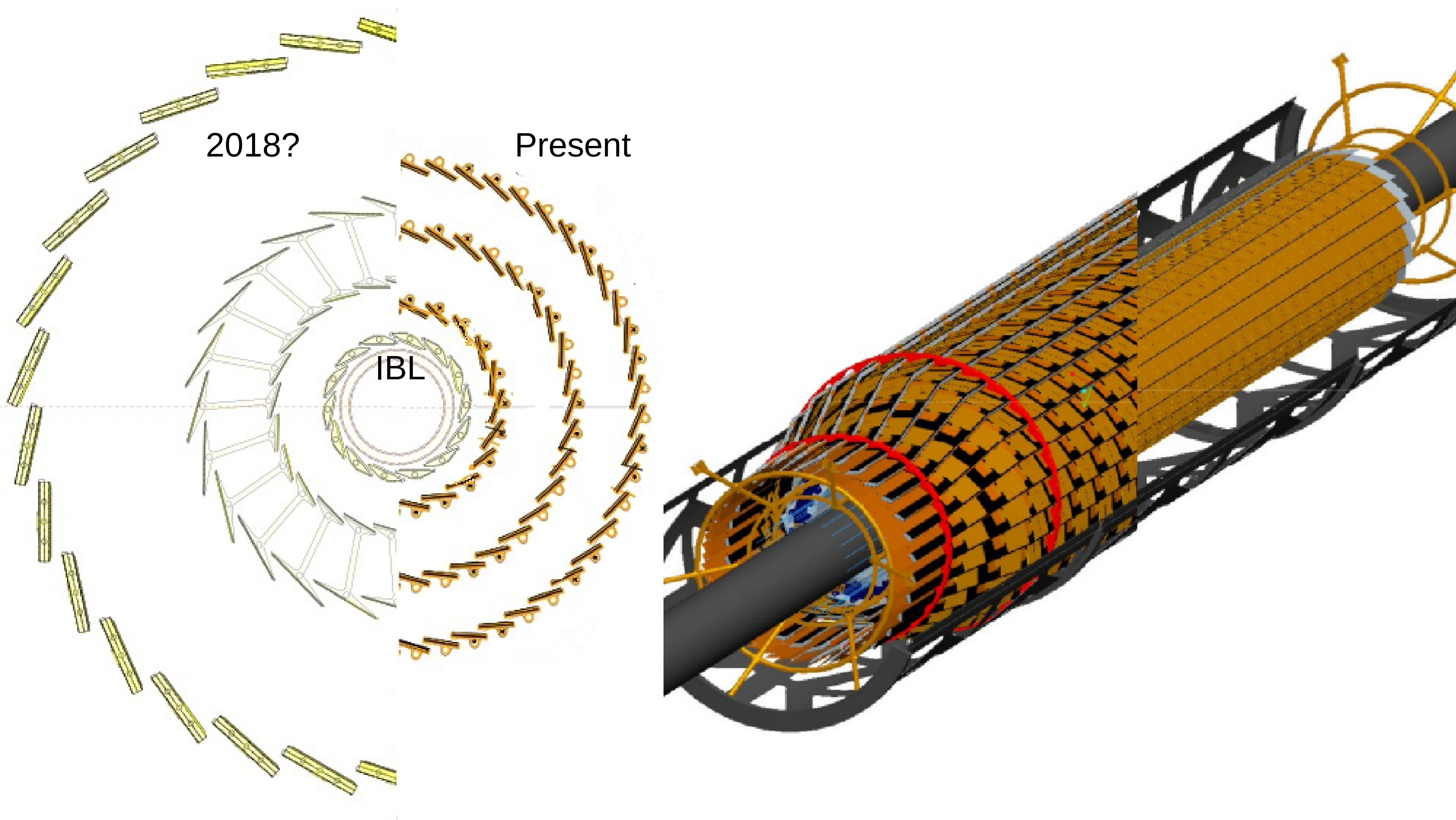
- Layout studies and component prototyping have been on-going for several years.
- Designs are fairly detailed in order to understand requirements and have realistic simulations
  - But this does not mean final choices have been made



Upgrade pixel sample layout



Possibility of staged deployment- early pixels



2018 deployment?

- Not clear today if this is necessary for ATLAS
- Depends on
  - Evolution of luminosity and bunch structure
  - Evolution of installed detector
  - Potential gains to physics program from
    - Lower mass
    - Higher granularity
- Studies ongoing
  - Expect to make a decision by 2013

Conclusions

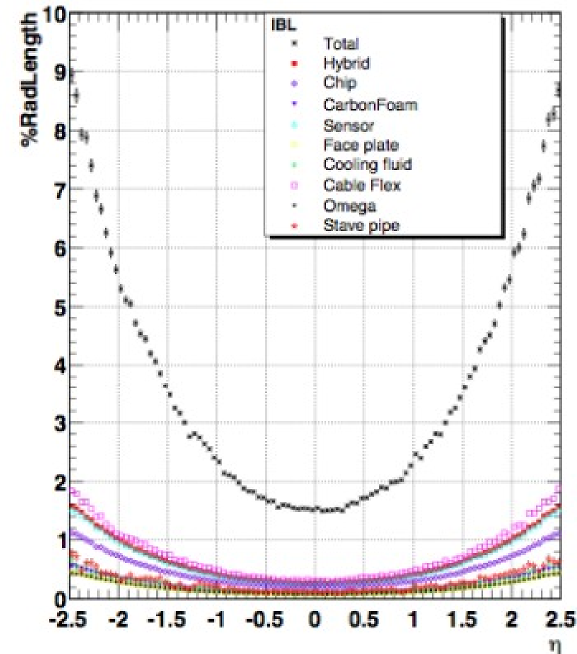
- Pixel technology development has been made a priority
- Several advances are ready today and will be deployed in IBL (2013)
  - New FE-I4 chip
  - New sensors
  - Low mass foam
- Further advances will be ready for 2018 deployment if needed
  - Low mass i-beam and bent stave structures with integrated services
  - Lower cost per unit area (chip, sensors on 6" wafers, faster bump bonding)
  - On-stave power conversion
  - Did not talk about others: low mass high speed cables, DAQ, etc.
- Even further advances ready for HL-LHC – no time to cover
  - Further chip generation beyond FE-I4 (higher rate and radiation)
  - Even more radiation hard sensors
  - High speed communication, DAQ, etc.

BACKUP

IBL mass

IBL integration: Material budget

- Task force in place to monitor actual X0 during construction
- Went from 1.5% (TDR) to 2.0% -> now go back and save material
- Aim on saving X0 now (within reasonable engineering limits)



Present status with conservative material thicknesses:
(perpendicular incident, smeared over active surface, average over stave length $\eta<3$)

Beam-pipe : 0.5848%

IST : 0.2151%

Staves : 0.6628%

Modules (sensor 300u, FE-I4 250 u): 1.1395%

Total IBL (IST+staves+modules) : 2.0174%

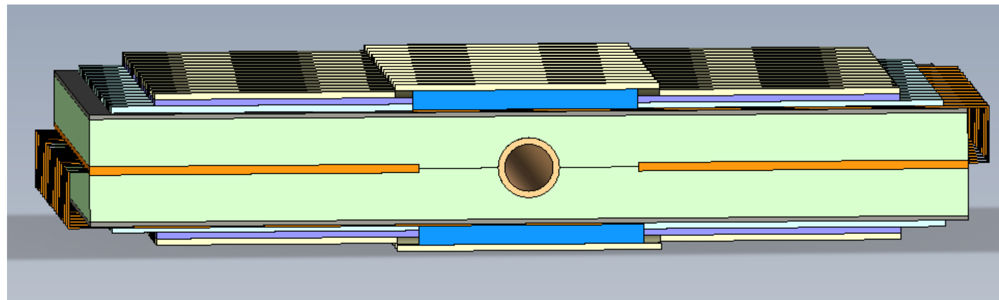
Services : ~1%

Potential Savings	
Stave: 1.5mm ID pipe	- 0.05% to 0.1%
Modules: 230um sensor and thinner grease	- 0.1%
Modules: 100um FEI4 (150um under test by IZM right now)	- 0.18%
Total savings to target	**-0.3% to -0.4%**

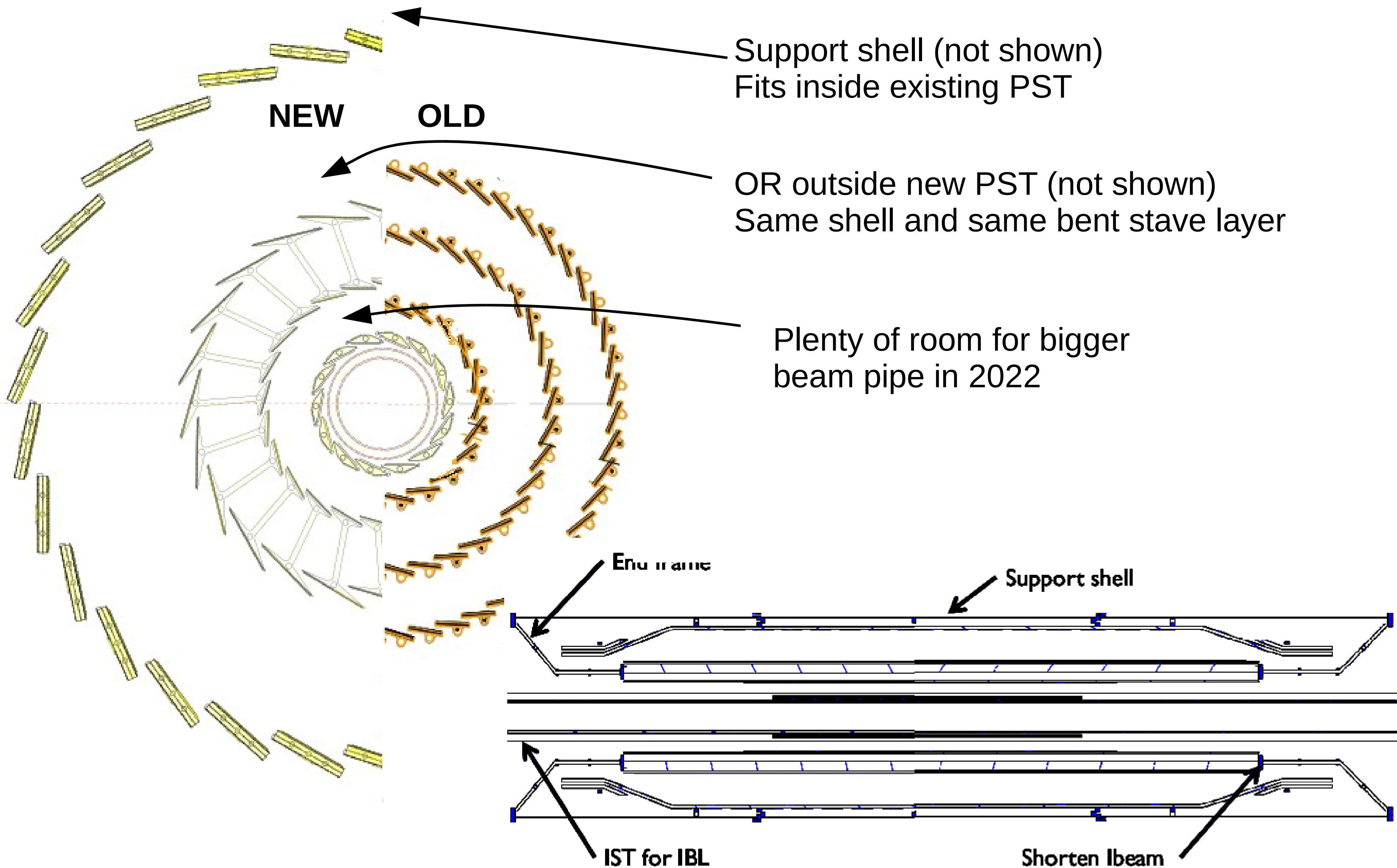
H. Pernegger/CERN Vertex 2011 21

Integrated stave mass

- Radiation length estimate based on measured weights of most recent prototype (pixel outer stave) is about 0.33% per layer for mechanics+cooling pipe.
- Does not include: modules, cables, global support, coolant
- Comparable value for IBL is 0.45%
(higher tube to area and cables to area ratio)



Maximized outer layer radius

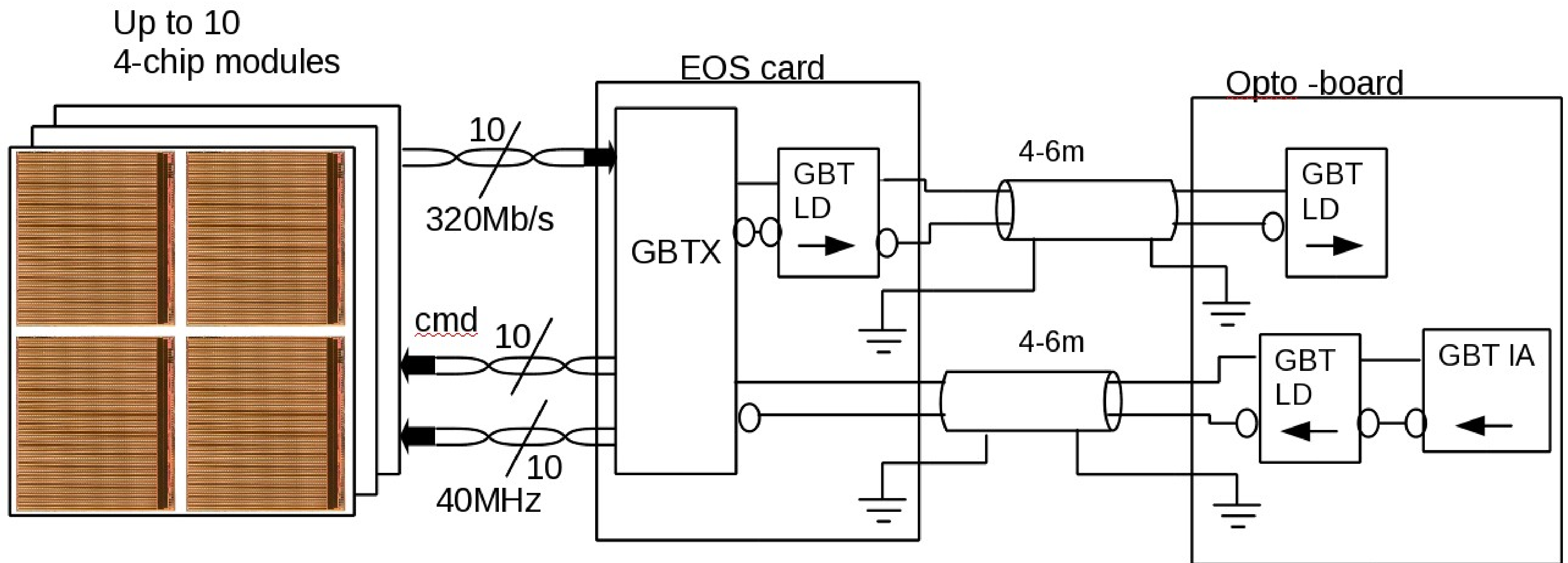


Impact of different R&D areas

(Most development is not ATLAS-specific and plenty for work from outside ATLAS is included)

Goal	R&D Area			
	FE Electronics	**Mechanics**	**System**	**Sensors**
Lower mass	Lower power, System-on-chip.	Materials, Integration, Cooling.	Integration, Power distribution.	
Lower cost	More channels/chip	Modular assembly	Modular assembly	Larger wafers, Simpler process, Bump bonding
Higher radiation tolerance	Deep submicron.			Rad hard silicon, Other materials.
Higher data rate	Architecture, Deep submicron, 3D		Data transmission. DAQ	

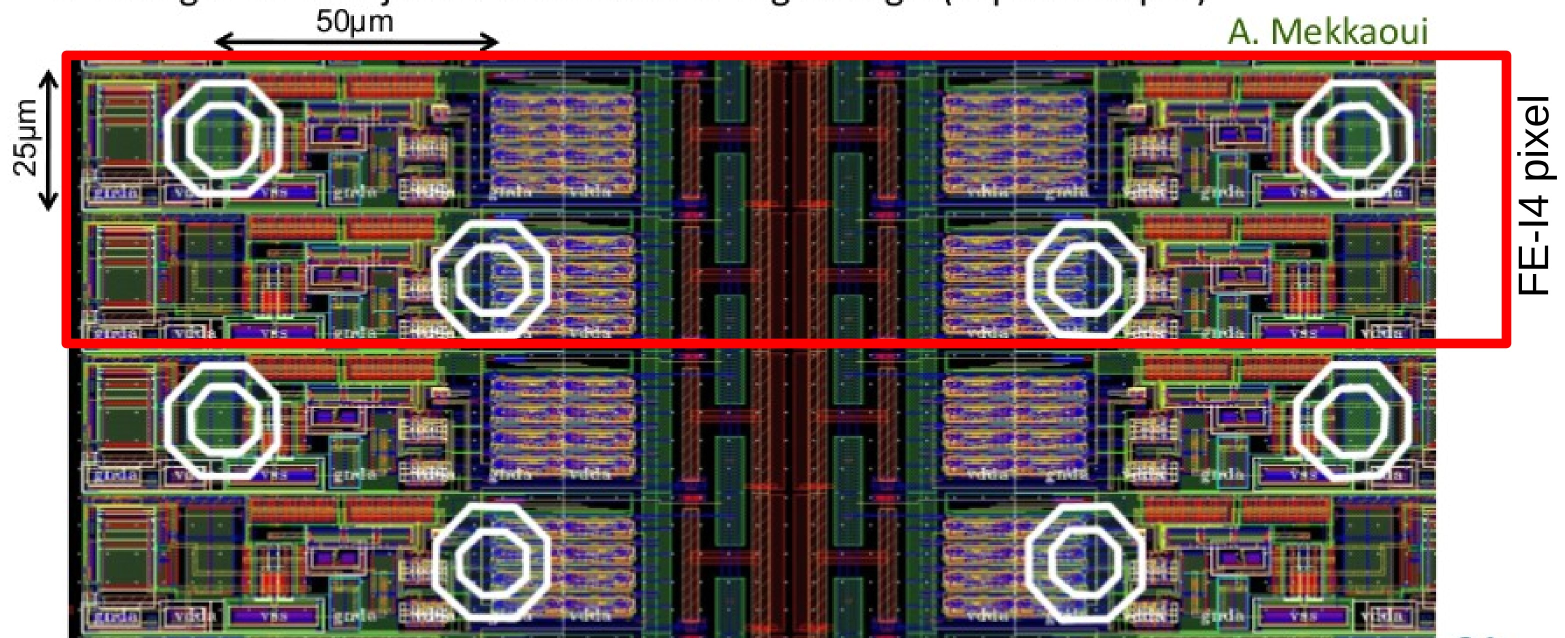
Proposed communication



65nm #1

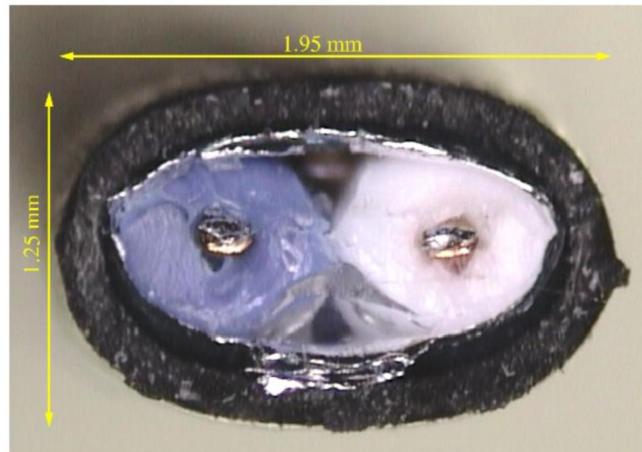
Prototype Analog Chip in 65nm

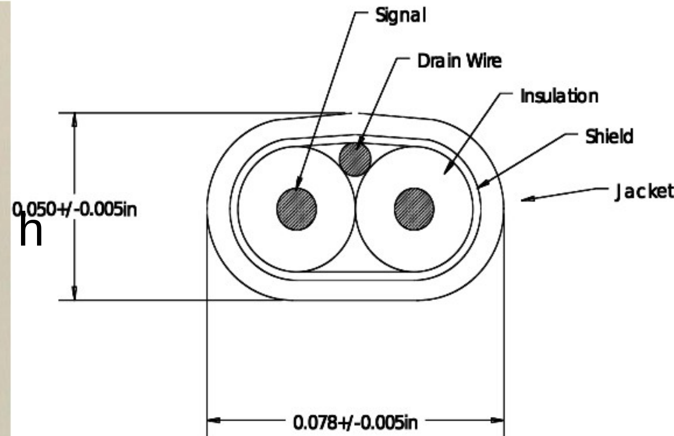
- Factor of 4 in area reduction for digital circuits compared to 130nm
- Idea: reduce analog complexity/performance and compensate with digital signal processing
- Prototype analog chip submitted on June 2, 2011
  - 25µm pitch in rϕ, 50µm bump spacing
  - z length to be adjusted as needed for digital logic (expect 150µm)



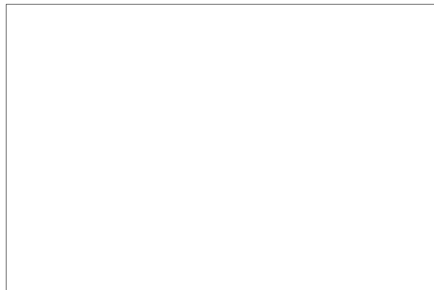
Data transmission and DAQ

Low mass microtwinax for data transmission





GBT SERDES chip



RCE DAQ system in ATCA crates

Installation in Bldg 32

RCE/CIM ATCA Crates

DAQ Switch 48x1GE + 2x10GE

GPN Switch 48x1GE

HP ProCurve 3500yl 2x 10GE X2 SR

Development/Test Machines 2x 1GE NIC

2x Dual-3GHz Xeon

Infrastructure Server for DHCP, DDNS NFS, NTP

PowerEdge 2900

Rainer Bartoldus *ROD Workshop, 19 June 2009* 16