The ATLAS Upgrade Plan (Preparing for the next 2 Decades of Data)

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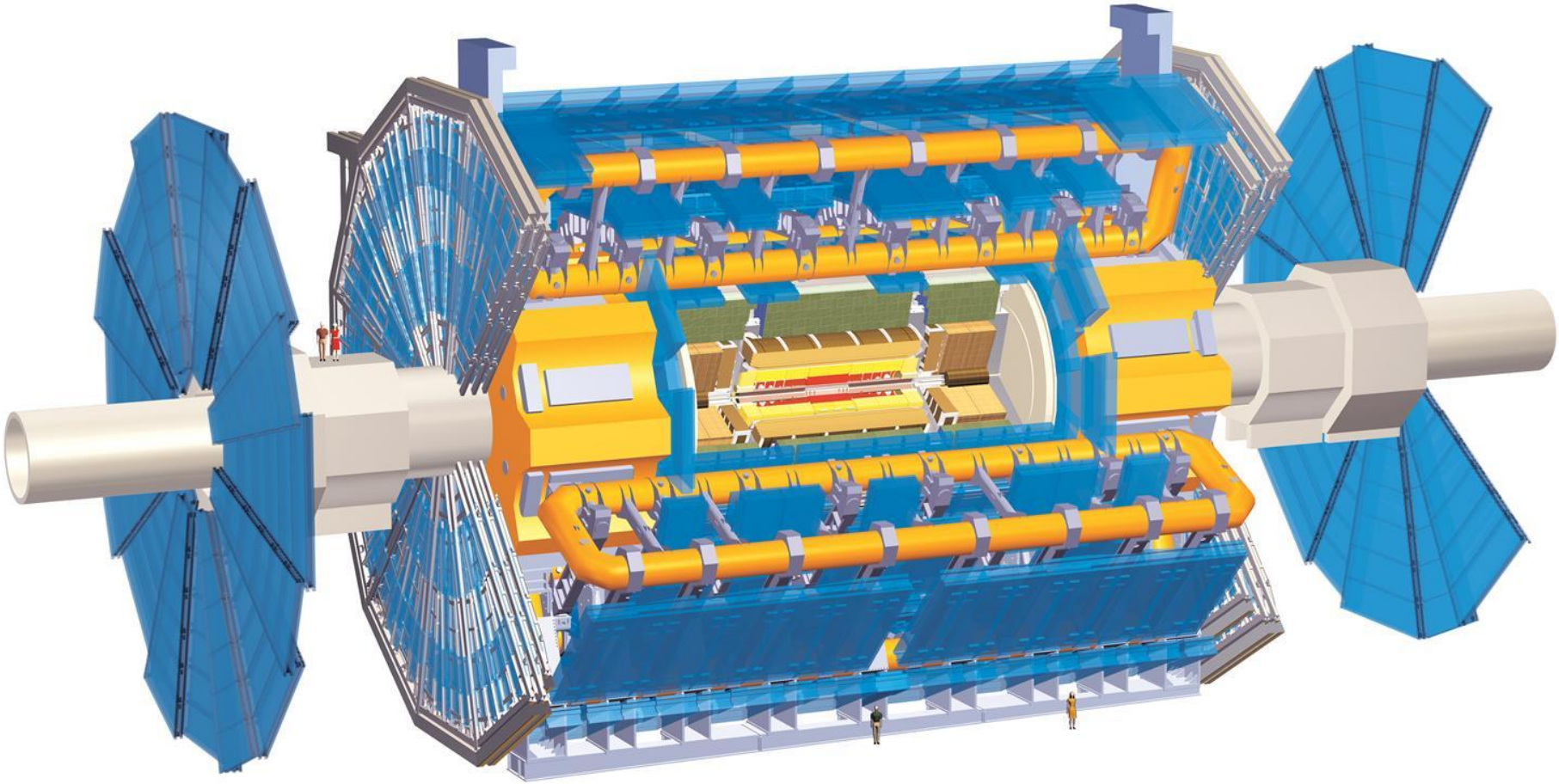
DPF Providence, RI, 9 August, 2011

Outline

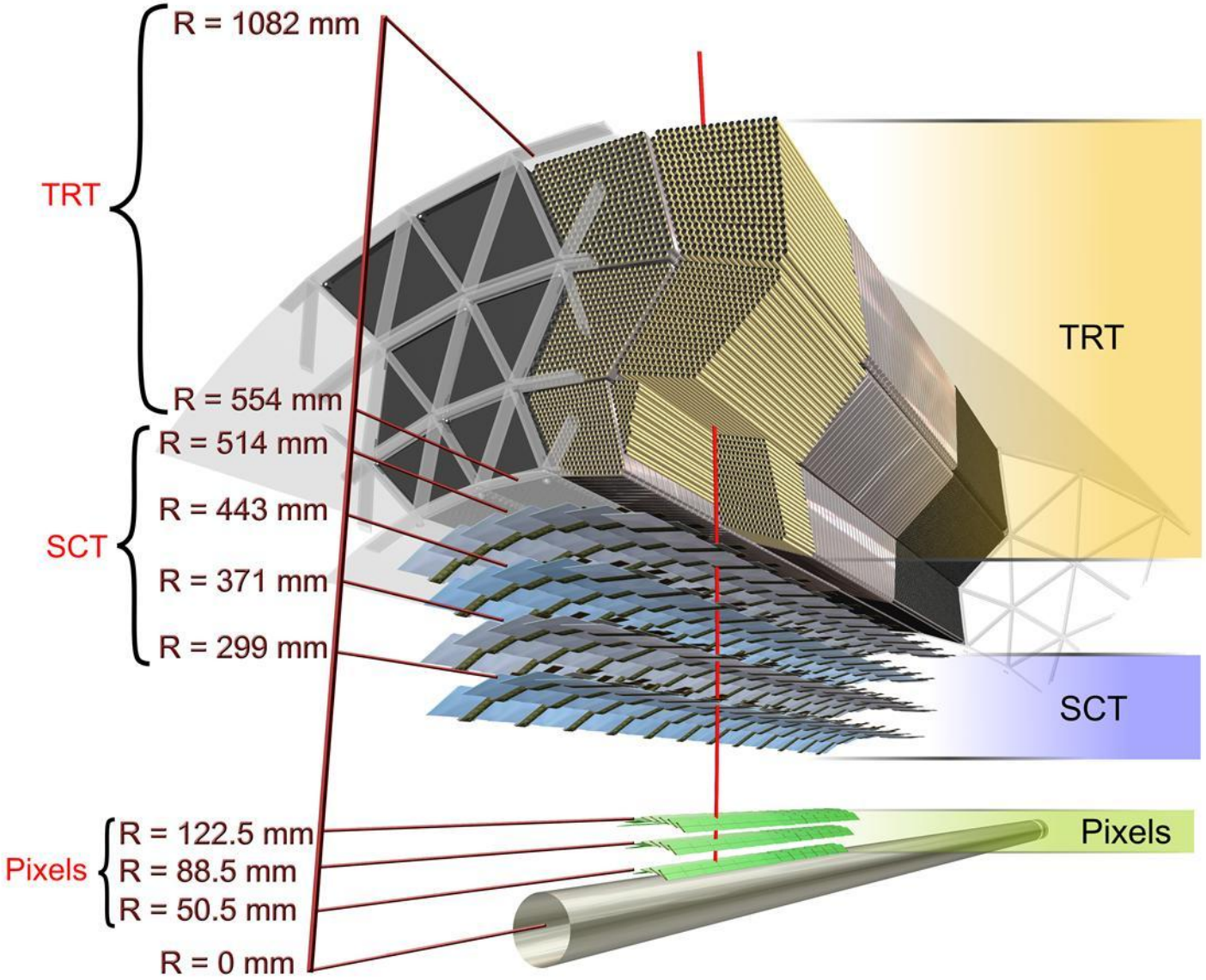
- Context
  - (Very) Brief Description of the ATLAS Detector
  - Possible Machine Schedule and Boundary Conditions Imposed on Upgrade Plans
- ATLAS Upgrade Management Structure
- A Three - Phase Upgrade Plan
  - Phase 0 (2013/14 Shutdown)
  - Phase 1 (2018 Shutdown)
  - Phase 2 (2022?/? Shutdown)
- What I will NOT cover
  - Physics results (there will be plenty of talks this week)
  - Detector Performance (except where relevant to Upgrade Plans)
  - Upgrade Projects described in more detail in this Session (New Pixels, FTK)

The ATLAS detector

- Central trackers in a solenoidal magnet $|\eta| < 2.5$
- EM + hadronic calorimeters $|\eta| < 5$
- Muon spectrometer in toroidal magnets $|\eta| < 2.7$
- Forward detectors



The Inner Tracker at a glance

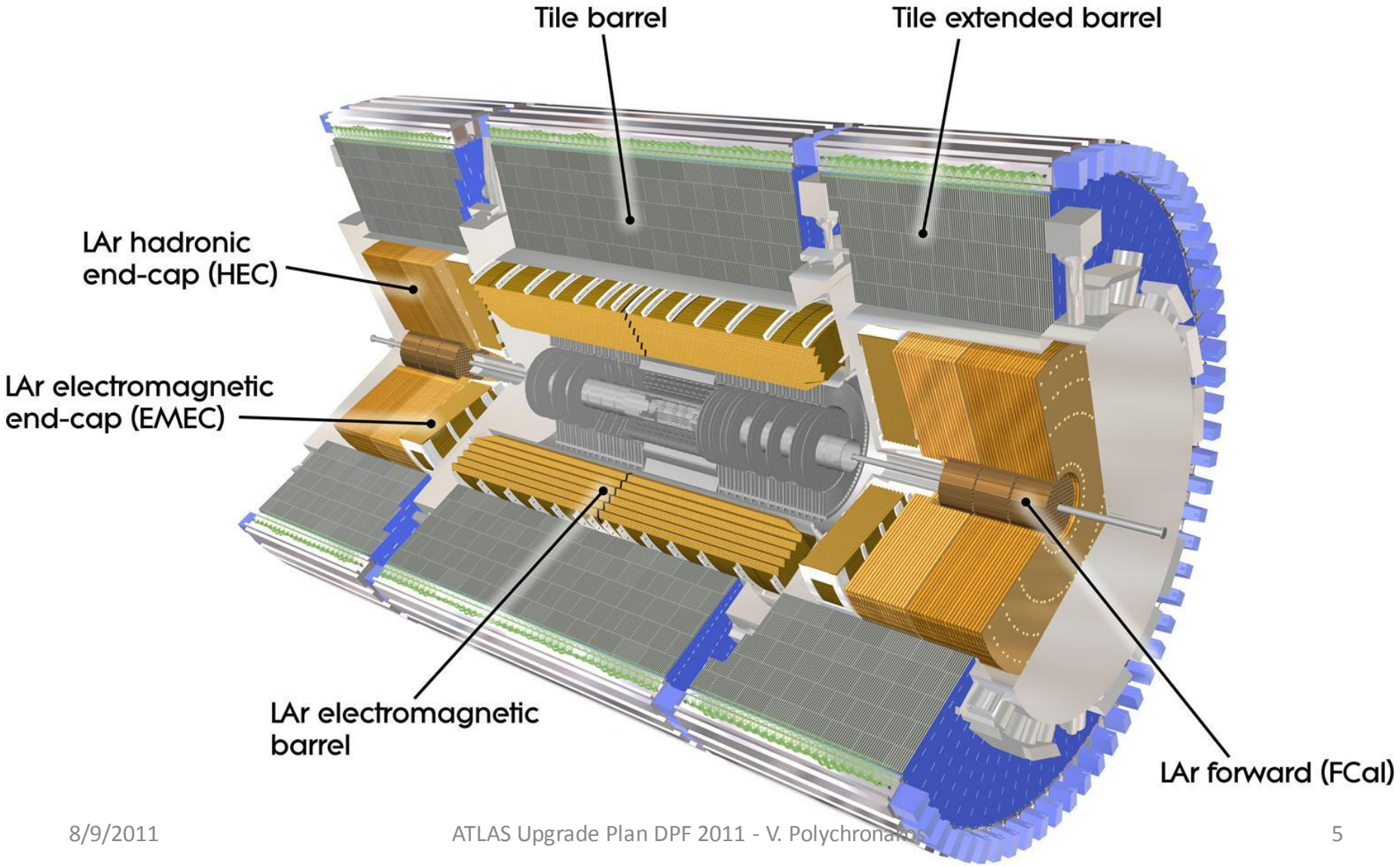


Straw tubes

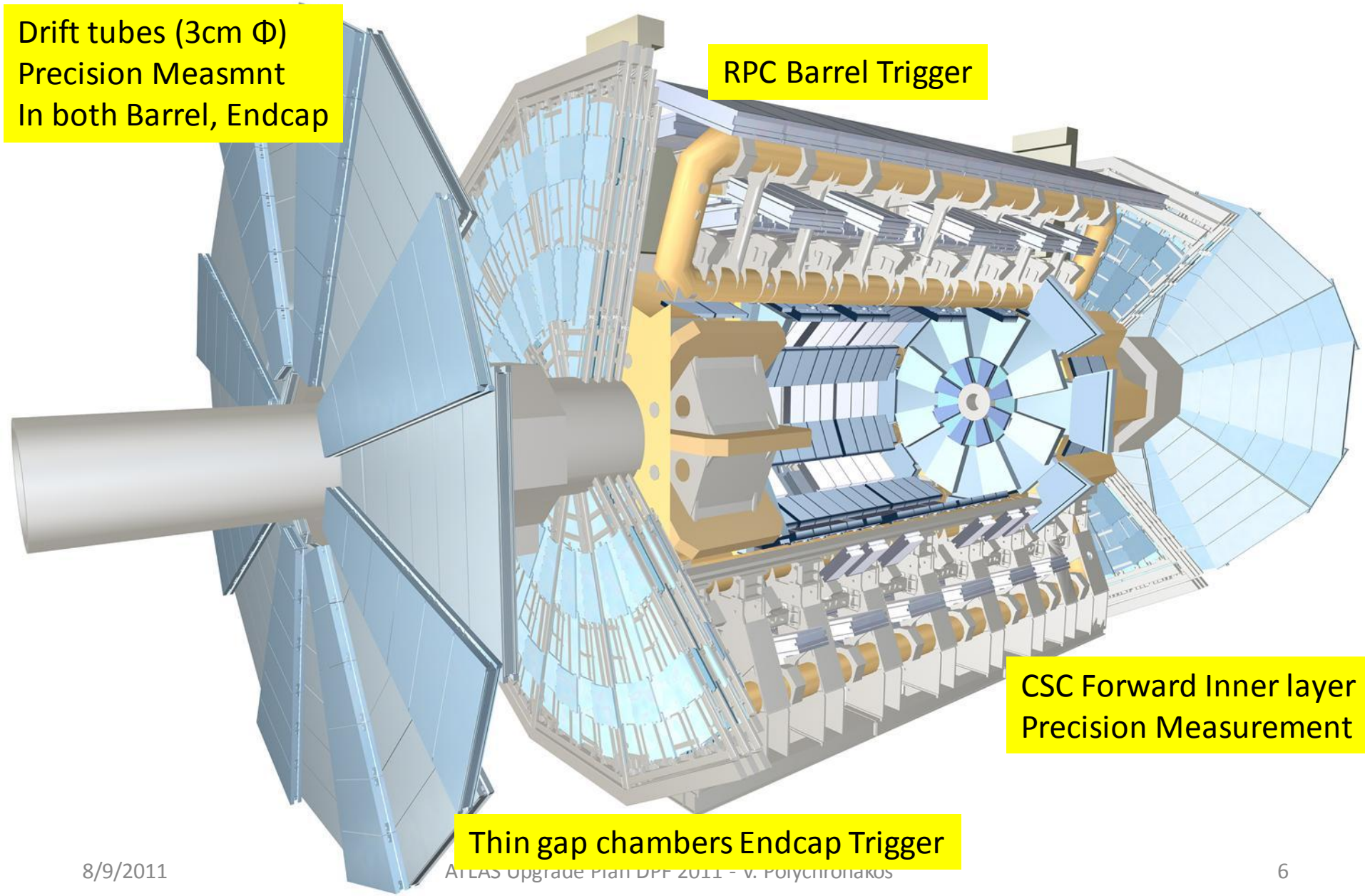
Silicon strip

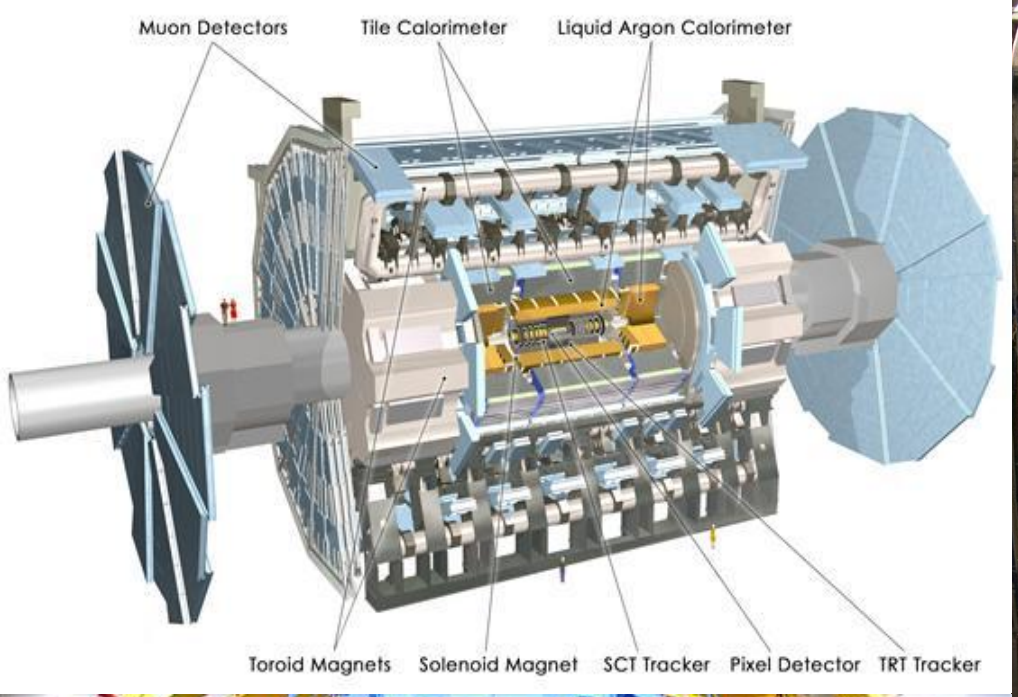
Silicon pixel

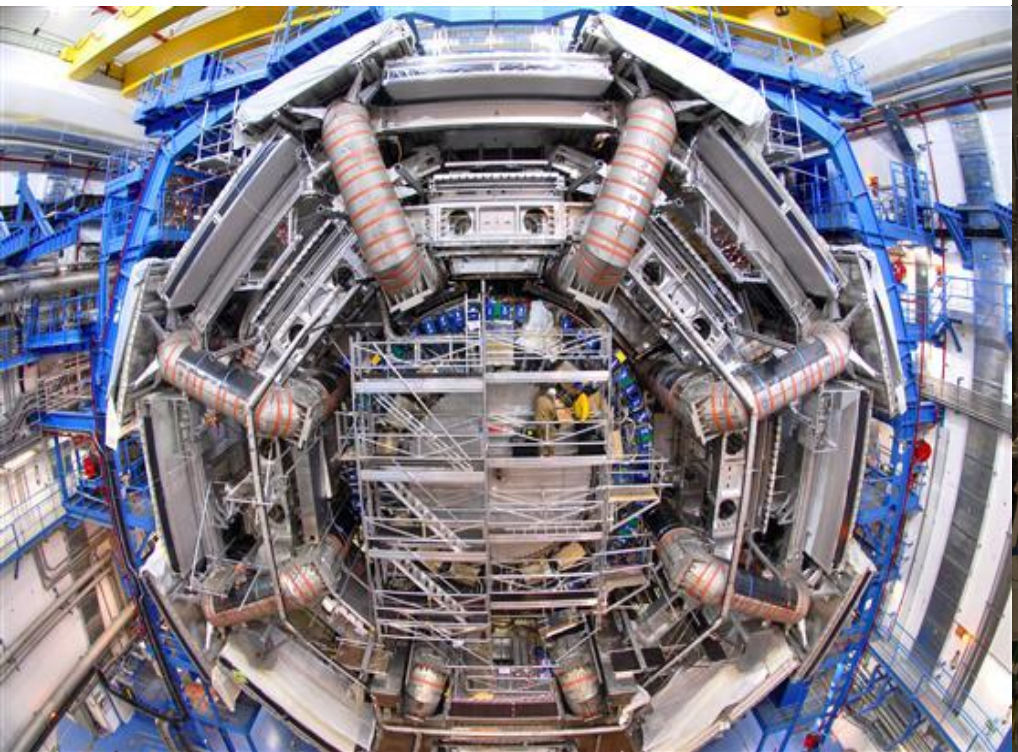
The Calorimeters

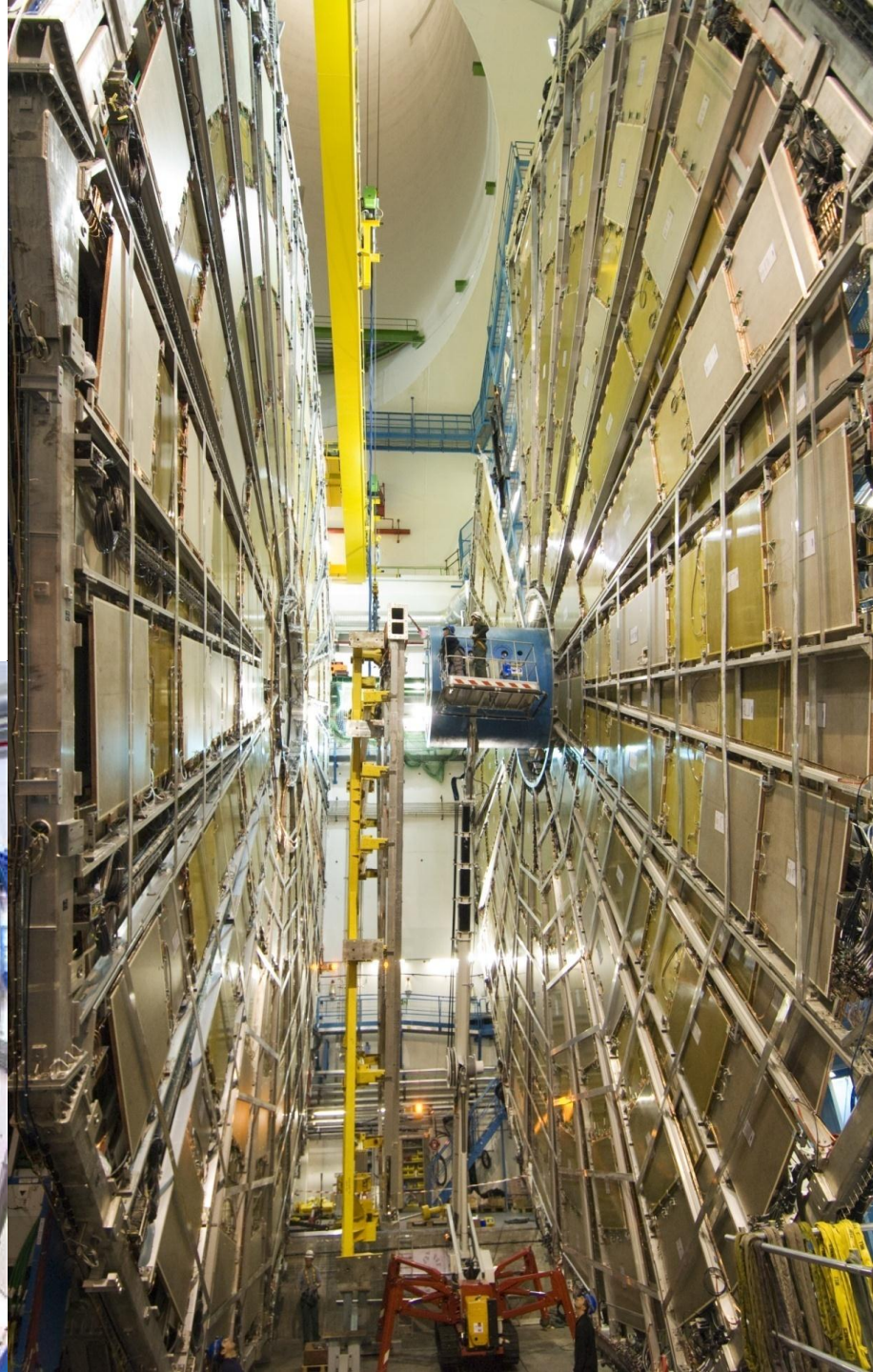


The ATLAS Muon Spectrometer

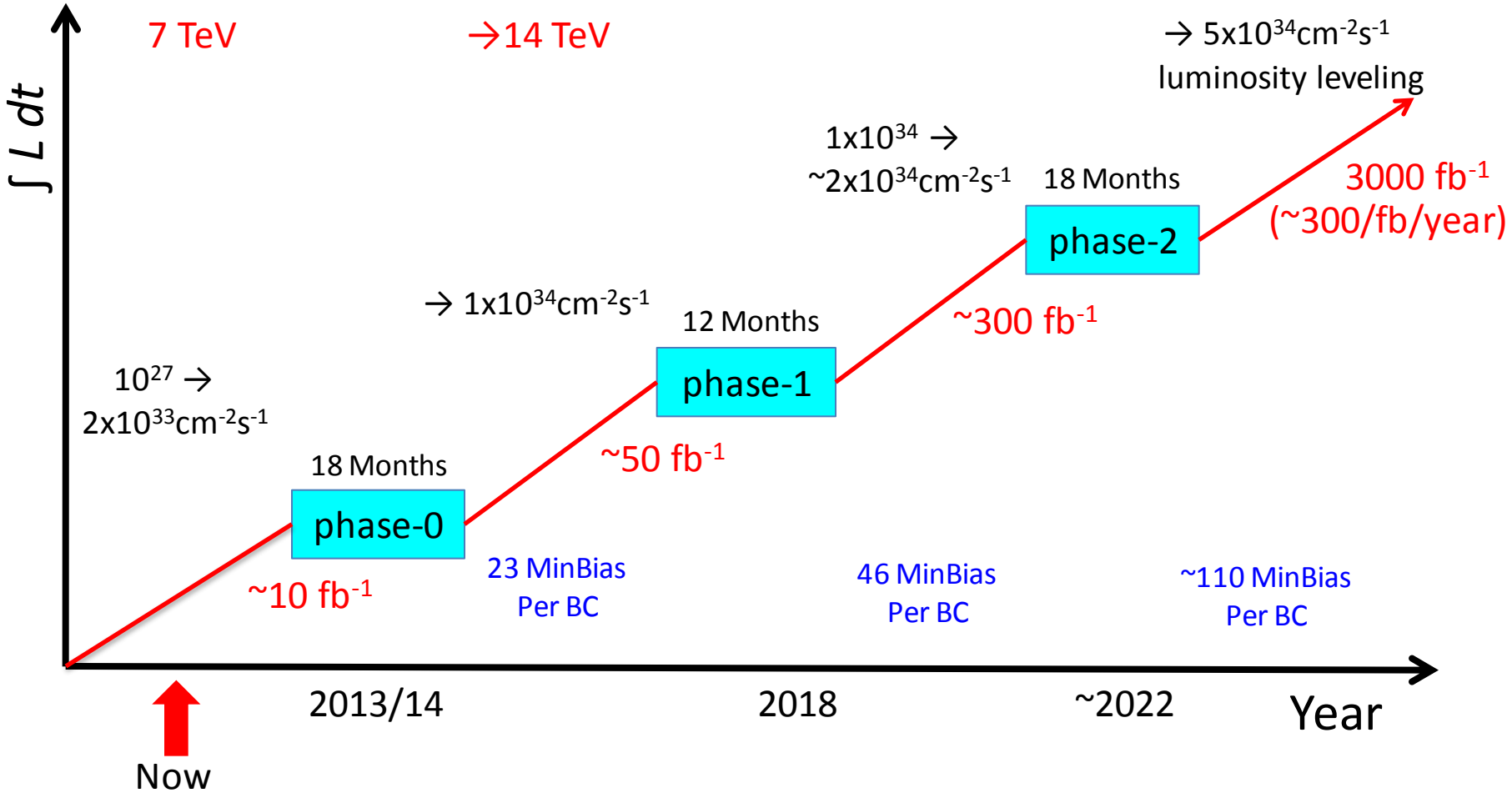



Muon Detectors
Tile Calorimeter
Liquid Argon Calorimeter
Toroid Magnets
Solenoid Magnet
SCT Tracker
Pixel Detector
TRT Tracker

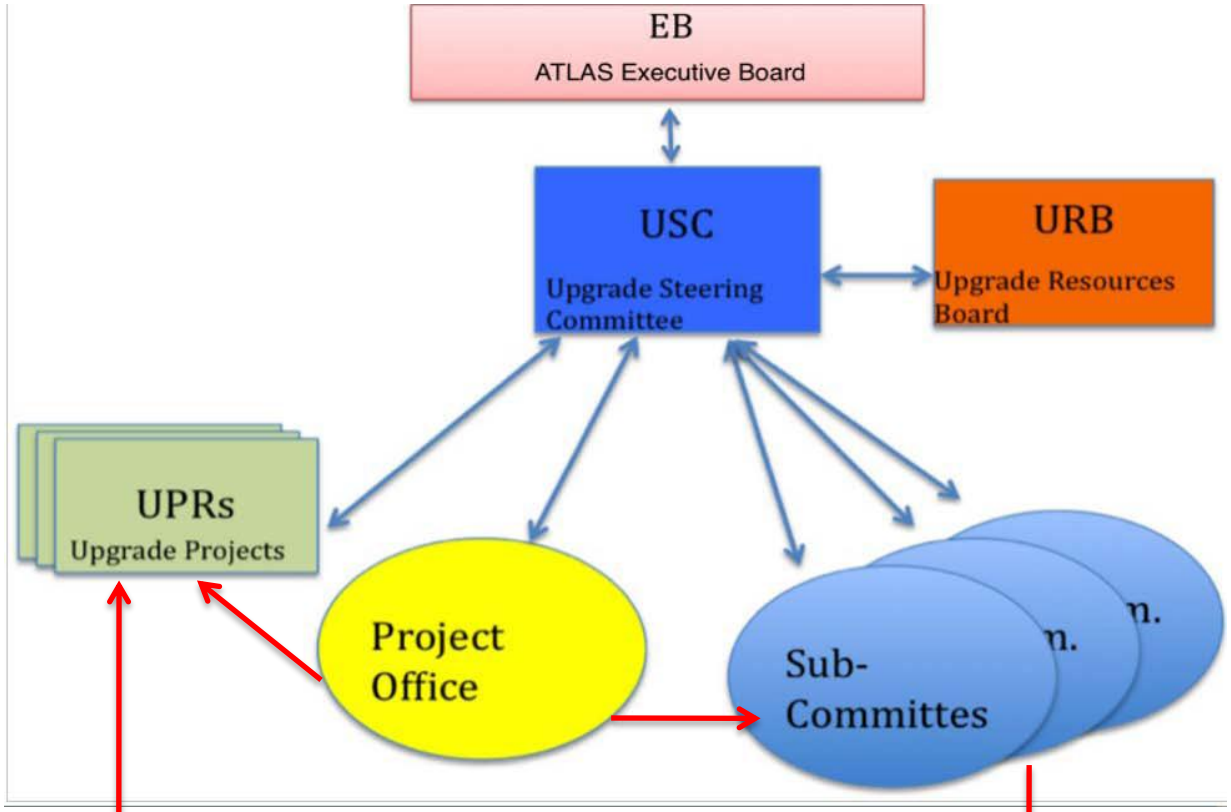




LHC Machine Boundary Conditions, Possible upgrade timeline



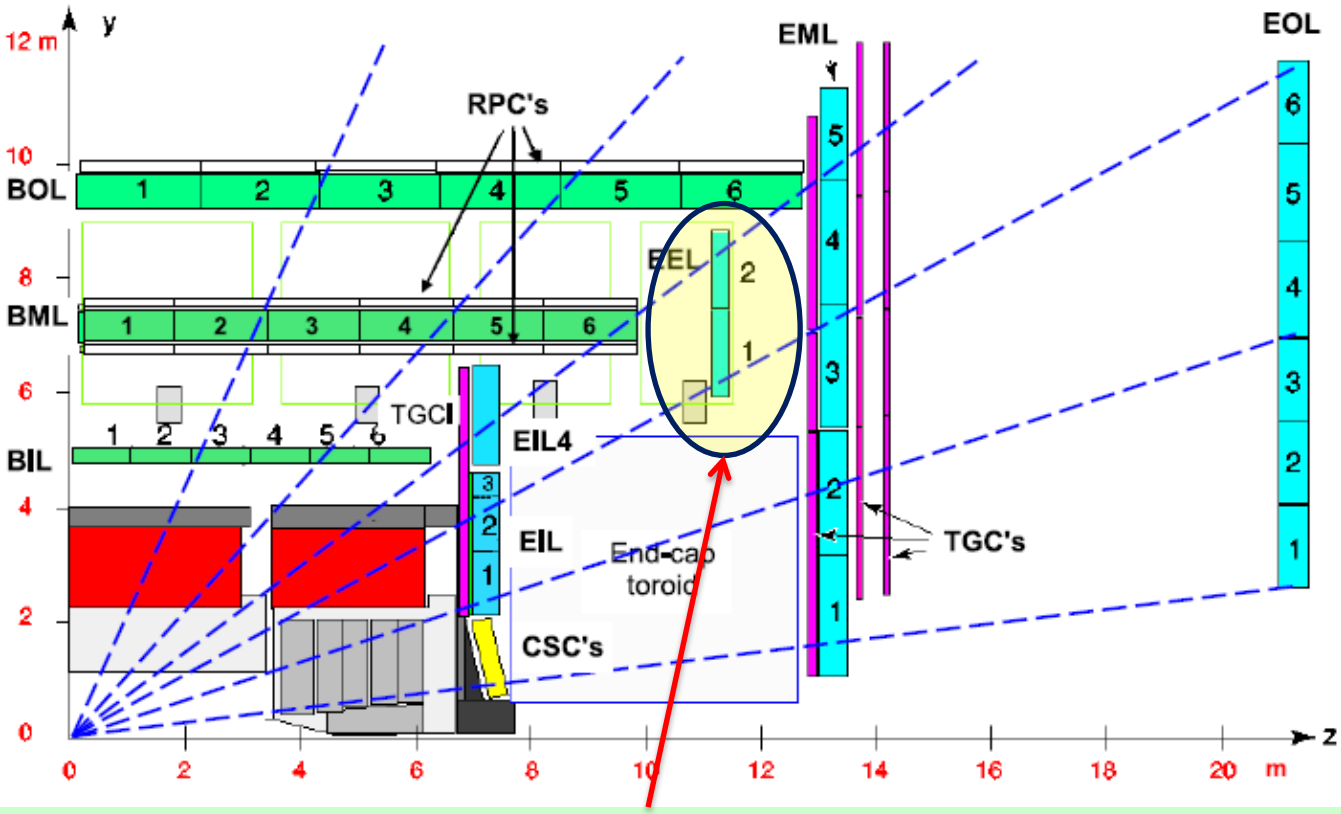
Upgrade Management Structure



Phase-0

- Prepare for operation at full energy (14 TeV) and full luminosity (10e34/sec/cm^2)
- LHC will redo splices, "machine consolidation issues"
- Upgrades and other work foreseen by ATLAS
  - New Al beam pipe to replace steel pipe will reduce background in Endcap Muons
  - Finish Installation/commissioning of some Muon Chambers that were originally staged
  - Repairs where needed and where can be done
- Two Major Projects
  - Insertable B-Layer (new pixel layer)
  - FTK (Fast Tracker to improve Level 2 Trigger)

Muon EE "Chambers"

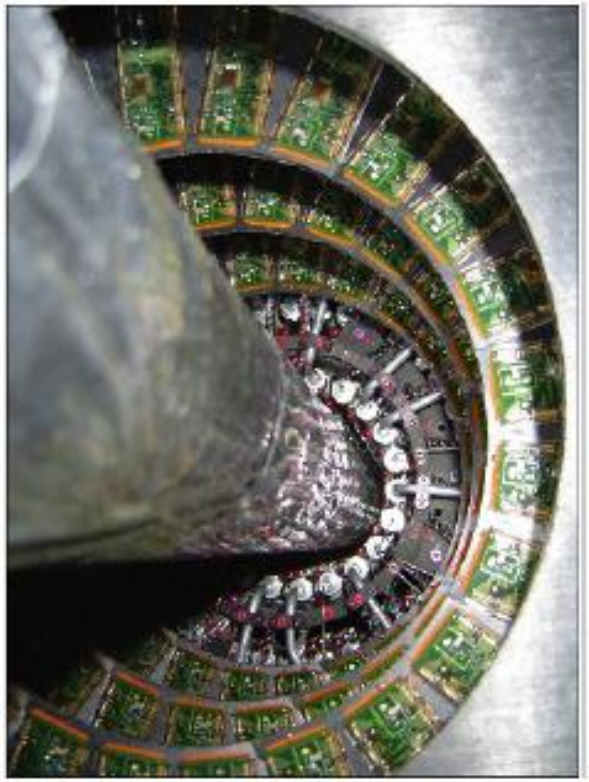


- EE Chambers help muon reconstruction in a weak magnetic field region where Barrel and Endcap Toroids are competing
- Staged originally are now gradually being installed as access permits
- Expect to finish installation, alignment, and commissioning during 2013/14 Shutdown

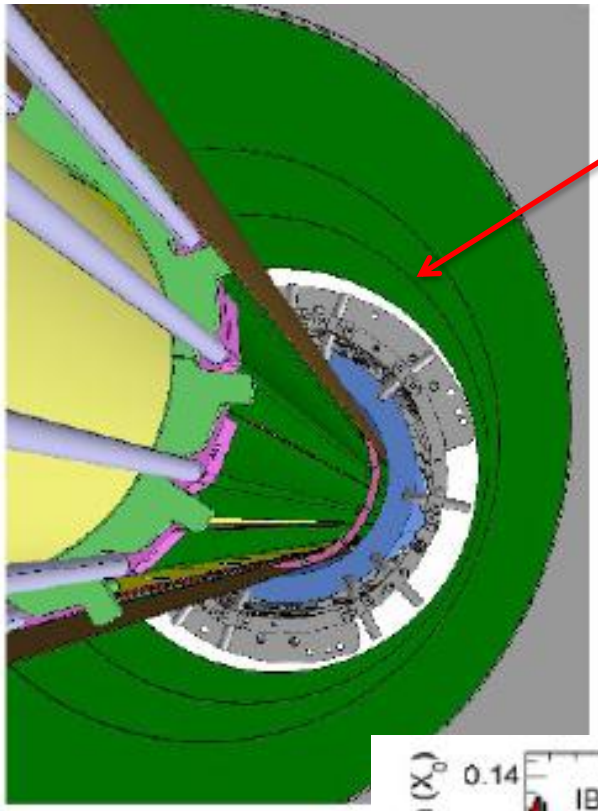
The "Insertable B-Layer" (IBL)

- Motivation
  - Innermost pixel layer (B-layer) is a special layer
  - Secondary vertex identification and B-tagging/light flavor jet rejection.
  - Must assure robust operation in spite of efficiency loss due to a variety of reasons
    - Component lifetime.
    - Radiation damage mainly after 2018-19.
    - Data rate, especially if bunch structure remains at 50 ns
- Difficult to impossible replacing it without risking damage
- Instead insert new layer in the space of the current beam pipe (reducing the pipe's diameter)
- Increase physics performance with low material budget, smaller pixels (250 micron instead of the present 400) at smaller radius (3.2 cm instead of 5 cm)

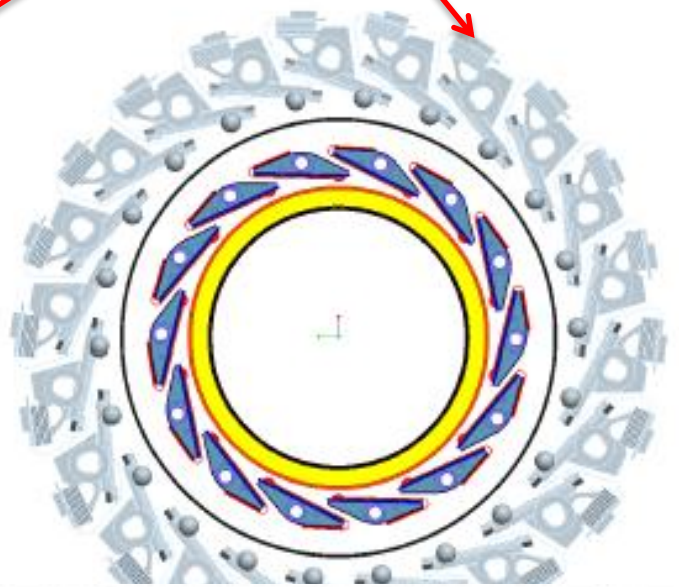
The Proposed Scheme

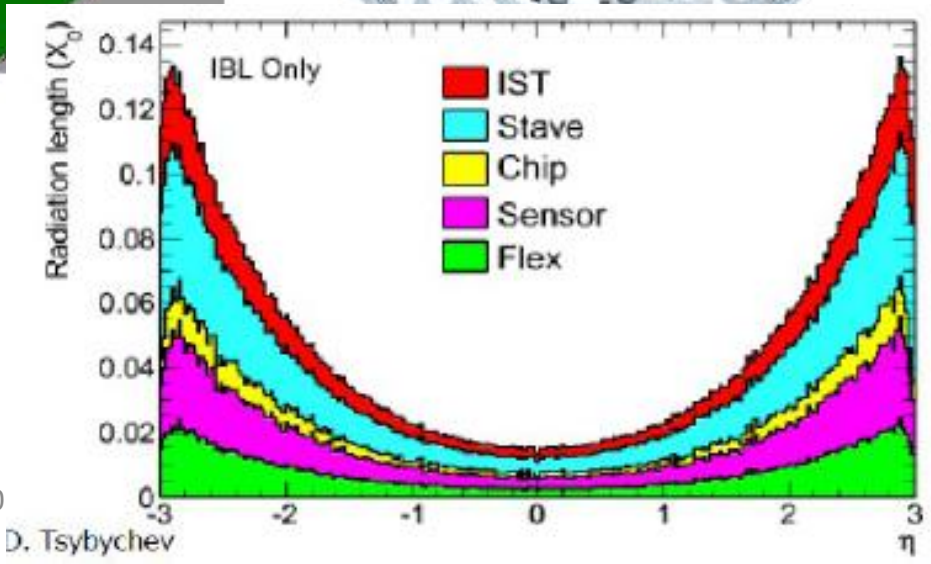


The pixel Detector now



The new IBL

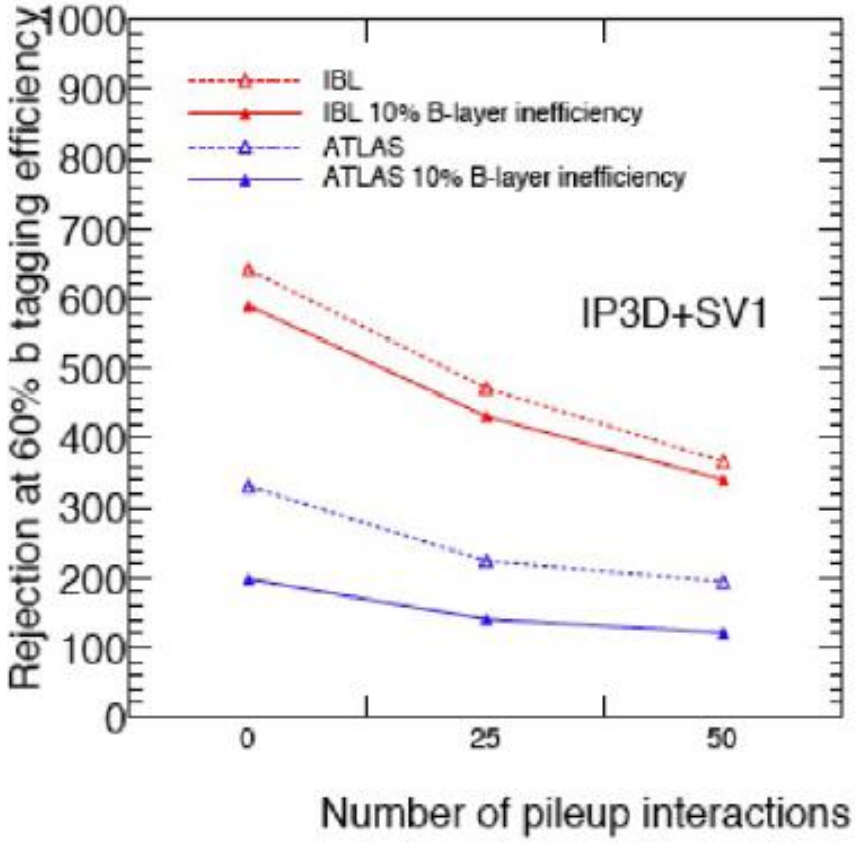


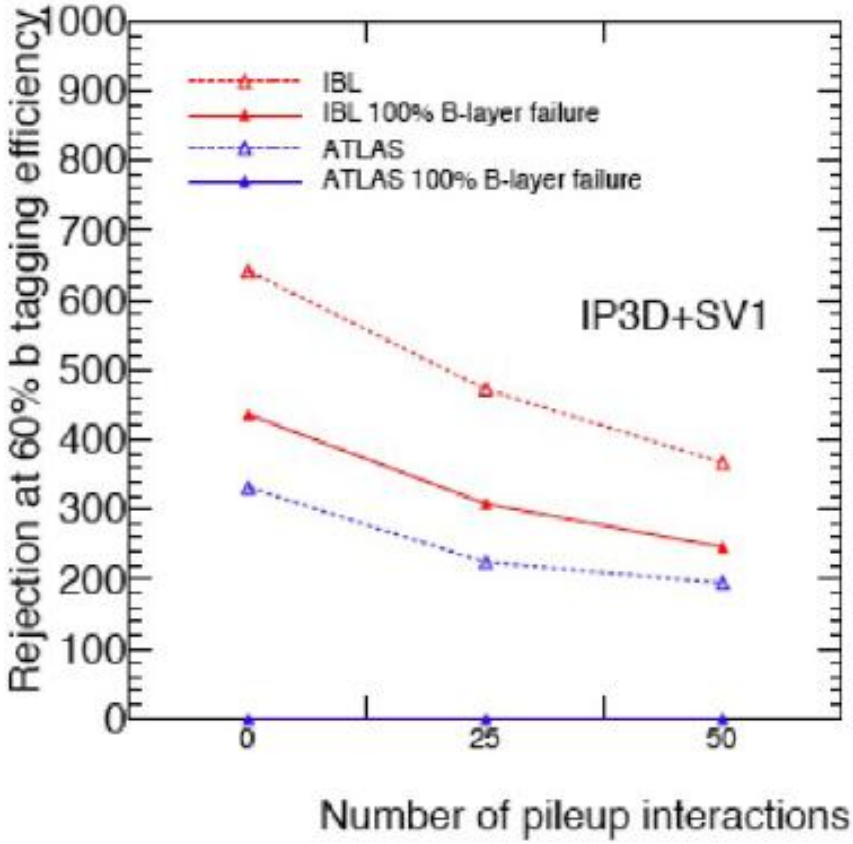


- Adds minimal material (~ 1.5% Xo)
- Mechanics fully defined
- Structure already fully integrated in GEANT geometry model

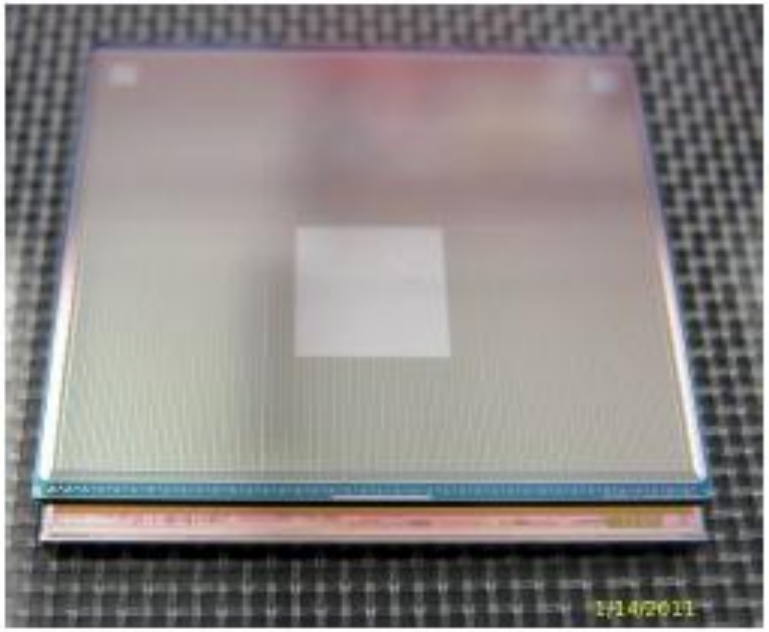
Example of Improved Performance

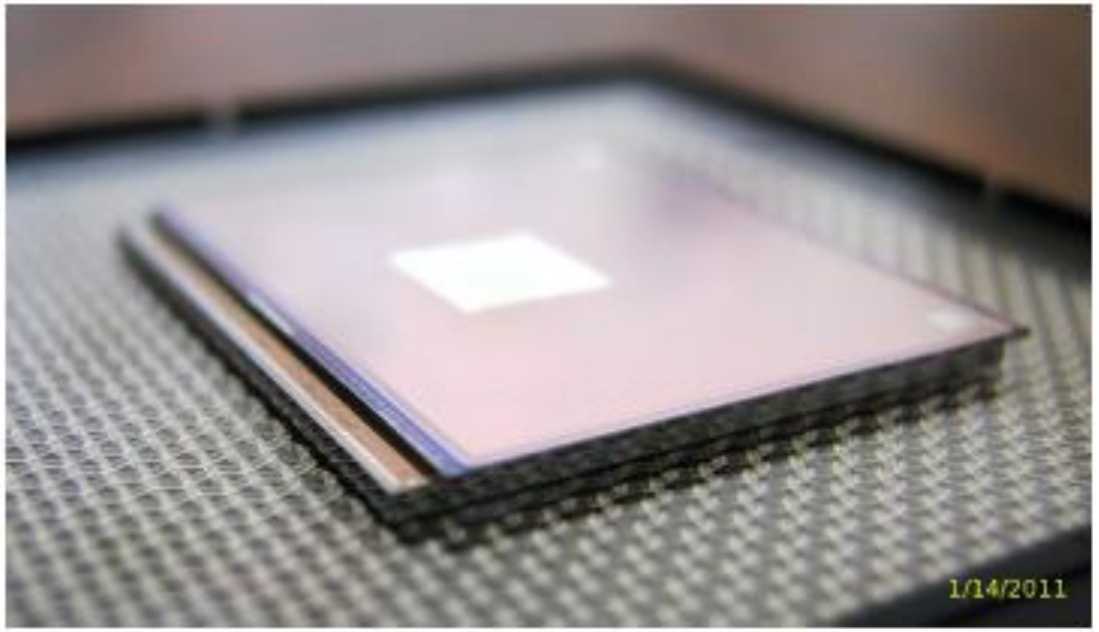
- B-tagging light flavor jet rejection
- Comparison with current detector
- Without and with possible defects and pileup



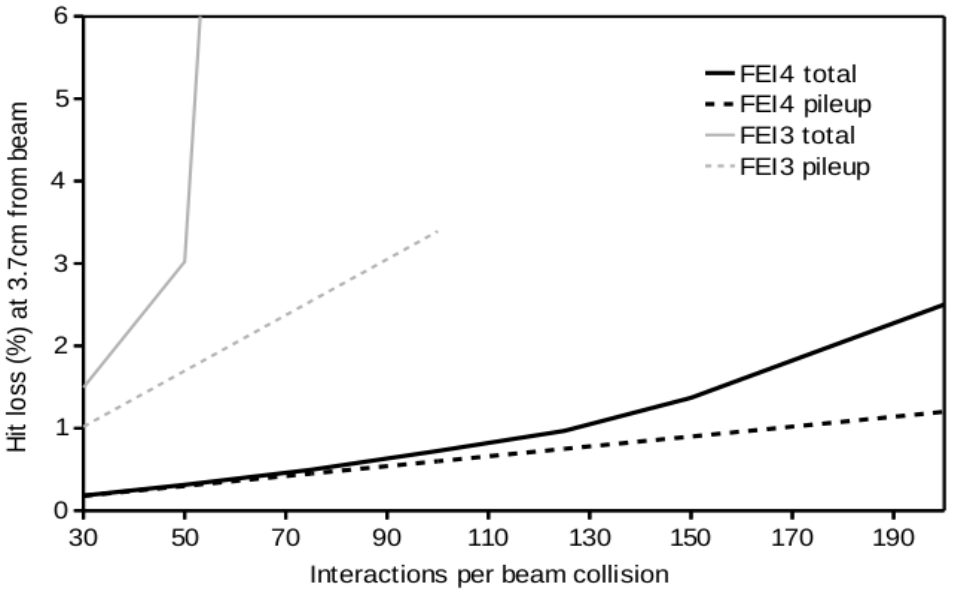


Development of the FE-I4 chip Critical for the Project





- Largest Area Chip ever used in HEP
  2x1.9 cm^2, 26,880 channels
- Bump bonded to sensor
- Reduced assembly cost scaling as 1/Area
- Increased functionality (system on chip)
  - Front end
  - Data formatting
  - Communication
  - Power Conversion



Phase 1, 2018 – Trigger Improvements the Main Theme

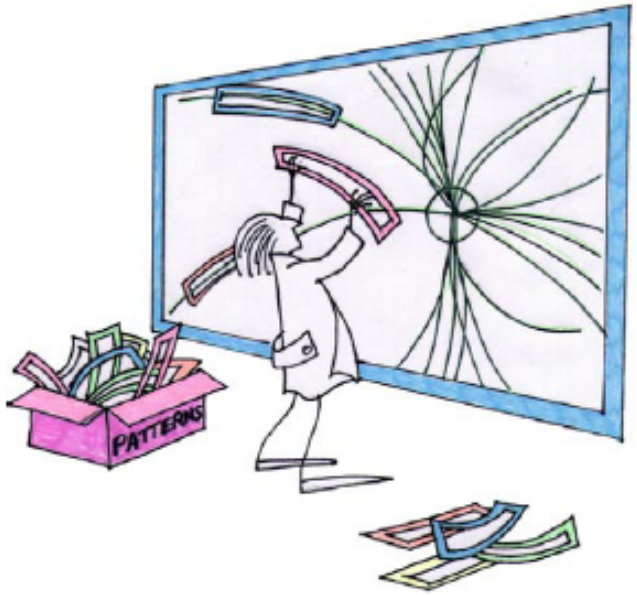
- Fast Tracker (FTK)
  - Use Sophisticated Tracking at the Trigger Level
- Topological Level 1 Trigger for Calorimeter Algorithms
  - Only 1% of EM Triggers are identified as Electrons (most are photons, of course)
  - Use Tracking Information already at Level 1
- Improve Endcap Muon Level 1 Trigger
  - Improve PT Resolution for Sharper Thresholds
  - Eliminate or greatly reduce fake Triggers
  - 90% of 20 GeV PT cut triggers are not associated with track originating at the IP (rejected later at Level 2)
- Possible New Pixel Detector

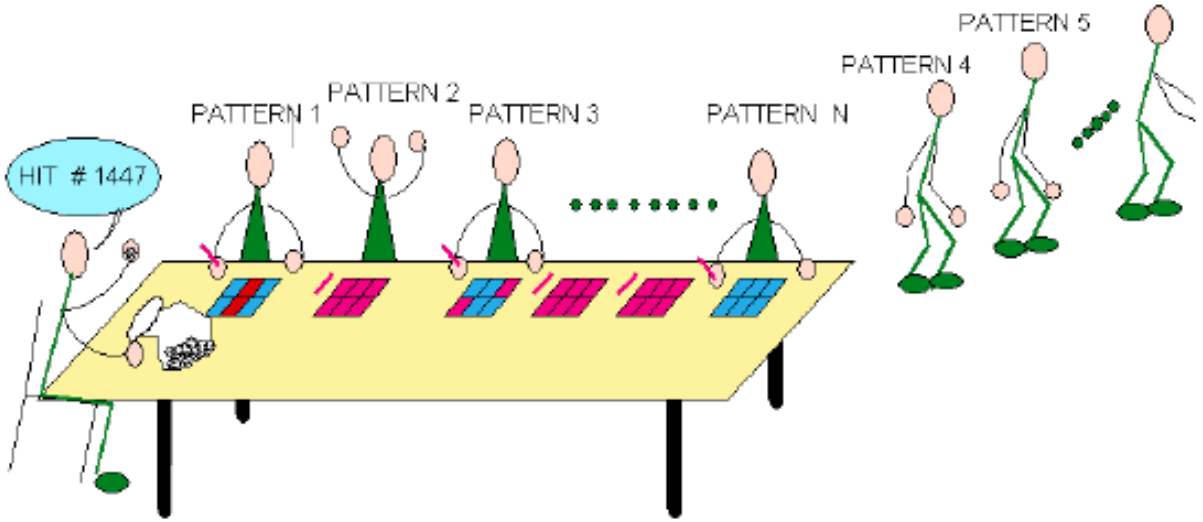
The FTK Project Associative Memories

(From Mel Shochet FTK)

Two time-consuming stages in tracking

- **Pattern recognition – find track candidates with enough Si hits**





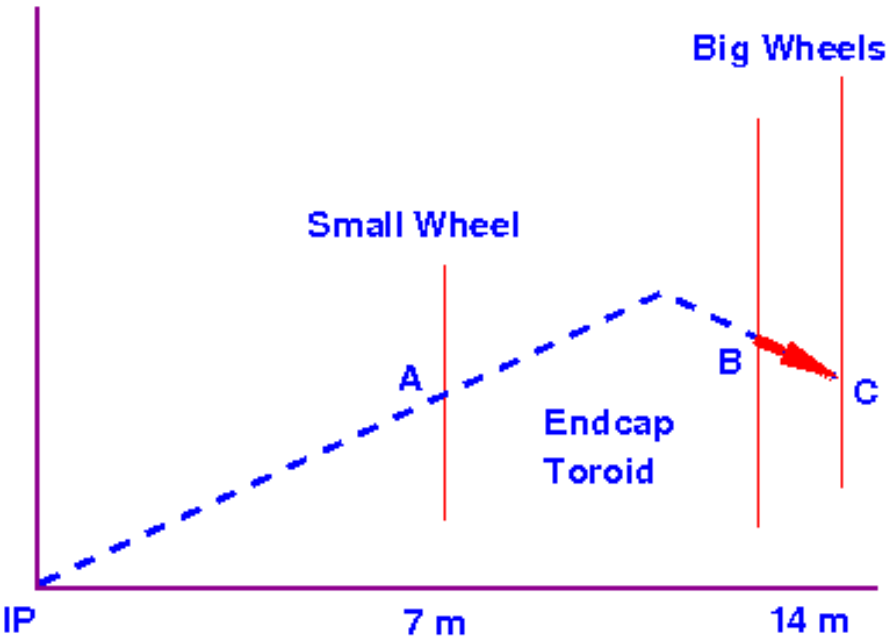
  - **10^9 prestored patterns simultaneously see each silicon hit leaving the detector at full speed.**
- **Track fitting – precise helix parameter & χ^2 determination**
  - **Equations linear in local hit coordinates give near offline resolution:**

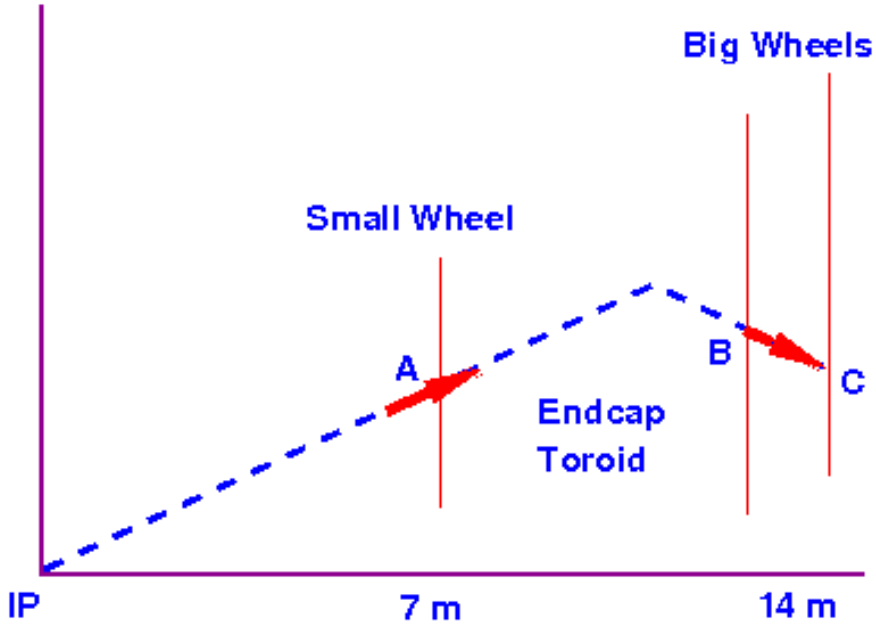
$$p_i = \sum_{j=1}^{14} a_{ij} x_j + b_i$$ **a & b are prestored constants; VERY fast in FPGA**

New Pixel Detector

- Motivation for a new Pixel Detector
  - A much higher performing detector is now possible thanks to important developments in:
    - Front End Electronics (FE-I4 chip mentioned earlier)
    - Sensors (both planar, 3D, Diamonds)
    - Data transmission (multi-Gigabit tranceivers)
    - Technology advances in low mass mechanics, etc
- Will dramatically improve performance
- Possible Upgrade Project for Phase 1, being studied
- Maurice Garcia-Sciveres (LBL) will present it later in this session

The Problem with High pT Muon Triggers





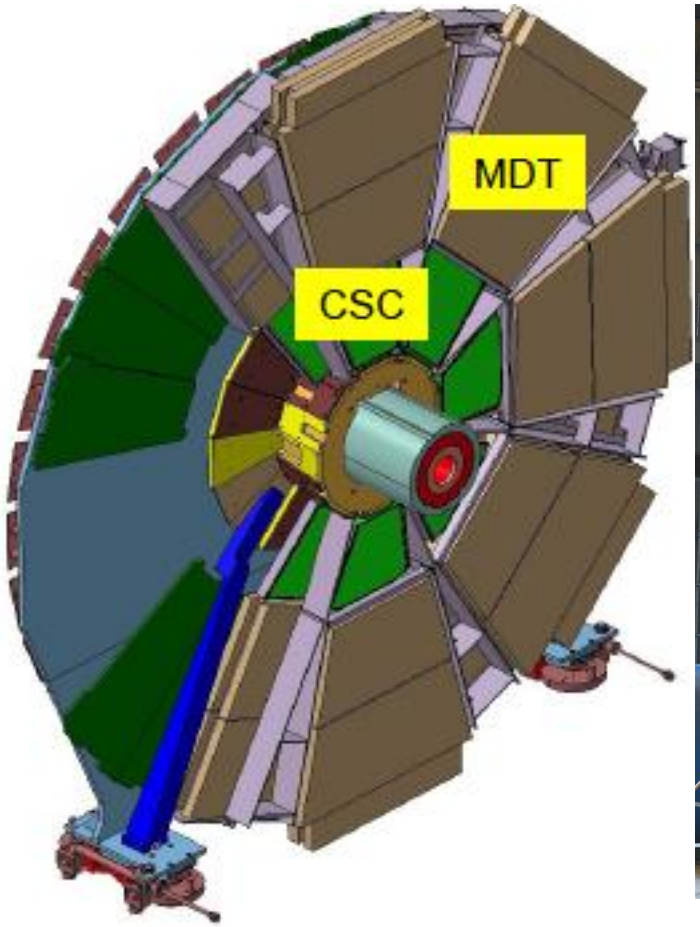
Current Endcap Trigger

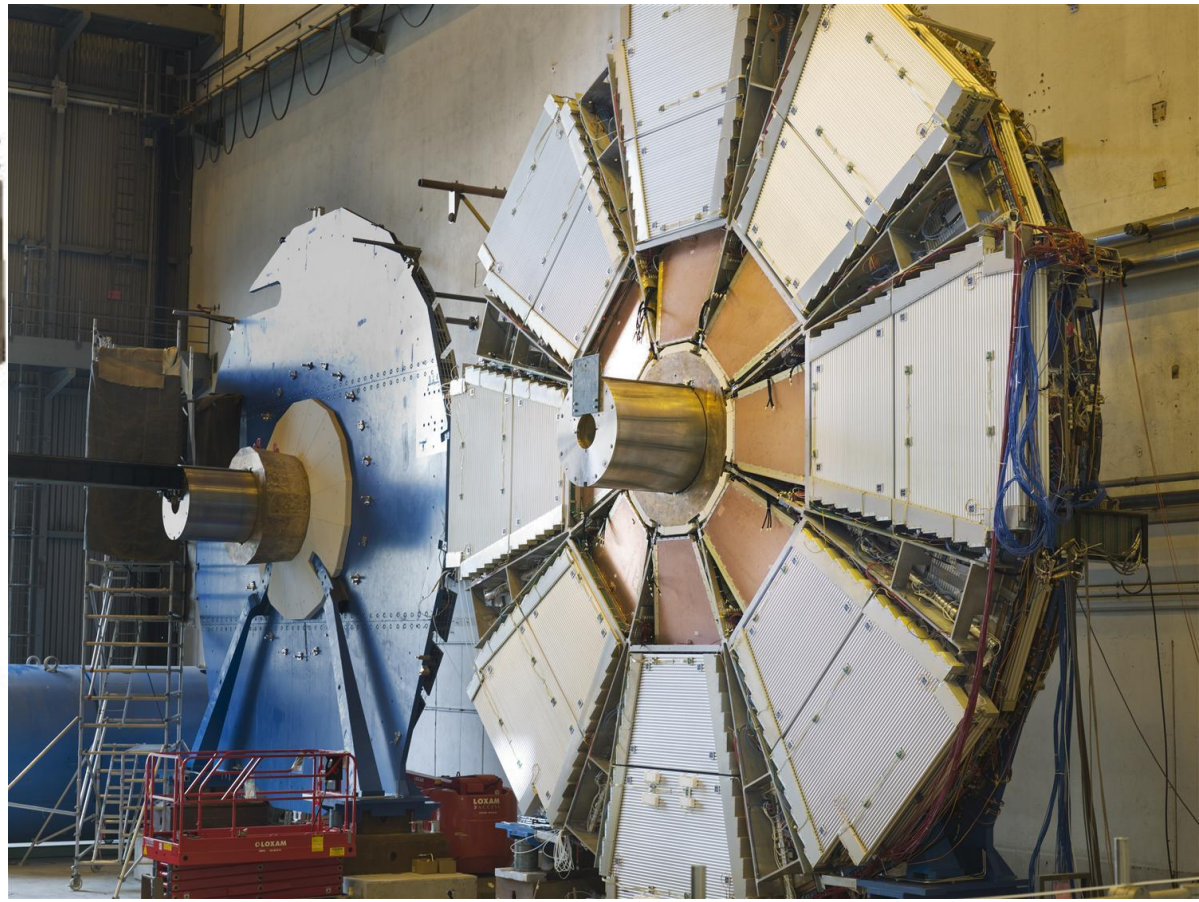
- Only a vector BC at the Big Wheels is measured
- Momentum defined by implicit assumption that track originated at IP
- Random background tracks can easily fake this

Proposed Trigger

- Provide vector A at Small Wheel
- Powerful constraint for real tracks
- With pointing resolution of 1 mrad it will also improve pT resolution
- Currently 96% of High pT triggers have no track associated with them

The Present “Small Wheels” (9m Diameter)

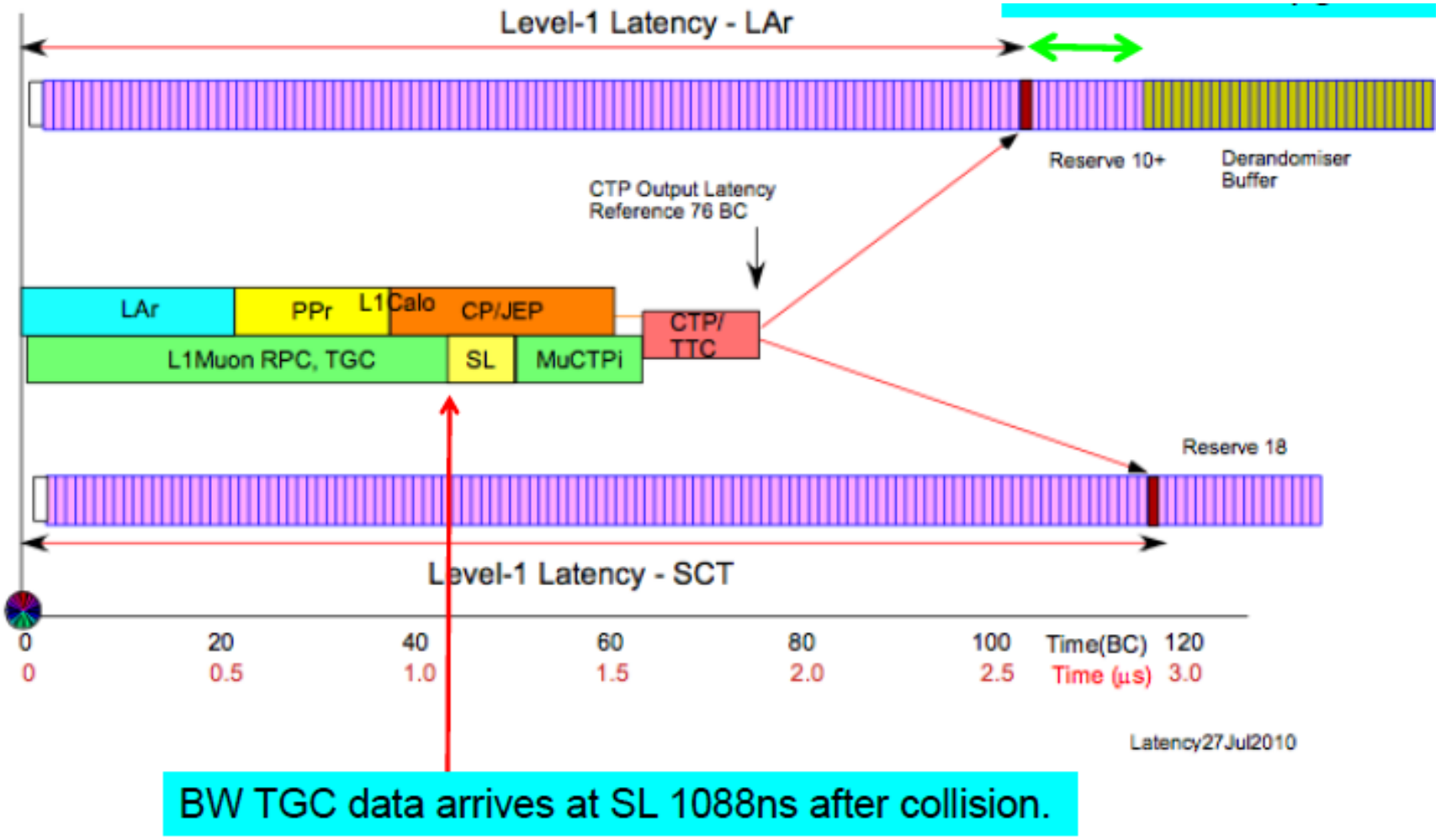




- Need New Detectors that participate in the Level1 Trigger by providing e vector with ~1 mrad resolution
- Need to handle considerably higher rates at L = 5x10e34

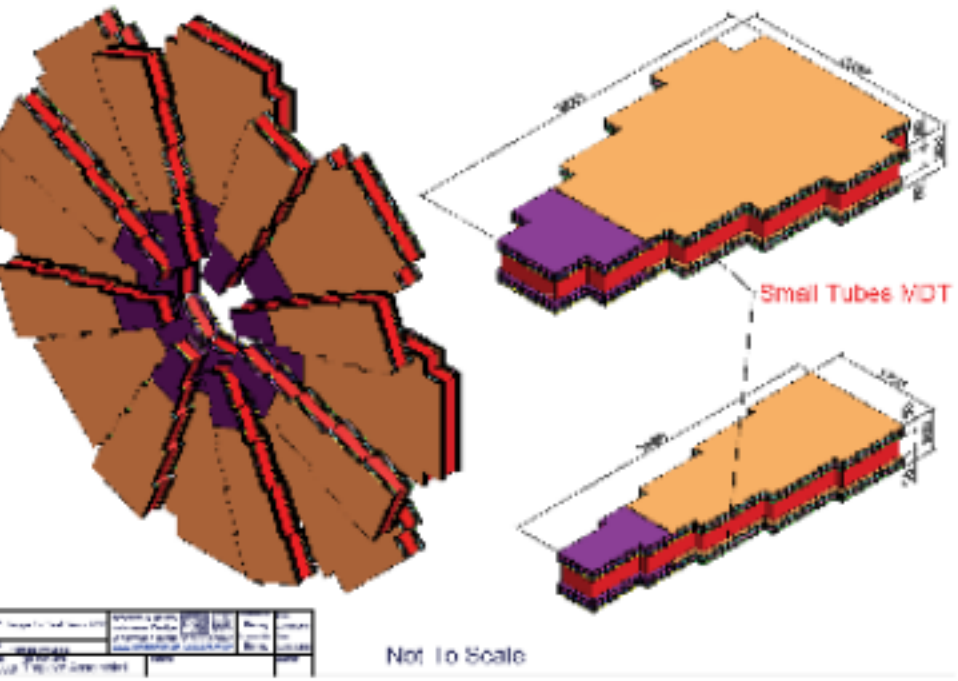
Constraints by the Current L1 Trigger

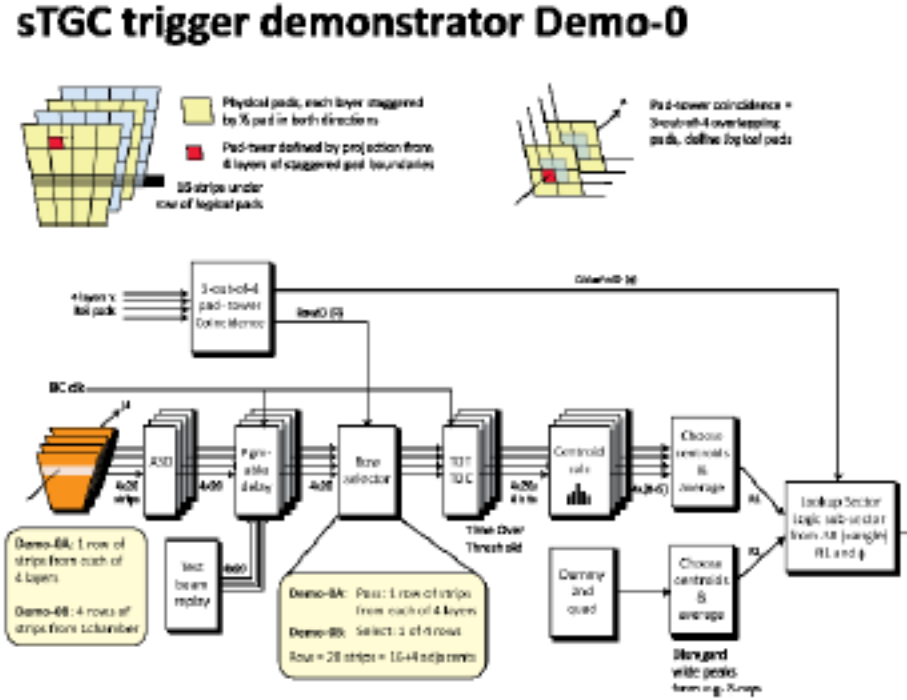
Must provide vector information in ~1 μsec (including transit time)



New small wheel

Proposed layout - 1





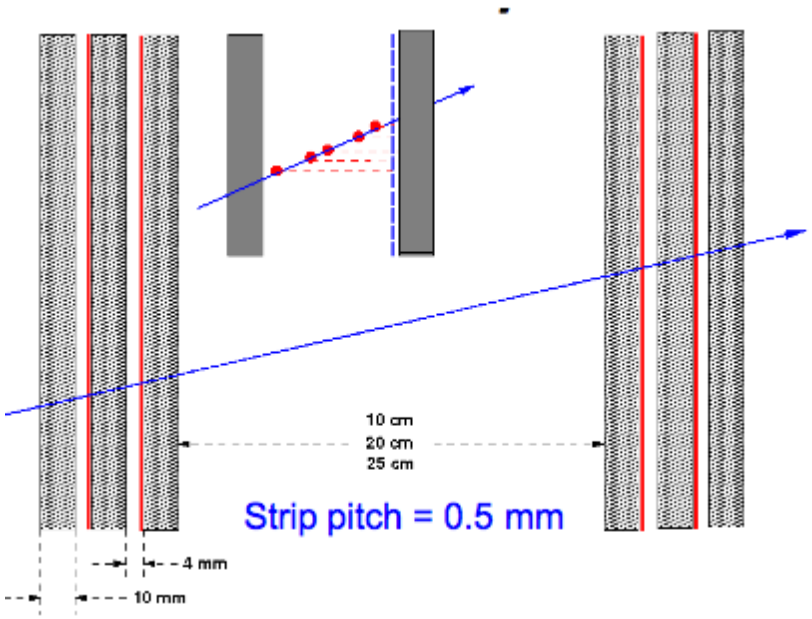
TGC with fine strip 3.5 mm pitch
with pads read-out

4 layers + 4 layers + 1.5cm ϕ MDT in between

Analog read-out (using ToT) of strip charges

Trigger by TGC, precision tracking with MDT and TGC

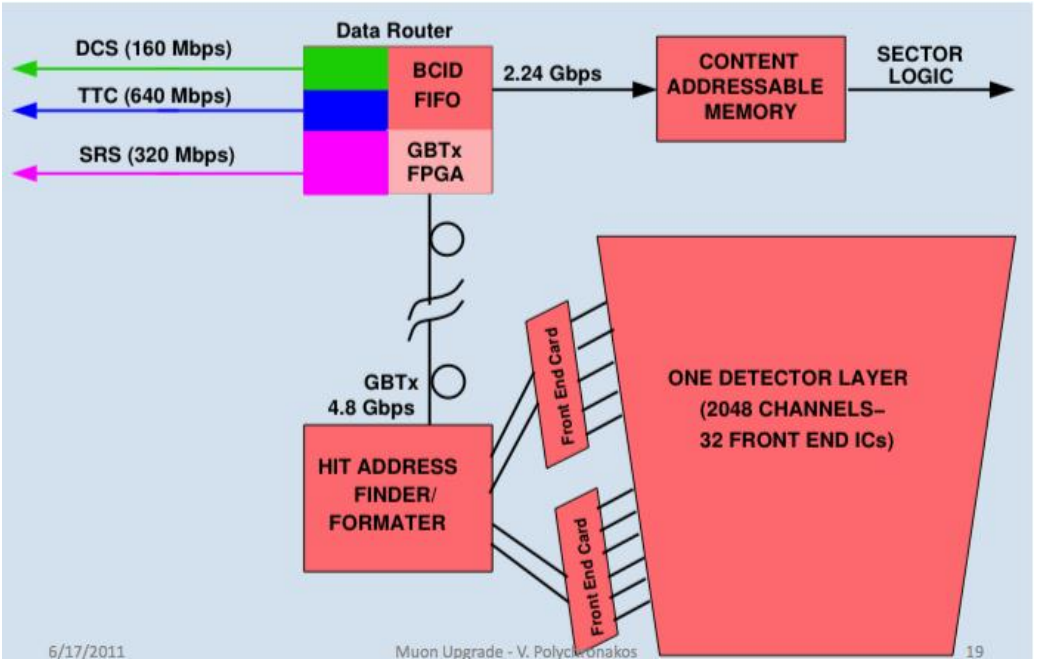
Proposed layout - 2



4 layers + 4 layers Micromegas
0.5 mm pitch strips

~ 2M channels, but take advantage of 0.5 mm strips to consider only the earliest arriving cluster for every BC (negligible loss in efficiency) to reduce the # of channels involved in the trigger to ~30,000

Using Spark resistant Micromegas Detectors

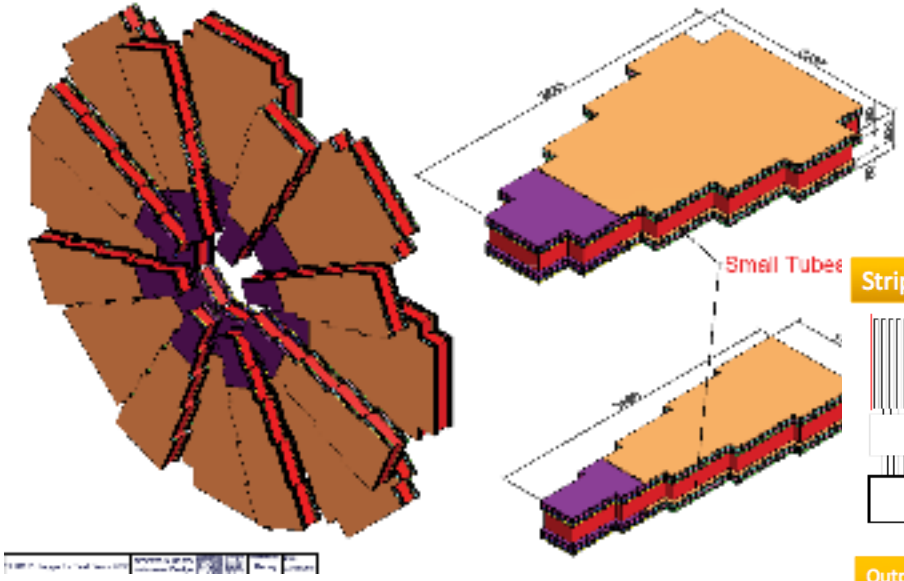


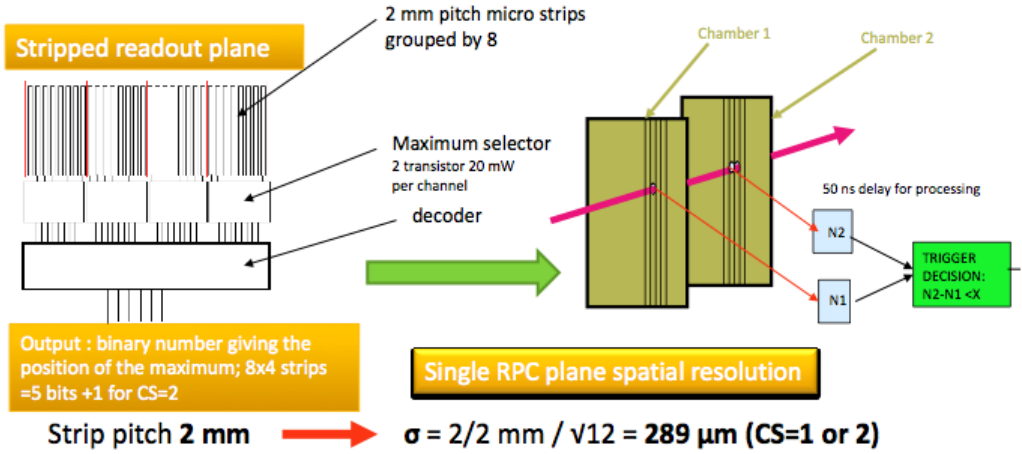
Trigger logic based on
Contents Addressable Memory

for real-time reconstruction of EI segments

Proposed layout - 3

New small wheel





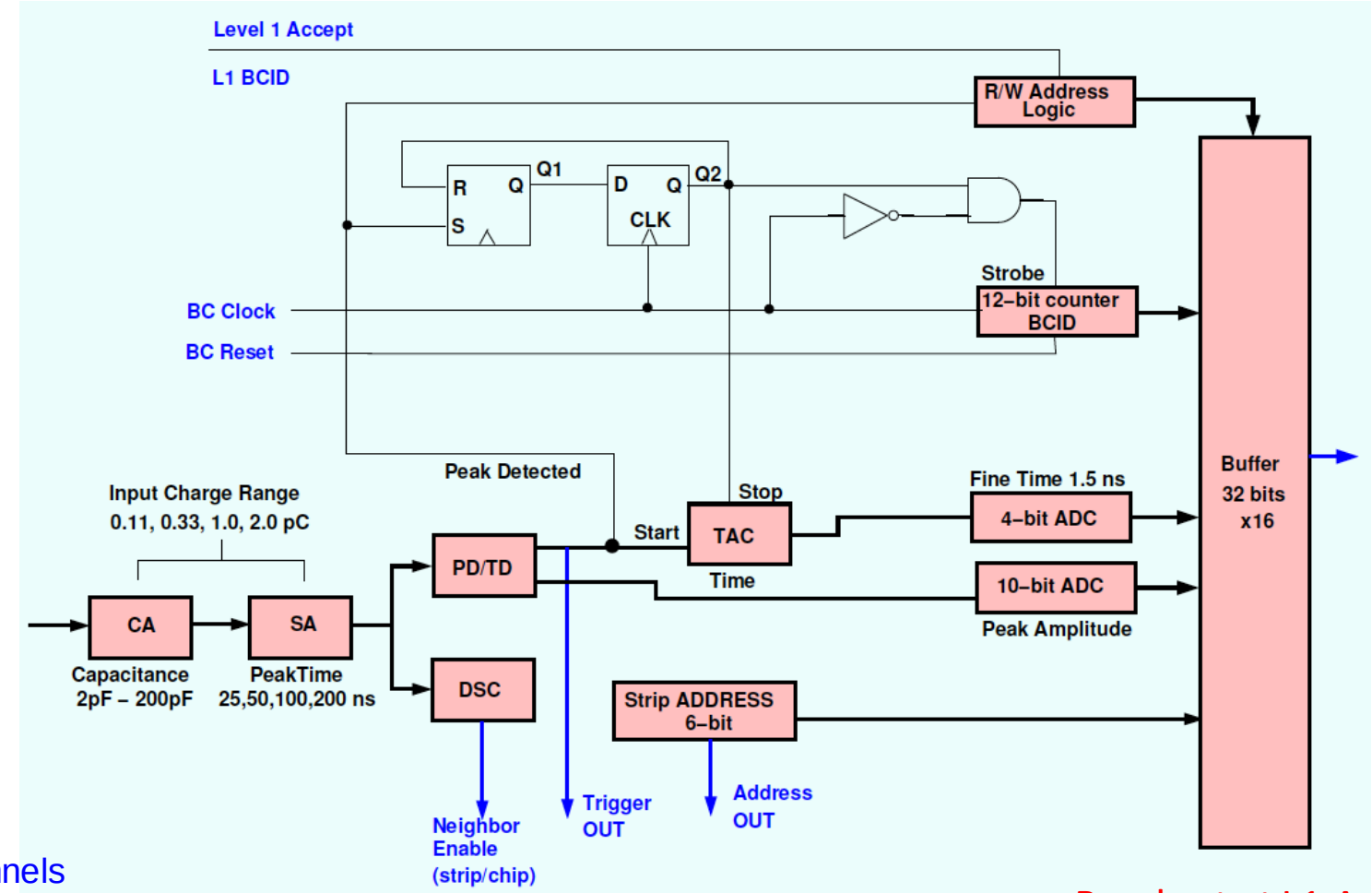
RPC with fine strip 2 mm pitch,
high rate capability with new amplifier and
allowing operation at low HV.

It will be tested in the summer H8 test beam

3 layers + 3 layers + MDT in between

precision tracking (in η) with MDT,
trigger with RPC, profiting from good timing resolution

A new front end IC is being designed (for both TGC and Micromegas)



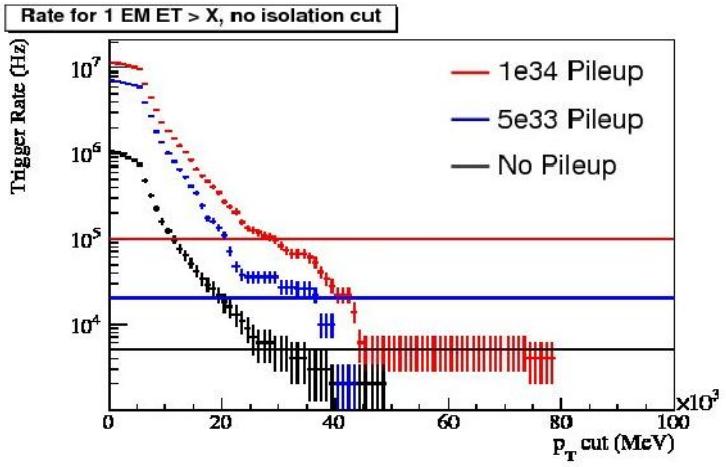
To SRS

- 64 channels
- adj. polarity, adj. gain (0.11 to 2 pC), adj. peaking time (25-200 ns)
- derandomizing peak detection (10-bit) and time detection (1.5 ns)
- real-time event peak trigger and address
- integrated threshold with trimming, sub-threshold neighbor acquisition
- integrated pulse generator and calibration circuits
- analog monitor, channel mask, temperature sensor
- continuous measurement and readout, derandomizing FIFO
- few mW per channel, chip-to-chip (neighbor) communication, LVDS interface

Readout at L1 Accept
No Problem
Zero-suppressed, already digitized, much of DAQ already on Front End IC

Phase-1 L1 Calo Upgrade (implementing Topological Level 1Trigger)

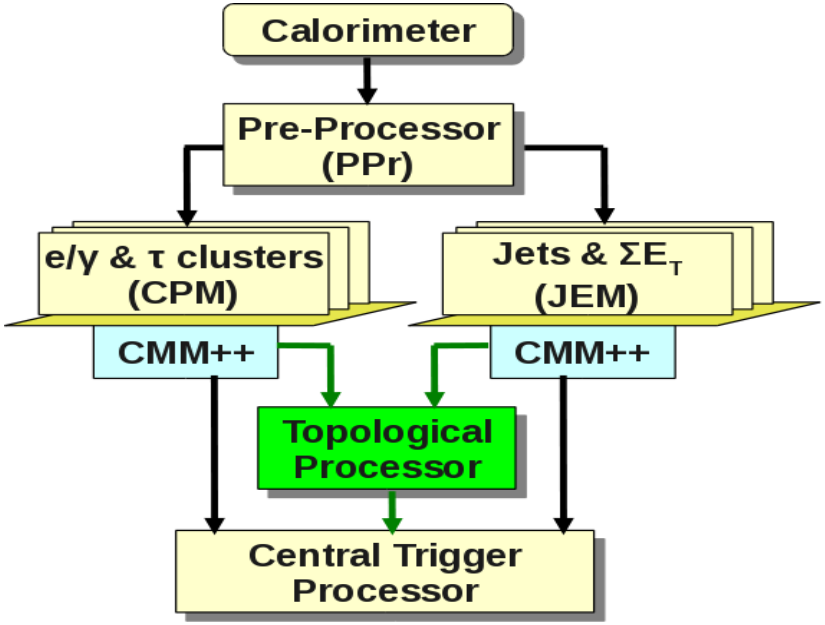
- L1Calo compromised as lumi exceeds design



$L = 10^{34}$	2-jet: $E_T > 35$ GeV	+ $\Delta\Phi < 2.5$
Rate	**35 kHz**	**9 kHz**

- Topological Triggers help
- System Modifications
  - more data from CPMs/JEMs
  - modified data merging
  - new "Topological Processor"

- Staged Implementation



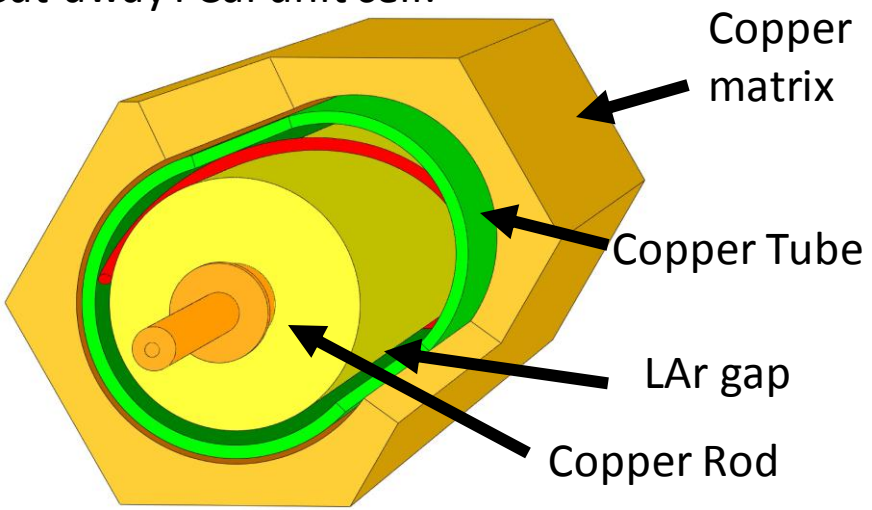
  - Existing (yellow)
  - 40 → 160 MHz bus speed (gold)
  - CMM → CMM++ (blue)
  - Topological Processor (green)

Phase 2 Plans

- Important to maintain single lepton trigger rates similar to those of the current Detector without significantly raising present threshold levels
- Maintain performance of all Systems close to present levels
- Plenty of challenges to be addressed:
  - 100 or 200 collisions/bunch crossing
  - High Radiation levels
  - High Data Rates
- R&D on-going in many areas to address them:
  - New Readout Drivers, optical links, all new Calorimeter electronics, etc

Forward Liquid Argon Calorimeter – Challenging Technology

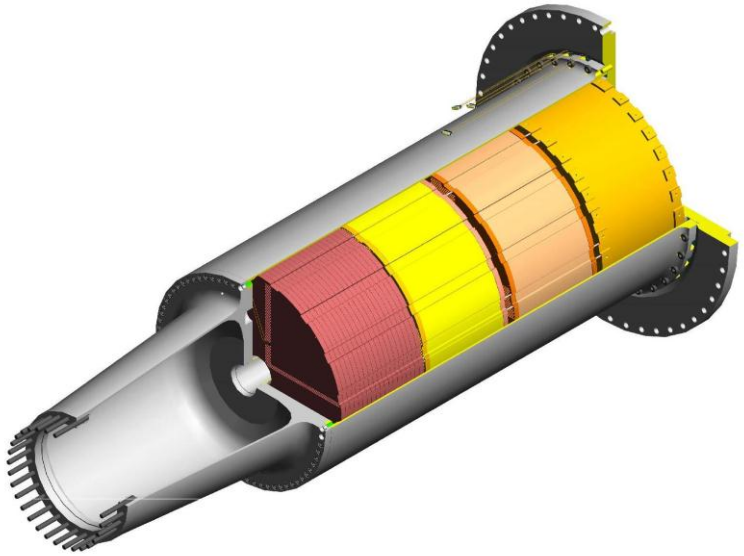
Cut-away FCal unit cell:



LAr gap is small to avoid space-charge effects.

OK for Phase 1, Must be smaller for Phase 2

Now 0.25 mm. Will be 0.10 mm

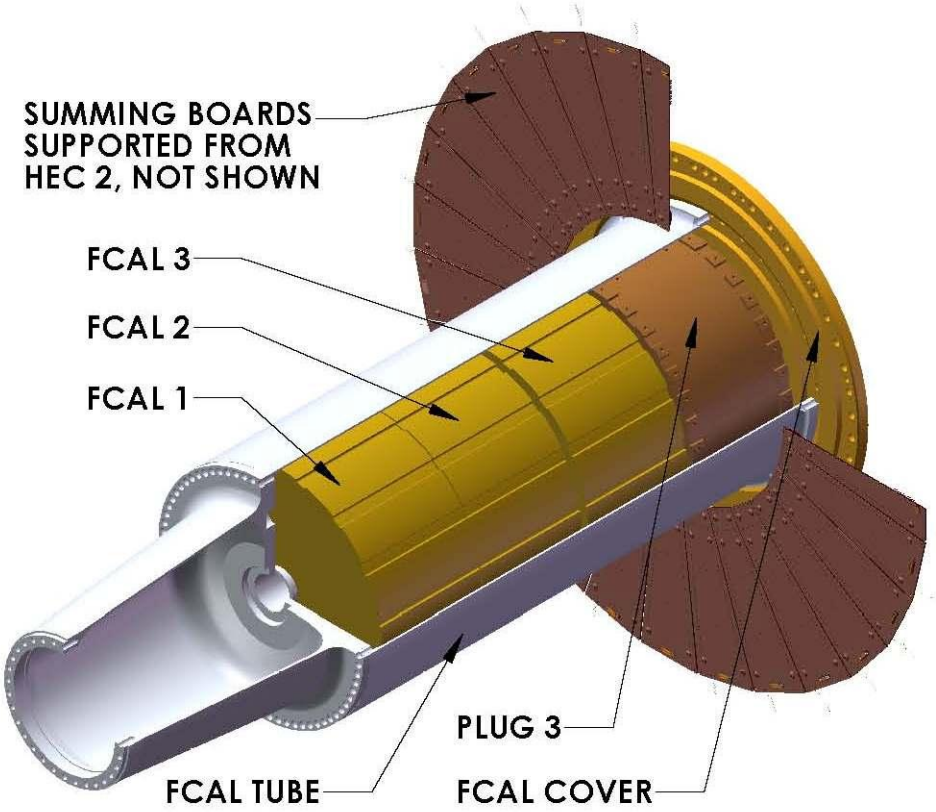


FCal modules in Cryostat support tube:

At HL-LHC phase 2, heating due to dE/dx loss of min-bias particle showers will boil Argon.

Must add LN2 cooling loops

Also considering option to add a warm module in the space in front of FCal



HV distribution circuits in the liquid argon cryostat are included on signal summing boards.

Protection resistors are too large for the HV currents which will be drawn at the HL-LHC phase 2. Must replace these circuits.

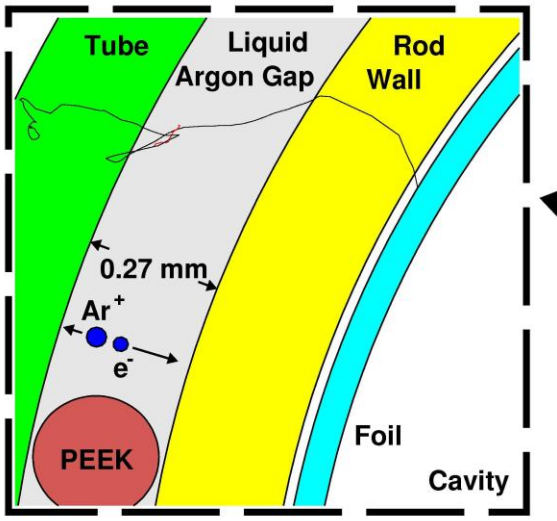
Extensive R&D on LAr in high ionization rates (Study of Space Charge Effects)

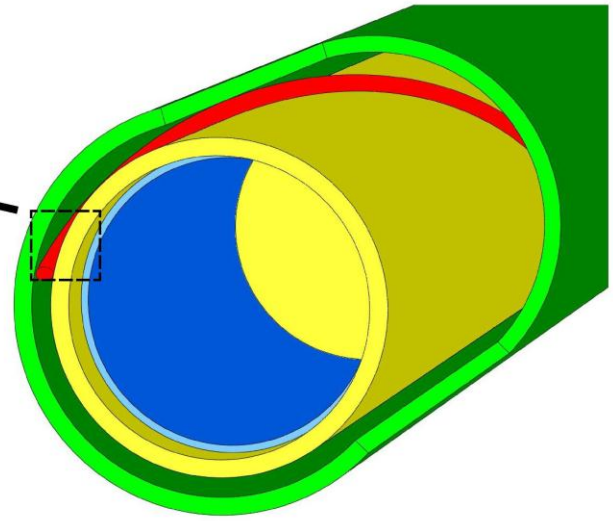
Use hot (50 mCi) Sr(90) beta source with endpoint KE of 2.28 MeV

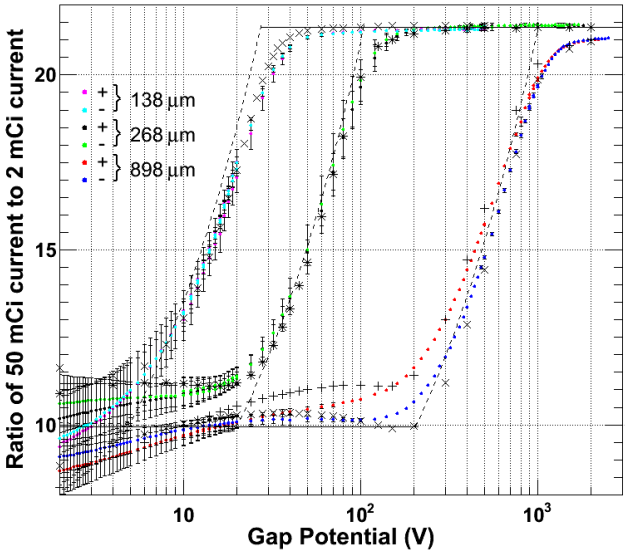
Betas from source ionize the liquid argon

Special electrode with cavity in rod to hold beta source

Three LAr gaps entering the space-charge limited regime



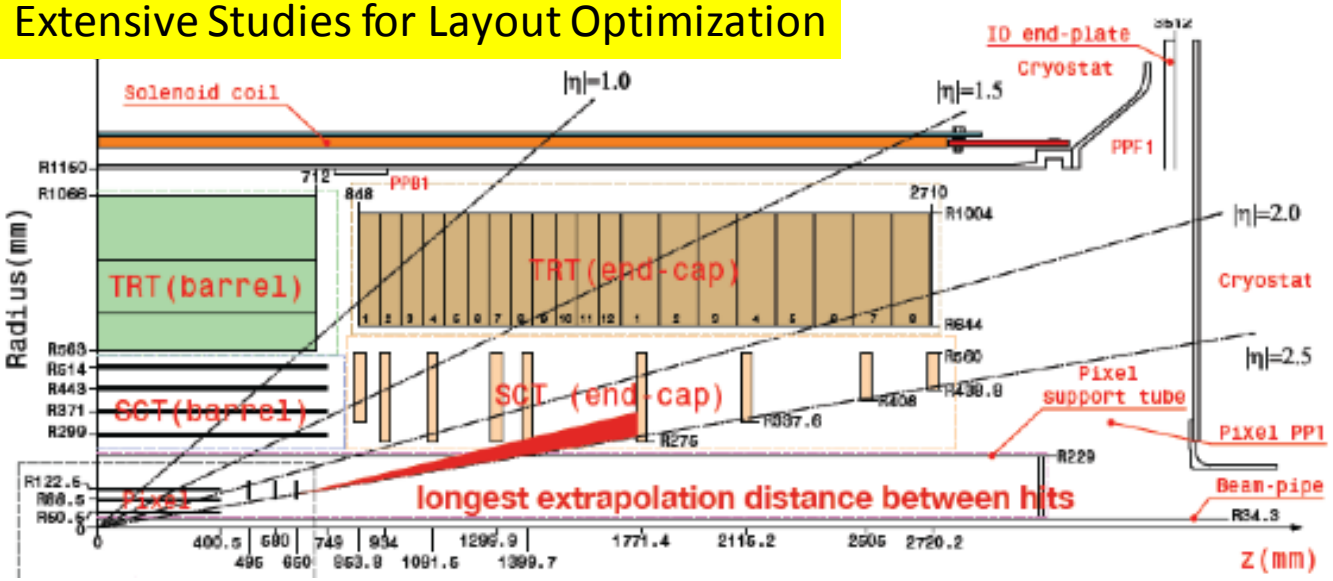


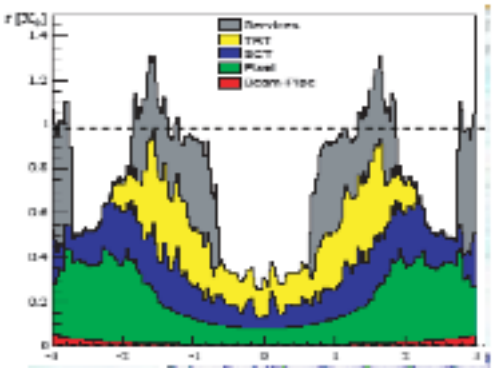


Big advantage: Most of the ionization is uniformly distributed.

New All Silicon ID tracker

Extensive Studies for Layout Optimization

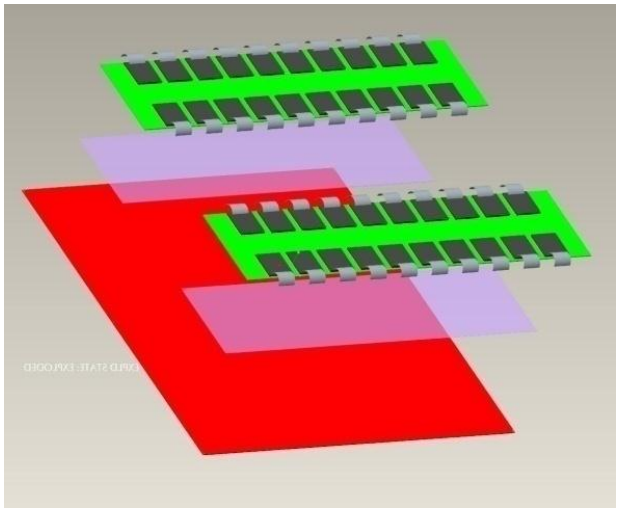




Substantial material for services

Studies are on going in all areas

- Sensors
- Readout chips
- Module integration
- Cooling
- Powering
- Layout and physics performance

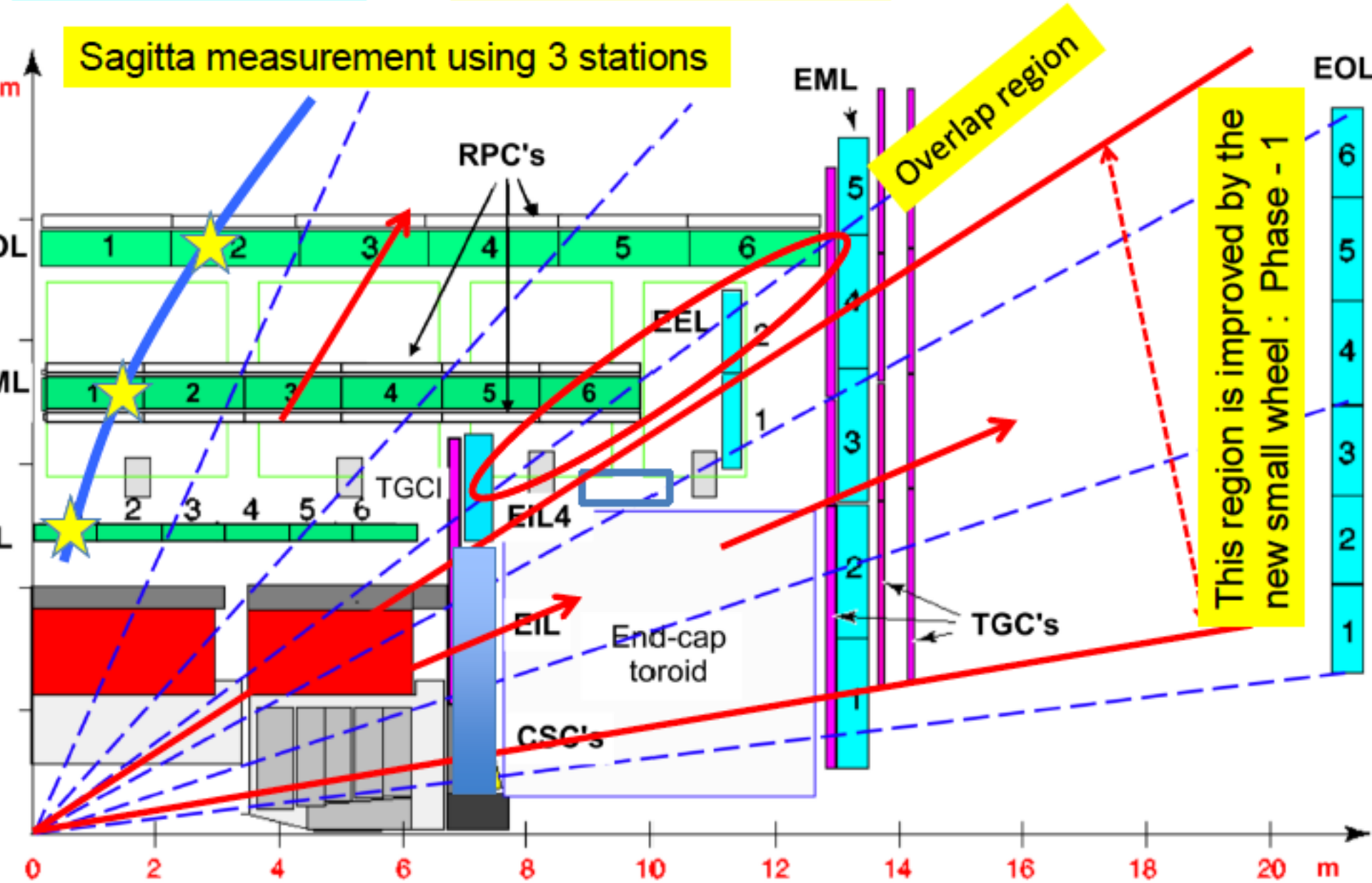


ATLAS upgrade : phase - 2

Trigger for phase-2

L1 Muons in barrel MDT

p_T resolution 20% → 5% at 20 G



Summary

- The HL-LHC is expected to provide ~300/fb/year for the 3d decade of this Century
- ATLAS is already preparing to handle this data deluge
- Shorter term plans/projects are better defined
- In 2013/14 shutdown, there will be a new detector element: IBL
- In phase-1, new muon small wheel, elements of new topological triggers
- In phase-2, completely new inner tracker, some trigger upgrade of muon chamber
- possibly new forward calorimeter, major upgrade on trigger and DAQ and Calorimeter electronics
- Extensive Studies and work are under way.