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The LHC at CERN has successfully reached energies and luminosities beyond previous hadron accelerators. To take advantage of this situation the ATLAS experiment plans to add a new pixel layer to the current pixel detector during the 2013 shutdown. The optical data transmission system will also be upgraded to handle the higher data transmission speed. Two ASICs have been prototyped for this new generation of optical links to incorporate the experience gained from the current system. The ASICs were designed using a 130 nm CMOS process. One ASIC contains a 4-channel VCSEL driver array and the other a 4-channel PIN receiver/decoder array with one channel of each array designated as a spare to bypass a malfunctioning VCSEL or PIN channel. Each of the receiver/decoder circuits includes pre-amplification, a bi-phase mark (BPM) clock/data recovery circuit, and low voltage differential signal (LVDS) outputs for both the clock and data. In order to allow remote control of the chip, the ASIC includes command decoders that have been designed to be single event upset (SEU) tolerant. The command word for configuring the chip is formed by a majority vote of the command decoders. To further improve the SEU tolerance, all latches are based on a dual interlocked storage cell (DICE) latch.
The driver ASIC is designed to operate at 5 Gb/s. Each channel has an LVDS receiver, an 8-bit DAC, and a VCSEL driver. One channel is designated as the spare channel and contains a 16:1 multiplexer. The multiplexer allows routing of the received signal from any of the three channels to the spare channel output. The 8-bit DAC is used to set the VCSEL modulation current. To enable operation in case of a failure in the communication link to the command decoder, we have included a power on reset circuit that will set the VCSEL modulation current to 10 mA upon power up.
We characterized the ASICs and then irradiated them to measure their radiation hardness and SEU tolerance. We will present results from this study. In addition, a new version of the ASIC has been submitted for production. Here the ASICs have been expanded to 12 channels with improvements based on the prototype results. We will briefly discuss this new design.

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