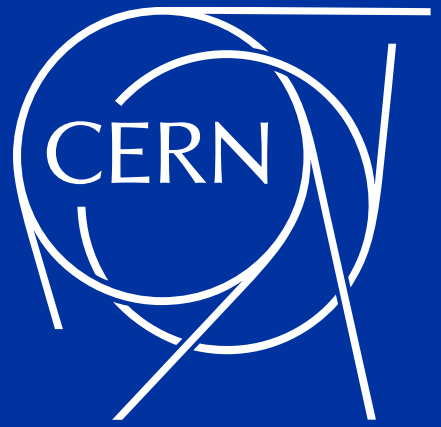


LHC BLM

Firmware Update during TS1-23

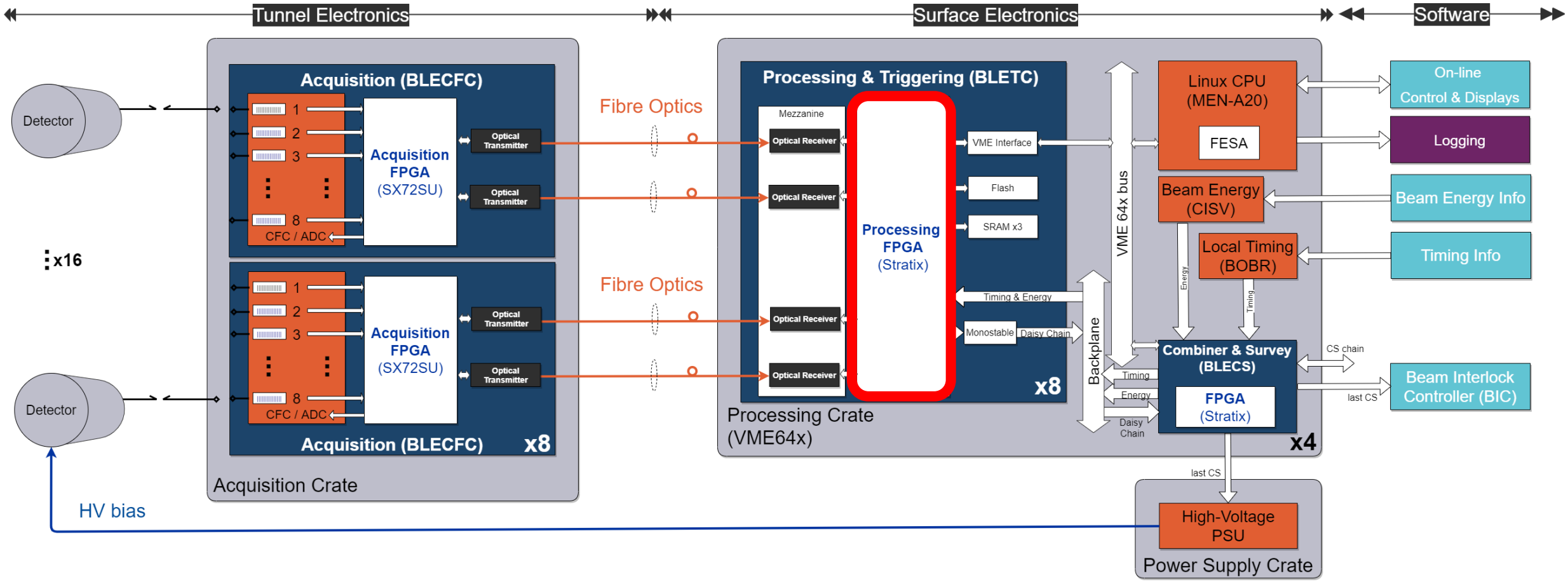
238th Machine Protection Panel Meeting

Mathieu Saccani (SY-BI-BL) on behalf of the BLM team

14/06/2023

BLMLHC Optical Link Architecture

- Surface Processing Electronics (BLETC): 2x2 **redundant optical links** receiver (carrying the same info)
- Link quality is evaluated at the reception: if no good package from either link, **an interlock is generated**
- Optical receiver very sensitive to **temperature**



Optical Link Reception

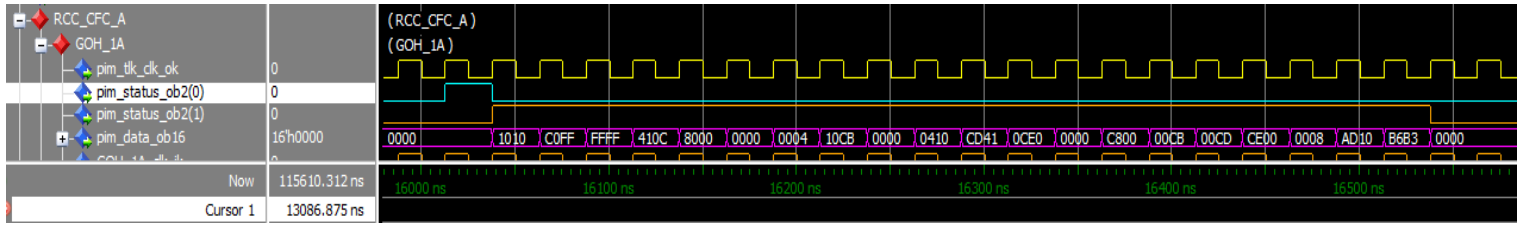
- **Redundant link**
- **Protected by CRC32**
- **Frame ID counter**

CID (card identity number)	
STATUS 1	
STATUS 2	
Count 1	ADC 1
ADC 1	Count 2 / ADC 2
ADC 2	Count 3
ADC 3	Count 4
Count 4	ADC 4
Count 5	ADC 5
ADC 5	Count 6 / ADC 6
ADC 6	Count 7
ADC 7	Count 8
Count 8	ADC8
FID (frame identity number)	
DAC1	DAC2
DAC3	DAC4
DAC5	DAC6
DAC7	DAC8
CRC	
CRC	

40us frame
(20x16bits word)

- **TLK1501 Deserializer**
  - 40MHz clock
  - 2 control bits: StartOfFrame (SOF) + RestOfFrame (ROF)
  - 16 data bits

Optical receiver mezzanine: EMDS https://edms.cern.ch/document/493588/4

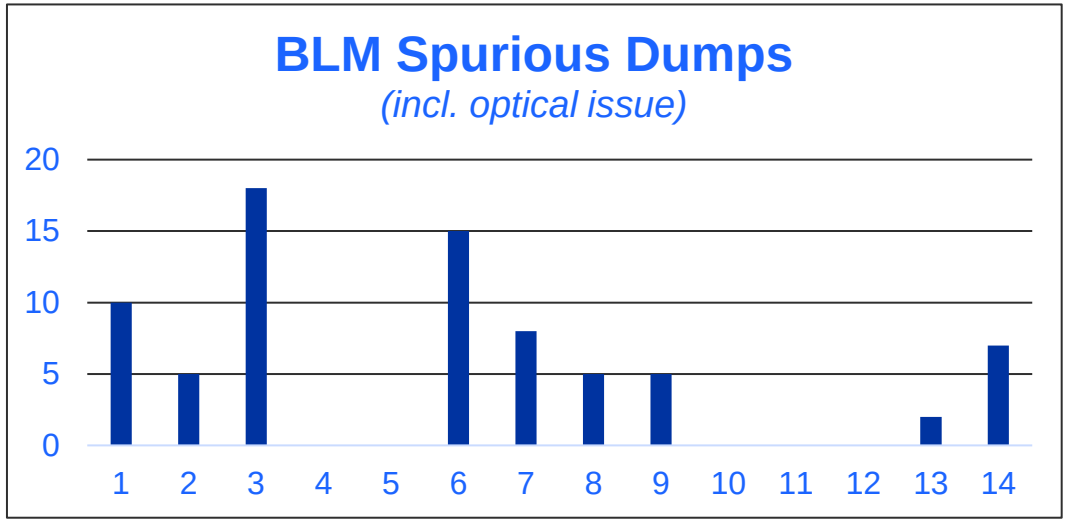


Simulation example

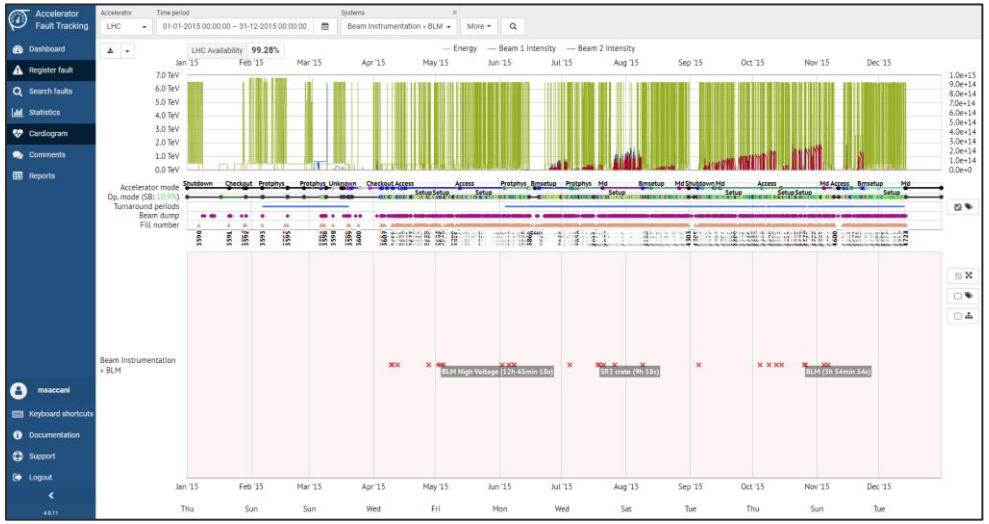
- **BLETC Firmware**
  - Receive asynchronous links (clock + 2ctrl + 16data)
  - Wait for both frames
  - Decide which frame to keep:
    - CRC
    - card ID
    - frame ID increase

Spurious Optical Link Errors

This issue may have been present since Run1.



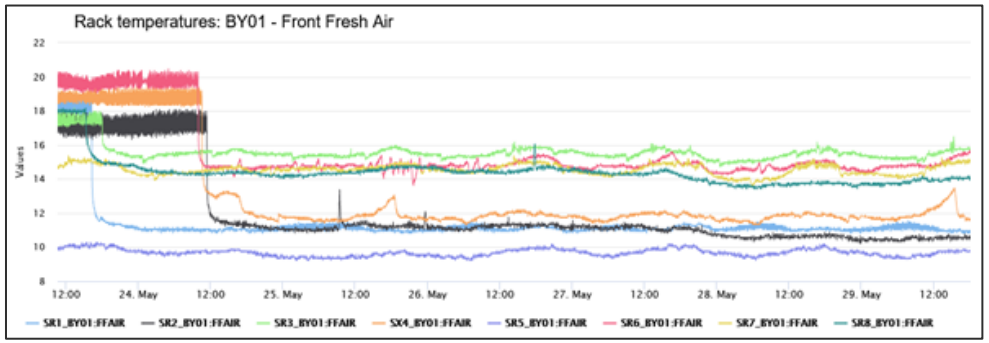
*Extract AFT (*approx. numbers)*



BLM AFT cardiogram view (2015)

Partially solved by decreasing the rack temperature during Run2.
But the temperature was increased during LS2, and not lowered after.
➔ Temperature set back from 23 °C to 16°C on the 24th May 2023.

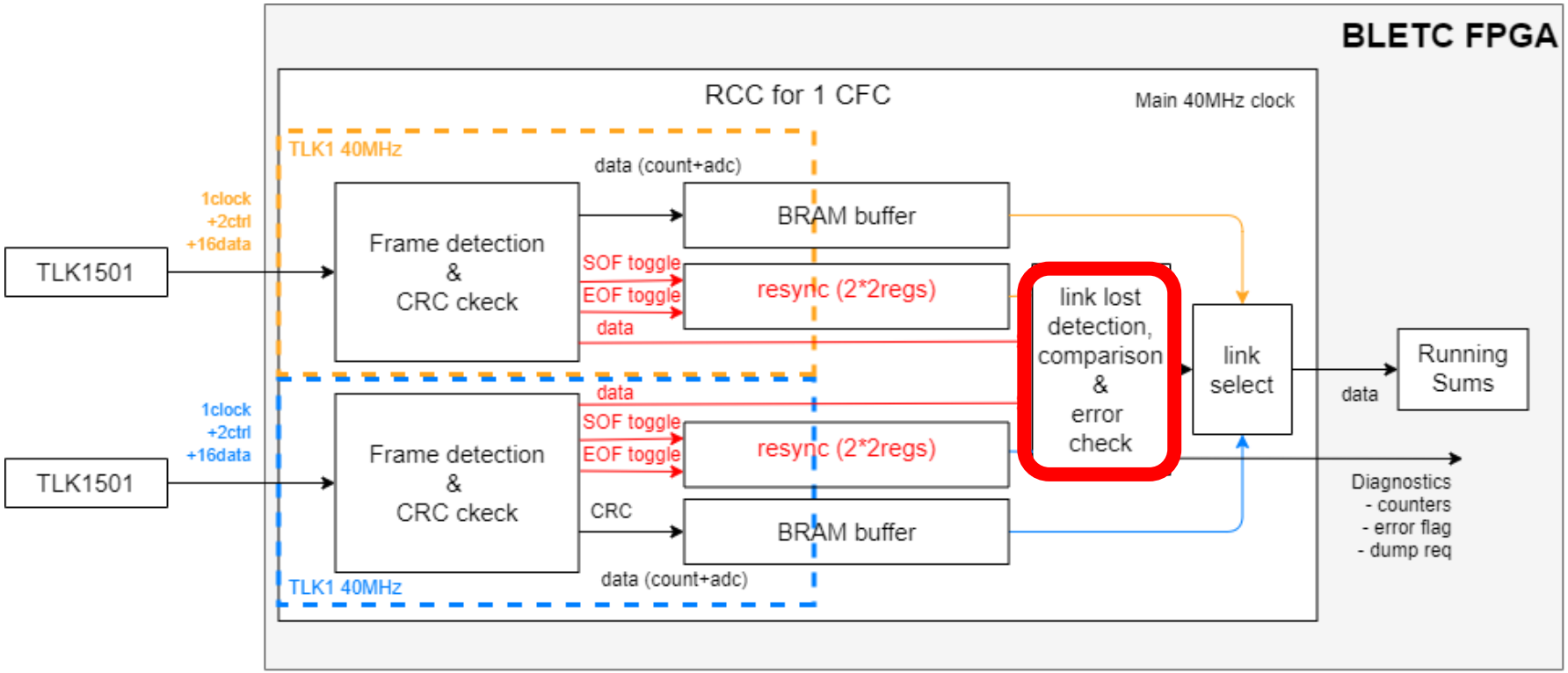
Example of spurious dump: https://issues.cern.ch/browse/BIBML-2710
Example of thermalized rack reconfiguration: https://issues.cern.ch/browse/BIBML-2741



BLM rack temperature reduction in May 2023

Optical Link Reception Issue

- An investigation on the spurious dumps in April/May 2023 allowed to identify the **source of the issue**.
- Failure case: **1 intermittent faulty link** leading to a spurious failure of the entire decision-making process for both links !
- The **Frame ID check** frameID(n+1) = frameID(n)+1 is **done twice on the same frame**: on the good link. then on the bad one.
- Happens in **very specific conditions**: temperature & weak tunnel transmitter make 1 link unstable
- FW code to be updated: fully synchronous decision process (no clock domain crossing) ➔ easy to update and simulate



Data reception in the processing FPGA

Redundant Link Arbitration Misalignment

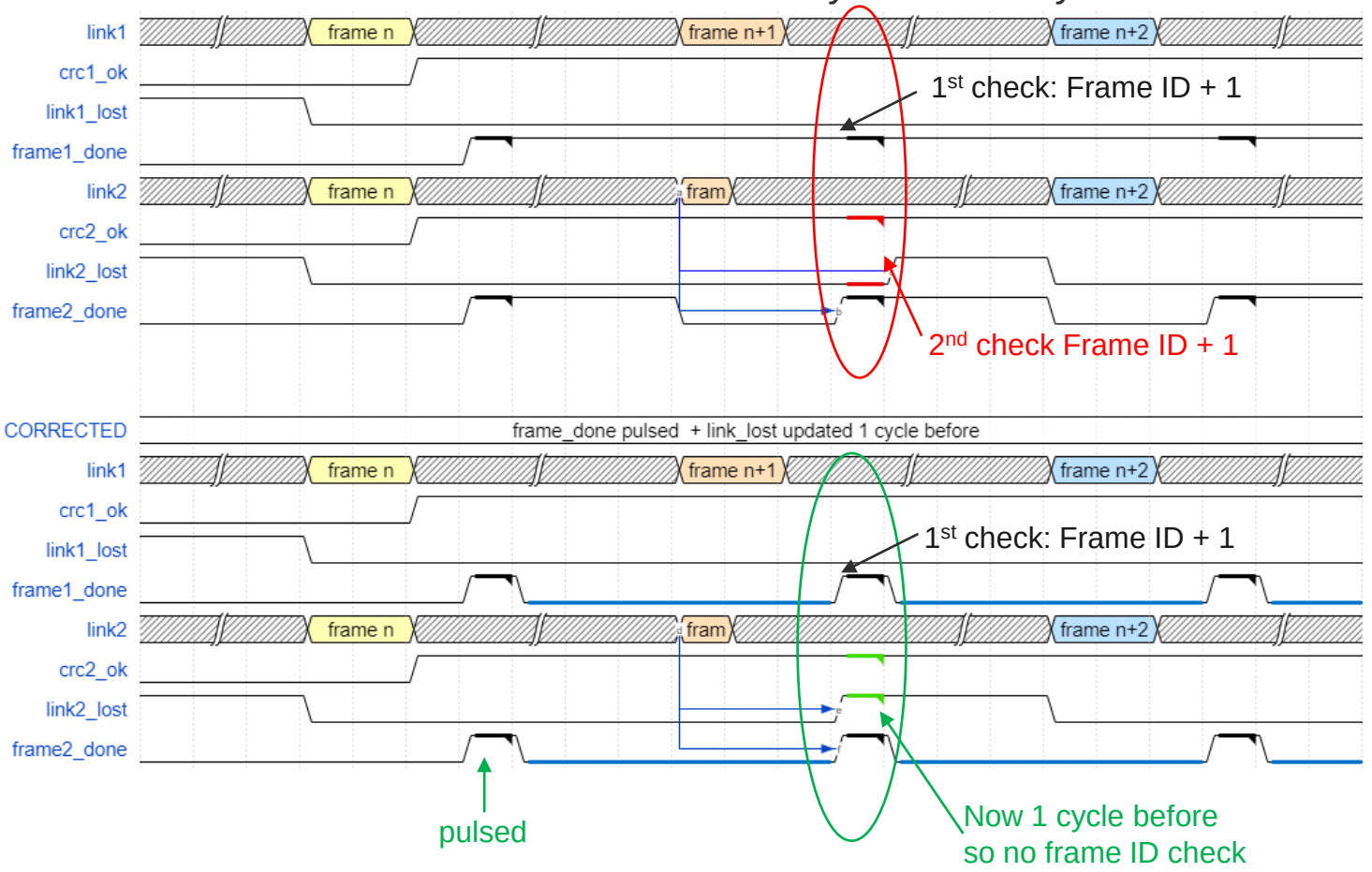
Firmware issue:
If one link is shifted and the end of packet is missing, the good link is used, but the **bad link is taken into account for the Frame ID check**, as the corresponding “lost” flag arrives **1 cycle to late** and the CRC_ok is not reset.
Consequence 2 FID errors are both frames are compared consecutively.

This issue happens only:
1- at high temperature: optical diode unstable, and the deserialiser TLK1501 at the limit (resynchro cycles + CRC errors, + lost frames).
2- when one link is good and the other recovers and stops continuously.
3- when the bad link received frame is shifted by exactly one 25ns clock cycle

Correction: 2 changes in the RTL code
- frame_done is now **pulsed**
- lost_link flag generated **one cycle before**.

Validation: **non-regression tests played in simulation**.

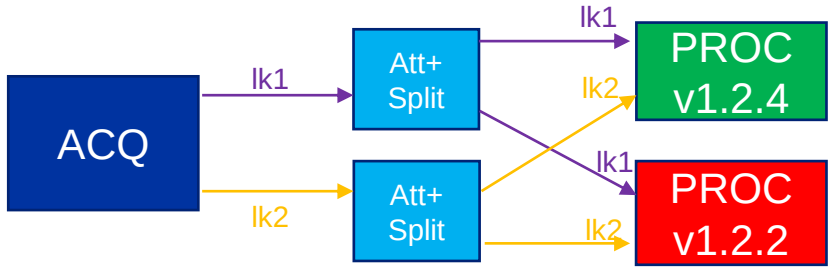
Temperature ➔ incomplete frame
Link1 is good & Link2 intermittently faulty
Bad link is shifted by one 25ns cycle



Lab Testbench

Custom and manual testbench on one board: **no more error spurious**.

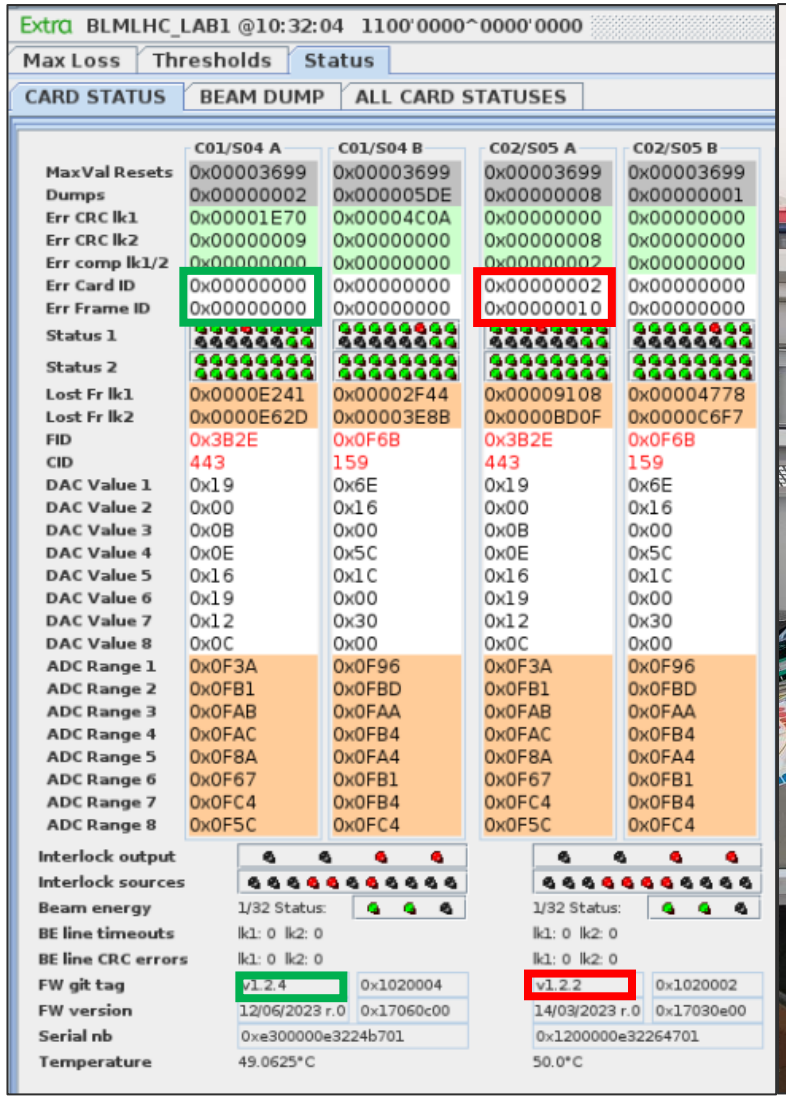
In the lab, 2 BLETCs board running:
- v1.2.4 corrected FW
- v1.2.2 current operational FW

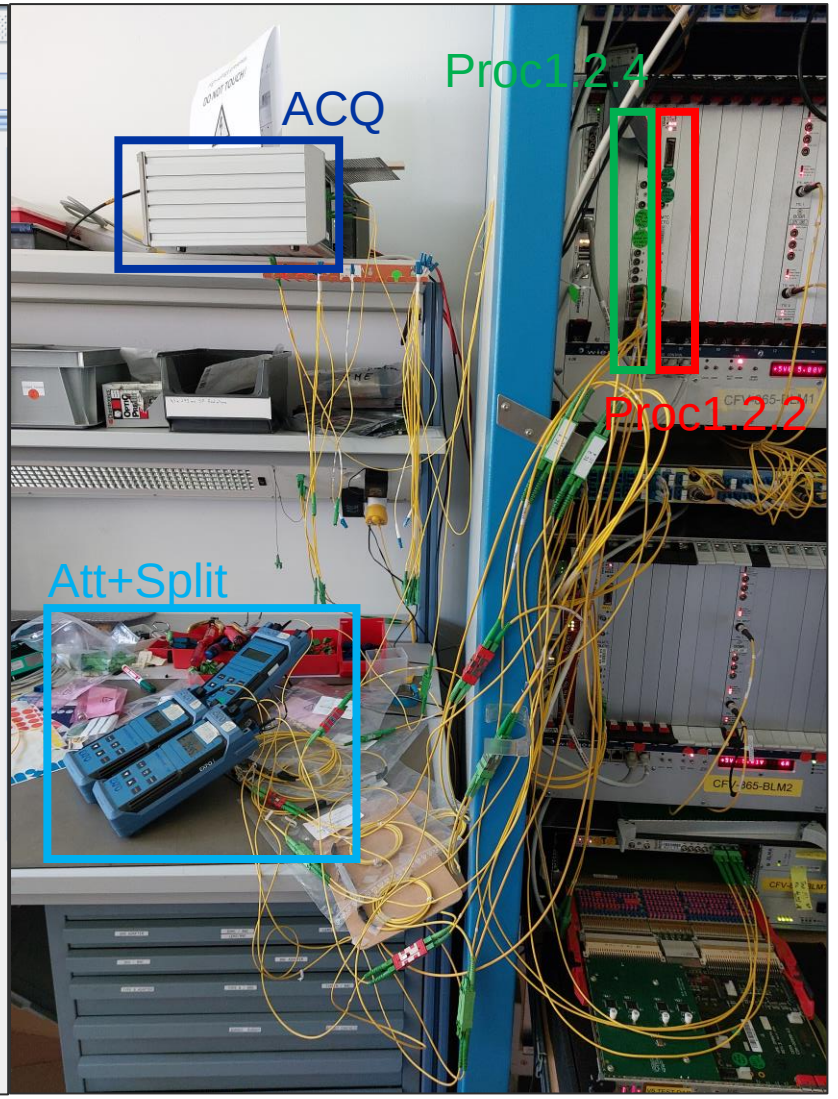


Tune the optical attenuator to reach the limit on one link, then the other.

More statistics: since TS1-23 in LHC >600 processing boards run the v1.2.4.

Can be easily **rolled-back** if needed.



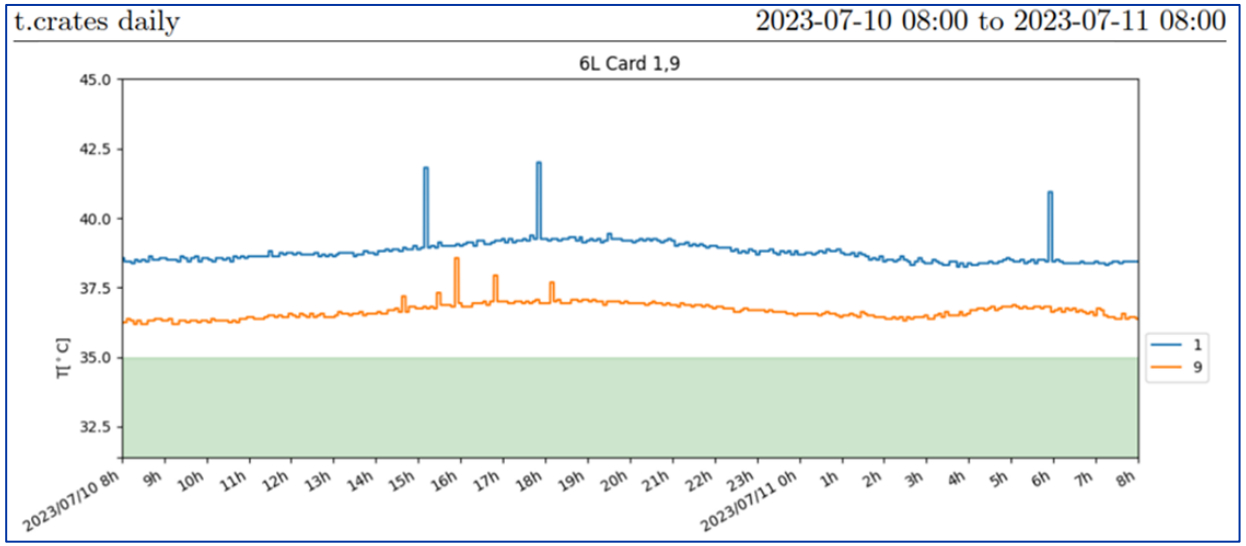


Testbench in the lab

Deployment and test with beam

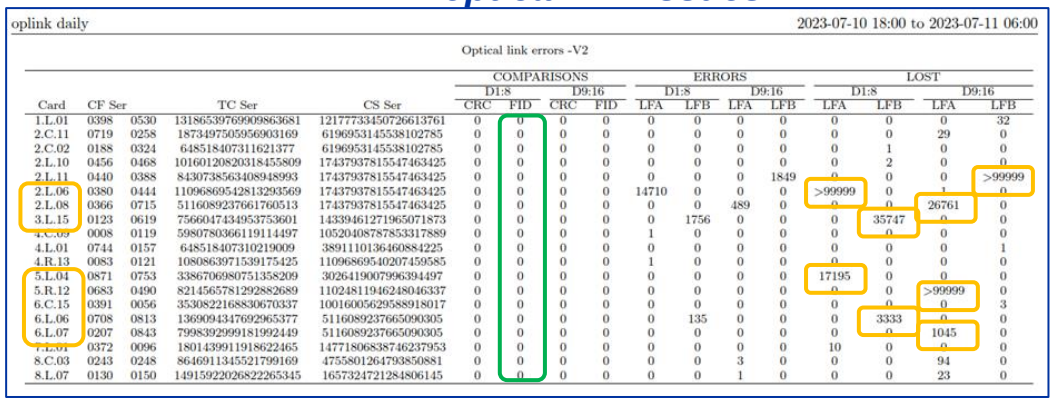
The new firmware v1.2.4 was deployed during TS1-23 on the 19th June 2023 (https://issues.cern.ch/browse/BIBML-509).
We have CRON jobs to get daily reports: temperatures & optical link diagnostics.

➔ Still a few hot boards and weak links
➔ No spurious dump detected since the upgrade.



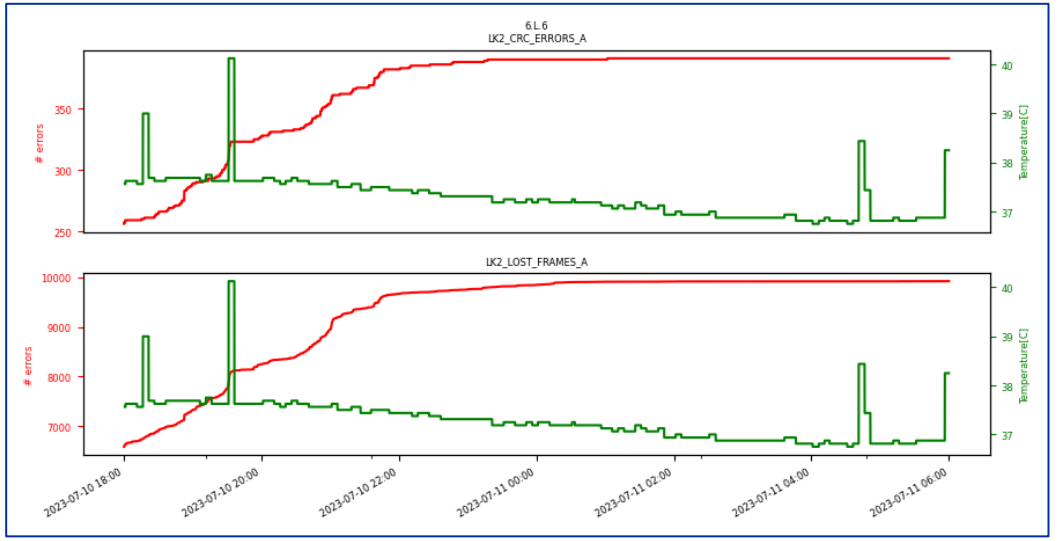
BLM Electronics Temperature Report at 6L

BLM optical link issues


oplink daily — 2023-07-10 18:00 to 2023-07-11 06:00

Optical link errors -V2

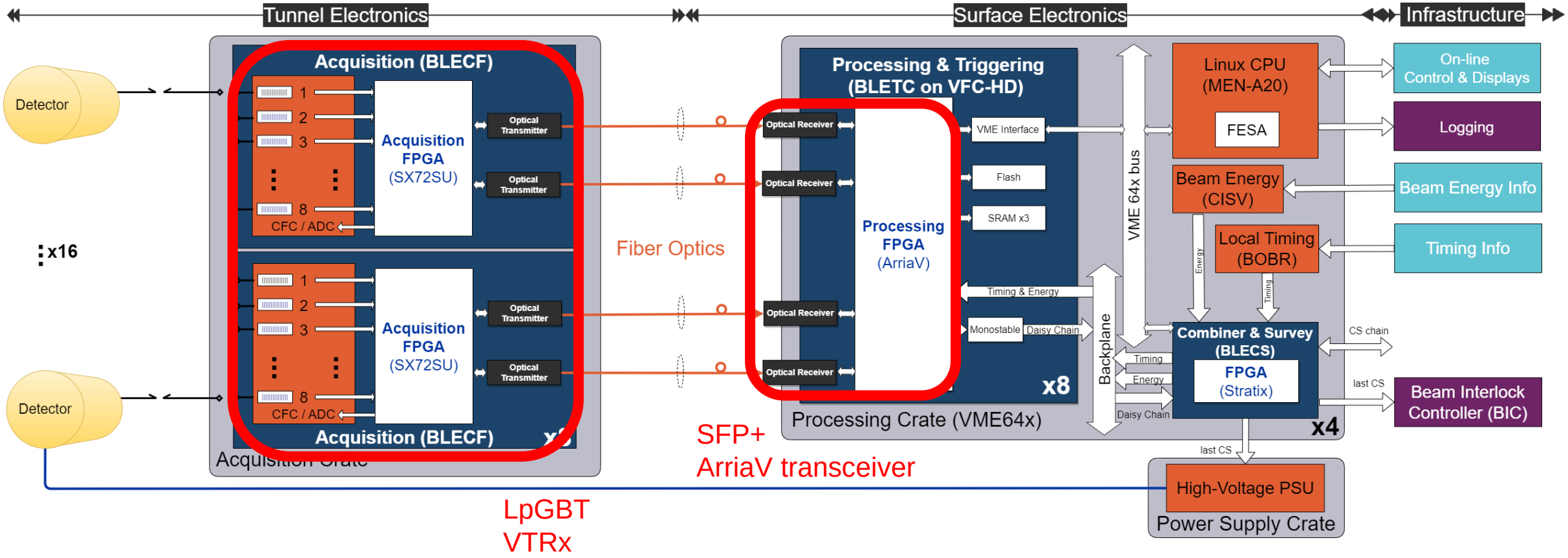
Card	CF Ser		TC Ser	CS Ser	COMPARISONS D1:8 CRC	COMPARISONS D1:8 FID	COMPARISONS D9:16 CRC	COMPARISONS D9:16 FID	ERRORS D1:8 LFA	ERRORS D1:8 LFB	ERRORS D9:16 LFA	ERRORS D9:16 LFB	LOST D1:8 LFA	LOST D1:8 LFB	LOST D9:16 LFA	LOST D9:16 LFB
1.L.01	0398	0530	1318653976990986368 1	12177733450726613761	0	0	0	0	0	0	0	0	0	0	0	32
2.C.11	0719	0258	1873497505956903169	6196953145538102785	0	0	0	0	0	0	0	0	0	0	29	0
2.C.02	0188	0324	64851840731162137 7	6196953145538102785	0	0	0	0	0	0	0	0	0	1	0	0
2.L.10	0456	0468	1016012082031845580 9	17437937815547463425	0	0	0	0	0	0	0	0	0	2	0	0
2.L.11	0440	0388	8430738563408948993	17437937815547463425	0	0	0	0	0	0	0	1849	0	0	0	>99999
2.L.06	0380	0444	1109686954281329356 9	17437937815547463425	0	0	0	0	14710	0	0	0	>99999	0	1	0
2.L.08	0366	0715	5116089237661760513	17437937815547463425	0	0	0	0	0	0	489	0	0	0	26761	0
3.L.15	0123	0619	7566047434953753601	14339461271965071873	0	0	0	0	0	1756	0	0	0	35747	0	0
4.C.09	0008	0119	5980780366119114497	10520408787853317889	0	0	0	0	1	0	0	0	0	0	0	0
4.L.01	0744	0157	64851840731021900 9	38911101364608842225	0	0	0	0	0	0	0	0	0	0	0	1
4.R.13	0083	0121	1080863971539175425	11096869540207459585	0	0	0	0	1	0	0	0	0	0	0	0
5.L.04	0871	0753	3386706980751358209	30264190079963944 97	0	0	0	0	0	0	0	0	17195	0	0	0
5.R.12	0683	0490	8214565781292882689	11024811946248046337	0	0	0	0	0	0	0	0	0	0	>99999	0
6.C.15	0391	0056	3530822168830670337	10016005629588918017	0	0	0	0	0	0	0	0	0	0	0	3
6.L.06	0708	0813	1369094347692965377	51160892376650903 05	0	0	0	0	0	135	0	0	0	3333	0	0
6.L.07	0207	0843	7998392999181992449	51160892376650903 05	0	0	0	0	0	0	0	0	0	0	1045	0
7.L.01	0372	0096	1801439911918622465	14771806838746237953	0	0	0	0	0	0	0	0	10	0	0	0
8.C.03	0243	0248	8646911345521799169	47558012647938508 81	0	0	0	0	0	0	3	0	0	0	94	0
8.L.07	0130	0150	1491592202682226534 5	16573247212848061 45	0	0	0	0	0	0	1	0	0	0	23	0

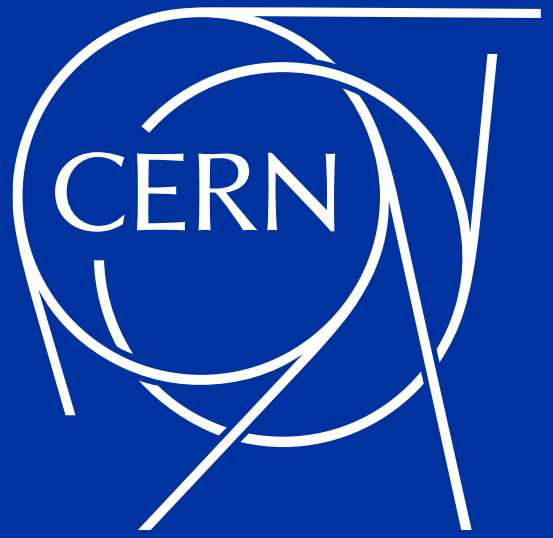


Link error vs temperature at 6L

BLMLHC Future Plan

- New surface processing electronics will be deployed during **LS3**: VFC-HD (embedded deserializer, larger/faster FPGA)
- New tunnel acquisition electronics will de deployed during **LS4** (new optical transmitter)




CERN