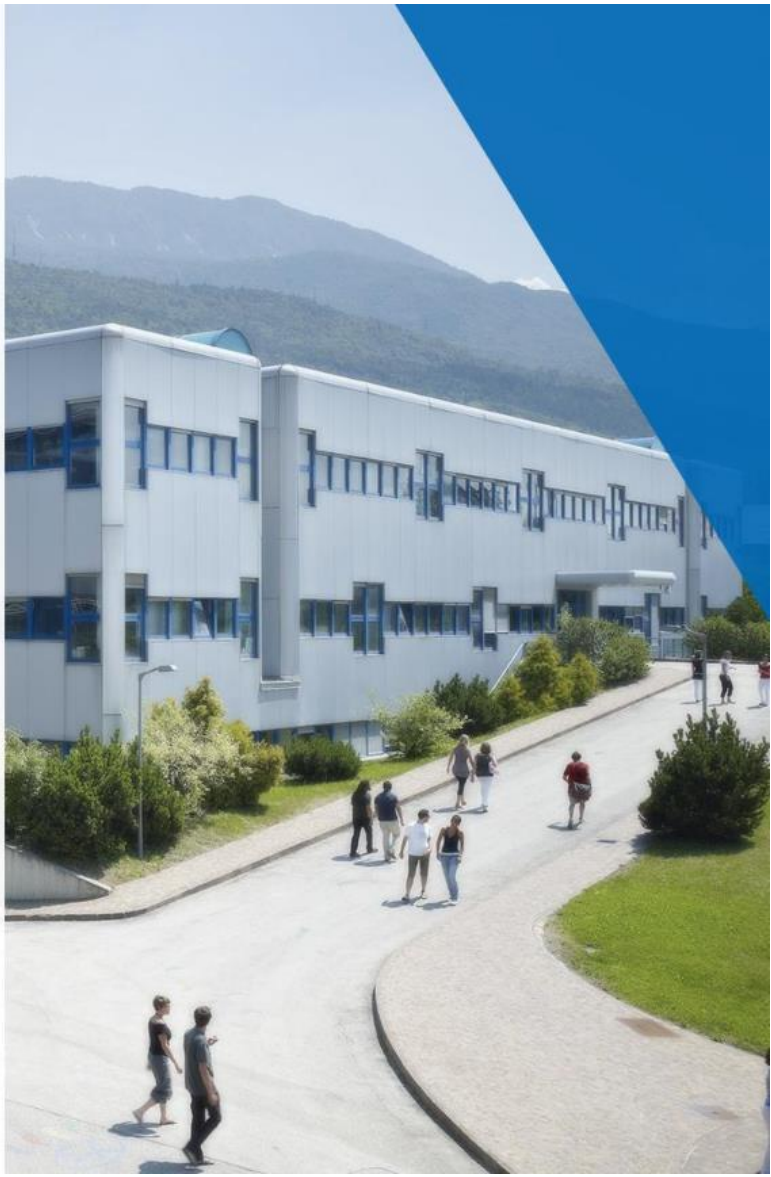
FONDAZIONE
BRUNO KESSLER

FUTURE BUILT
ON KNOWLEDGE



FONDAZIONE BRUNO KESSLER
SENSORS AND DEVICES

AIDA innova

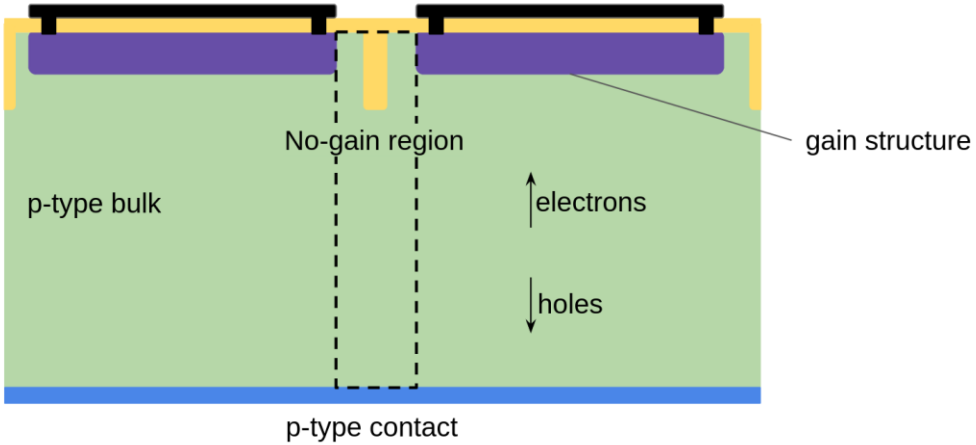
TI LGAD
FBK@AIDAinnova

Giovanni Paternoster
Matteo Centis Vignali
Maurizio Boscardin

Trench Isolated LGADs @ AIDAinnova

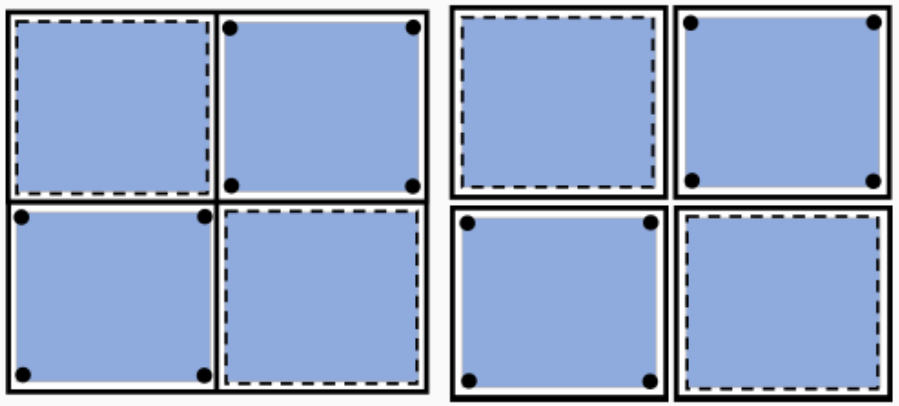
- The goal is to realize an LGAD compatible with small pitch (55micron or less) and with high fluences
  - Isolation made by trenches
  - Carbon co-implantation to increase radiationa hardness

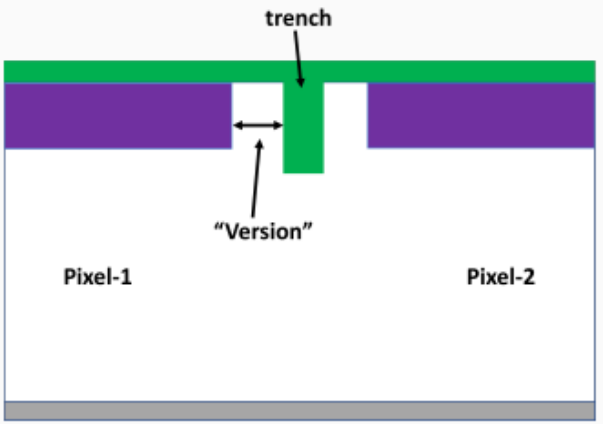
- Previus exeperiece
  - Internal FBK batches
  - Batches in RD50



SENSORS AND DEVICES
FONDAZIONE BRUNO KESSLER

Trench Isolated LGADs @ AIDAinnova





- 1-Trench
- 2-Trenches
- Contact Types: Ring/Dots
- Inter-Pixel Distance (IPD):
  → defined as the no-gain region between the pixels

Versions:

- V1, V2, V3, and V4
- V1 → Aggressive
- V4 → Safe

https://agenda.infn.it/event/39042/contributions/221974/attachments/116396/167772/tredi24_BishtAshish.pdf

Trench Isolated LGADs @ AIDA Process

- **12 wafers**
- **Main process**
  - 45 µm, D2 , P2 and «high diffusion»

Split on

✓ Wafer thickness
✓ With or without carbon (it's the first time that we use carbon on TiLGAD)
✓ Trench Depth
✓ Trench Process

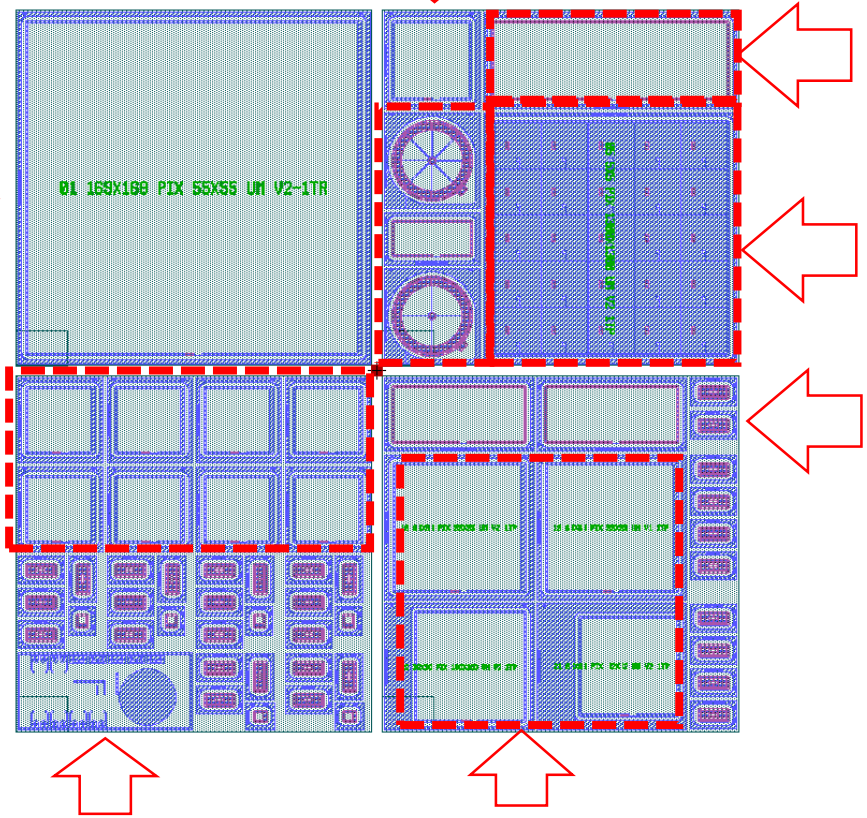
Note : two wafer per «main» split

Table splits

Wafer	Thickness	Carbon	Trench depth	Trench process
1	45	Y	D2	P2
2	45	Y	D2	P2
3	45	Y	D1	P2
4	45	Y	D1	P1
5	45	Y	D2	P1
6	45		D2	P2
7	45		D2	P2
8	45		D1	P1
9	55	Y	D3	P2
10	55	Y	D2	P2
11	55	Y	D2	P2
12	55		D2	P2

Trench Isolated LGADs @ AIDAinnova
Layout

50x50 pixels 42µm pitch



169x168 pixels
55 µm pitch

32x32 pixel, 55 um pitch
study of the border versions, with 1 or 2 trenches

Strip sensors

5x5 pixels
1300µm pitch

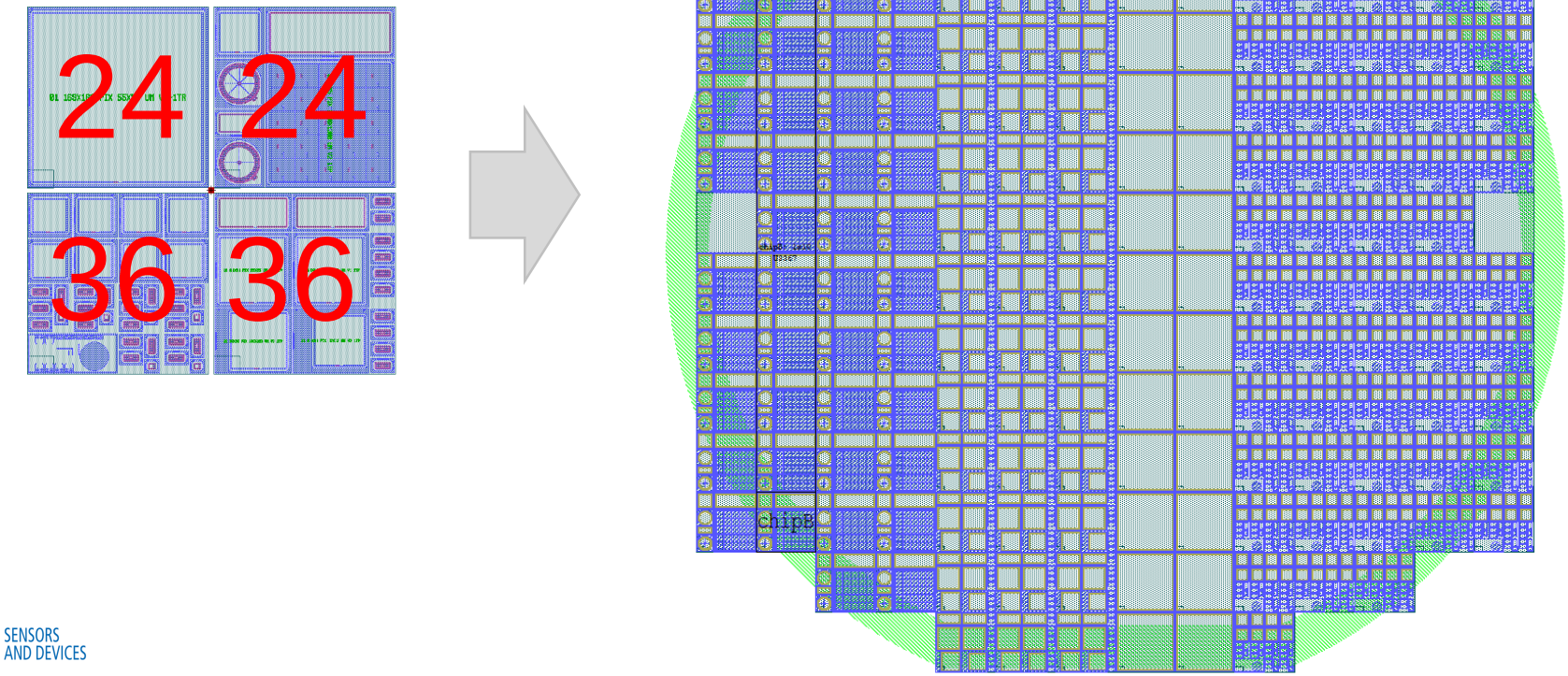
15 strip
100um pitch

Process Control Monitor Fbk

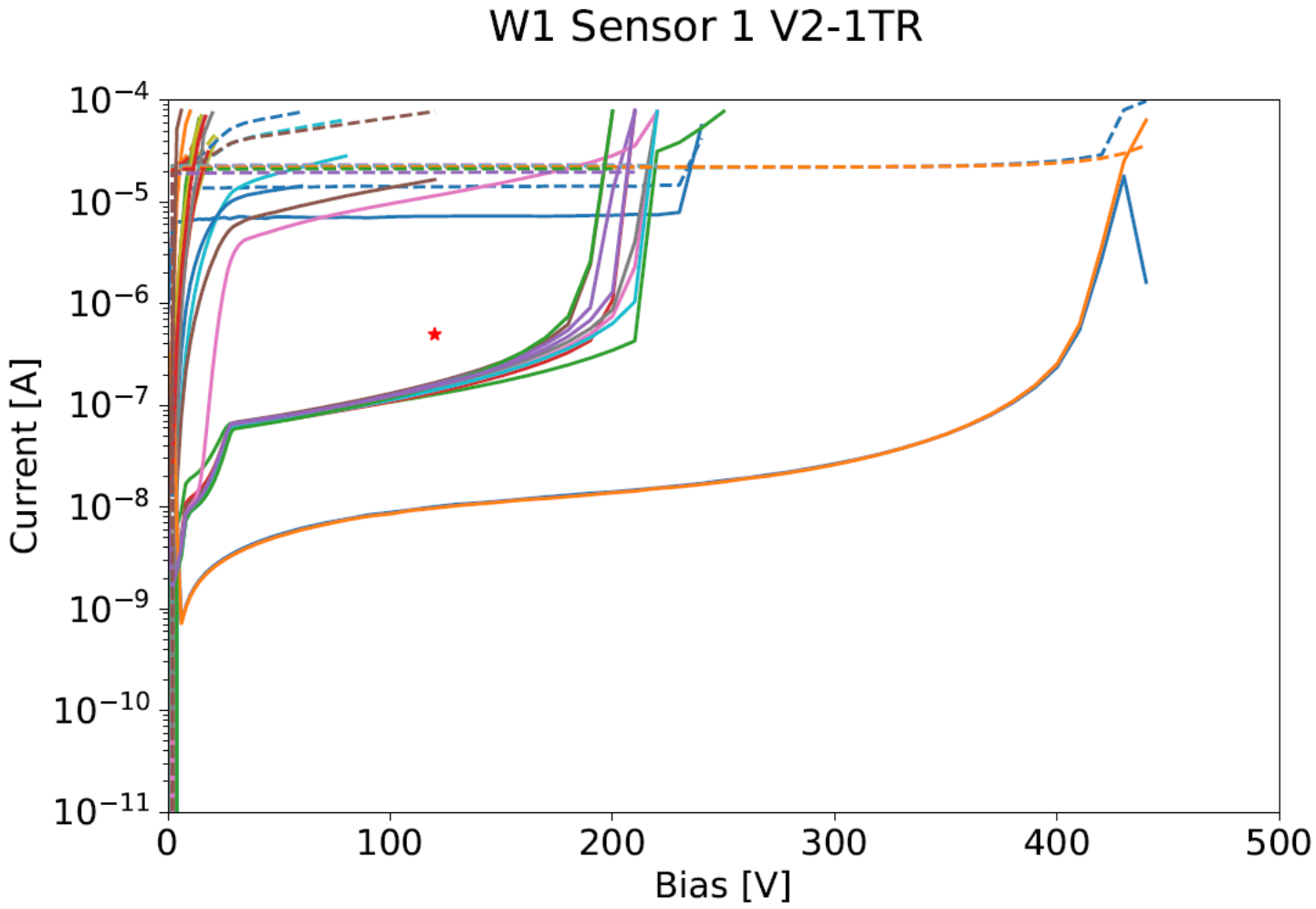
Pixel 100, 55, 42 um pitch
study of different sensor pitch and fill factor

Trench Isolated LGADs @ AIDAinnova
Wafer Layout

- the wafers are divided into a regular grid (1cm^2)
- in each column are printed the same quarter of the reticle



IV large sensors W1



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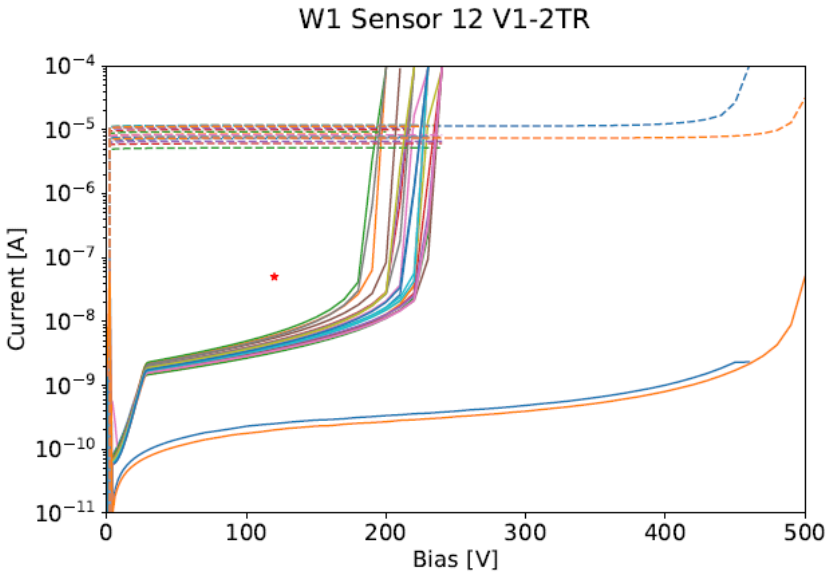
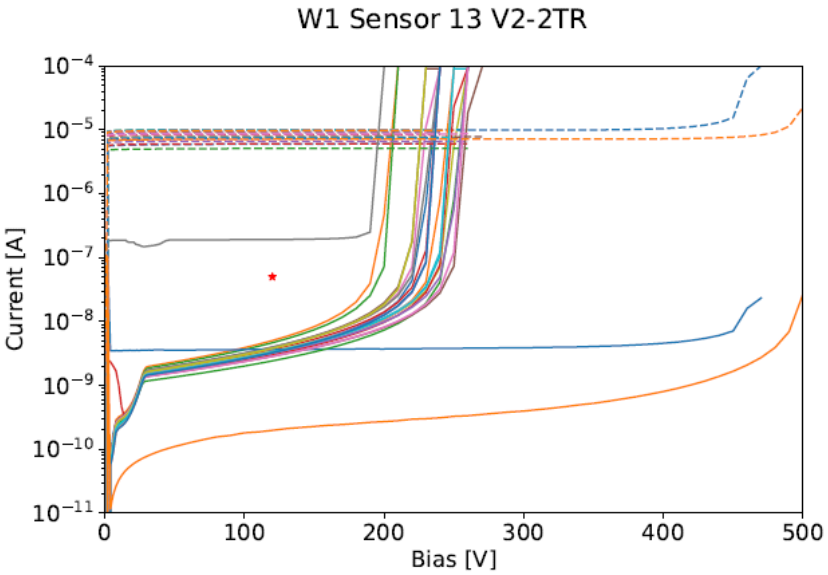
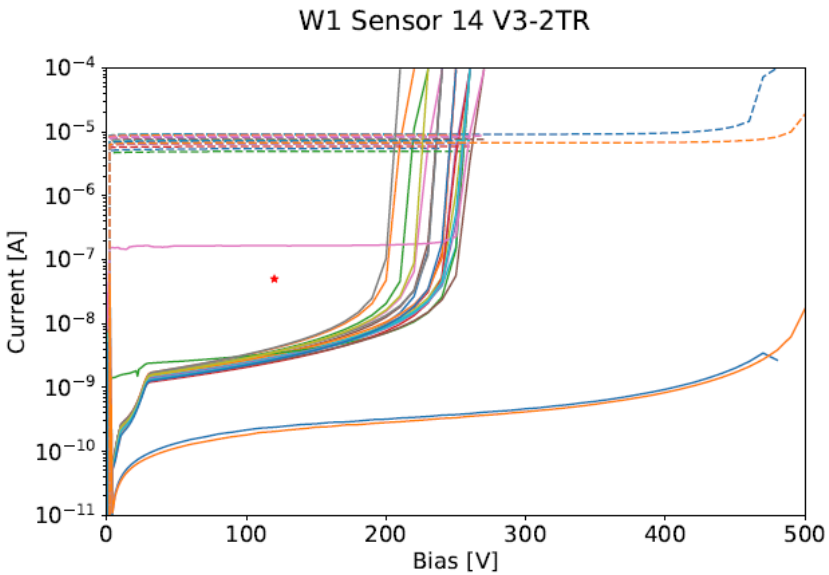
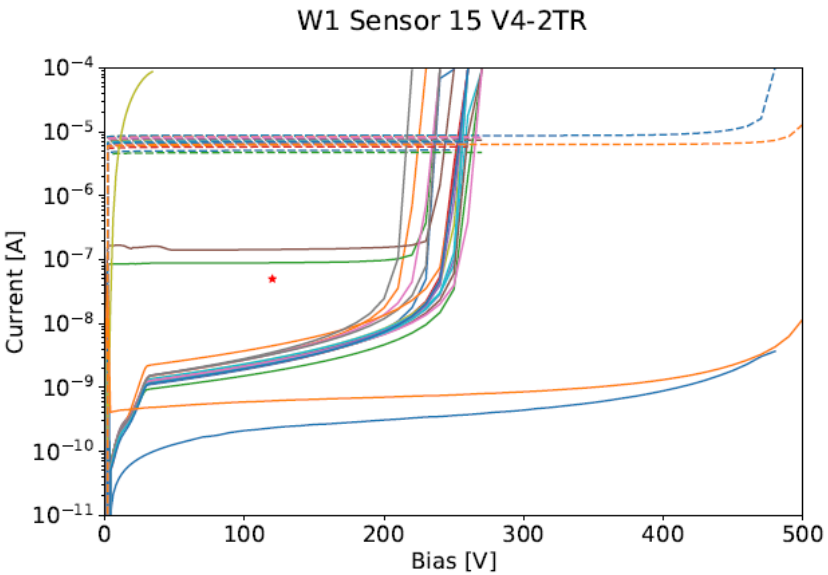
IV small sensors W1

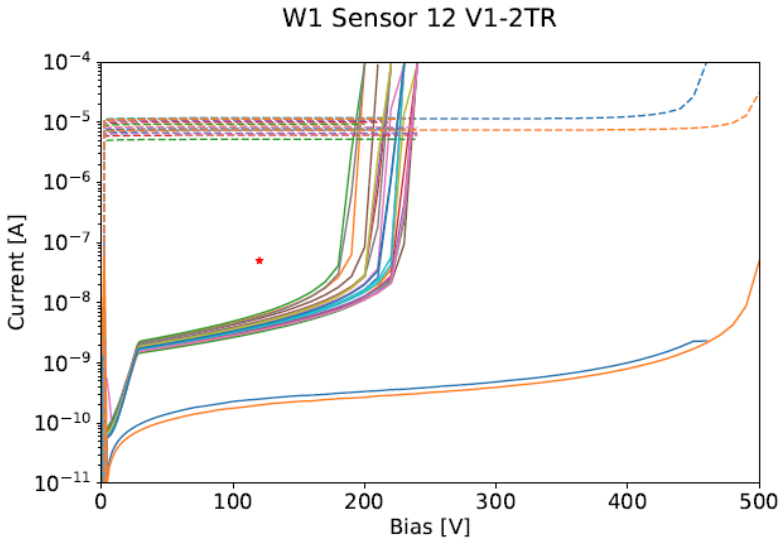


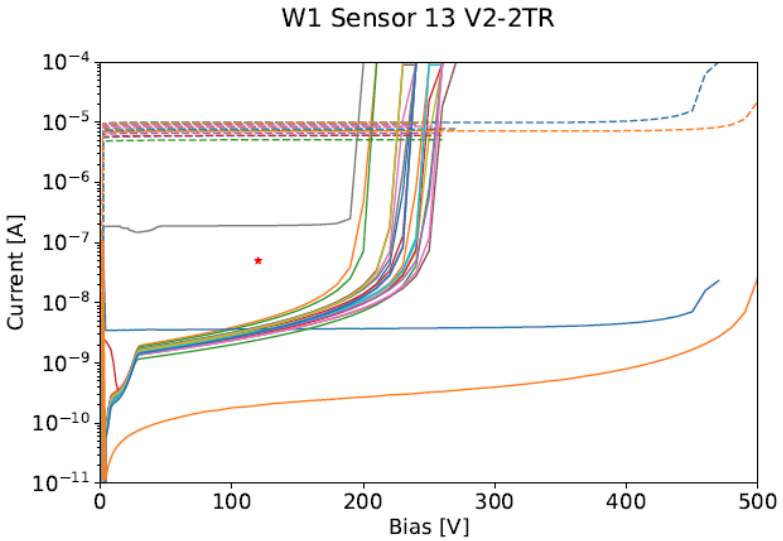


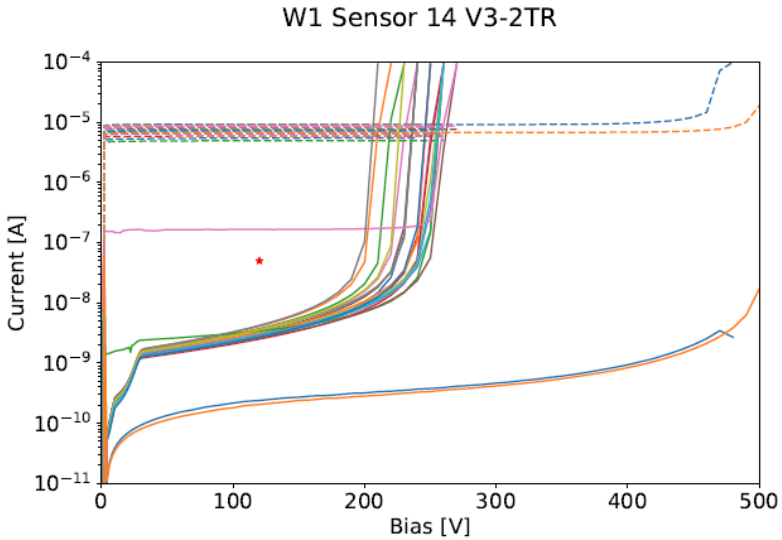


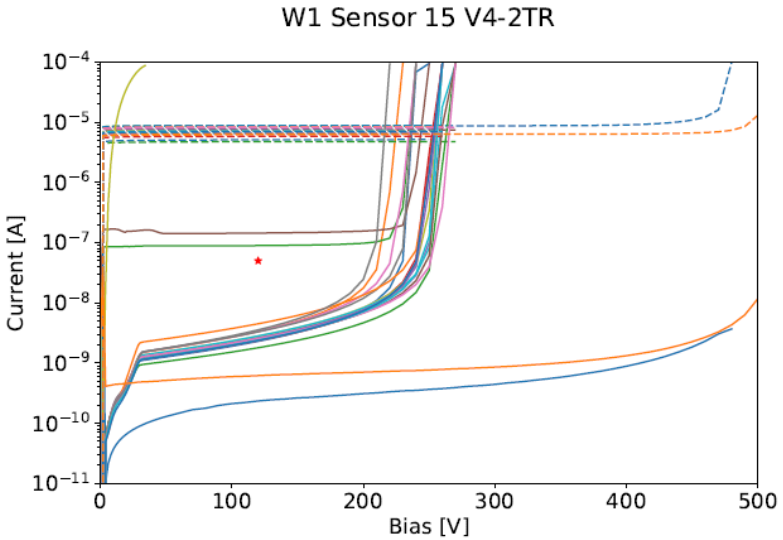


IV small sensors W1









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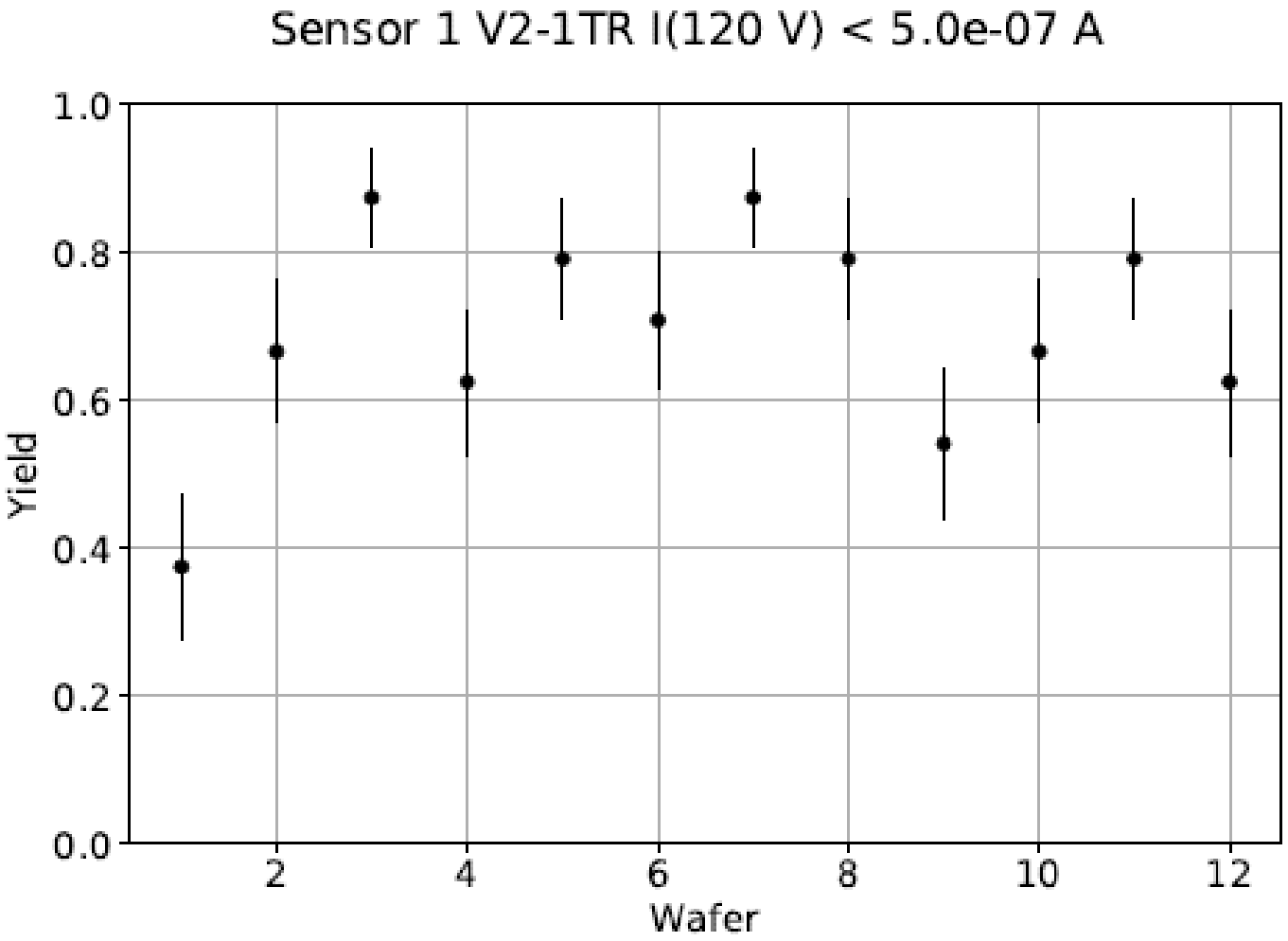
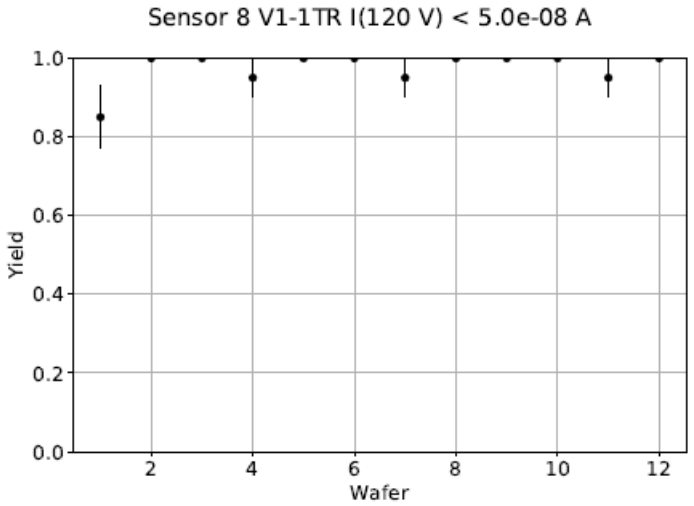
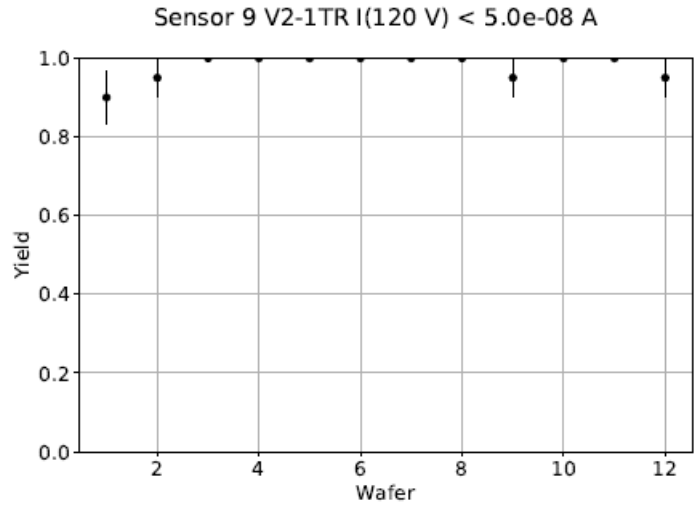
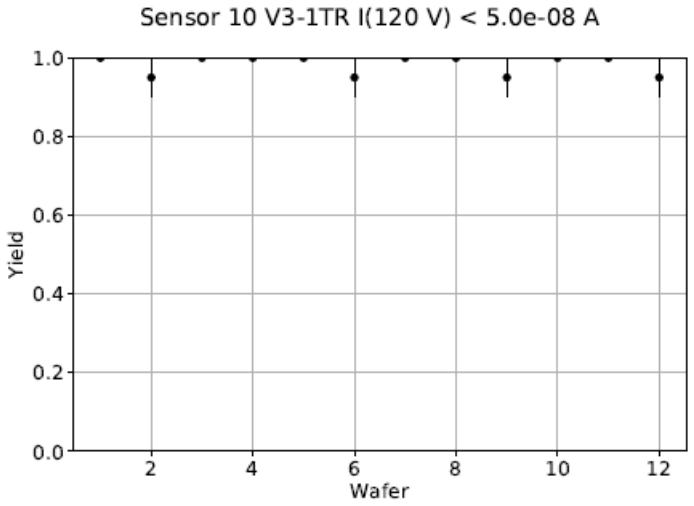
Yield Large Sensors

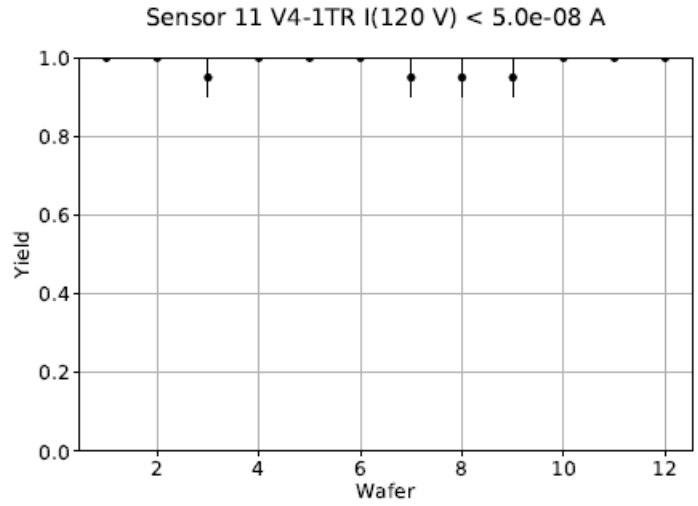


Yield Small Sensors

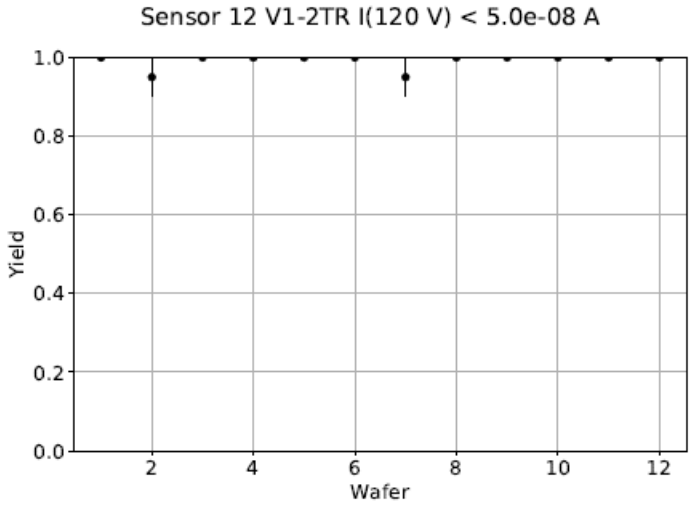


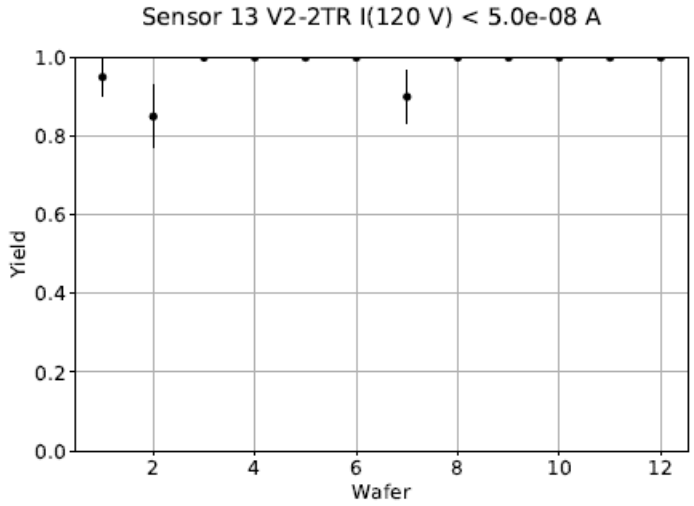


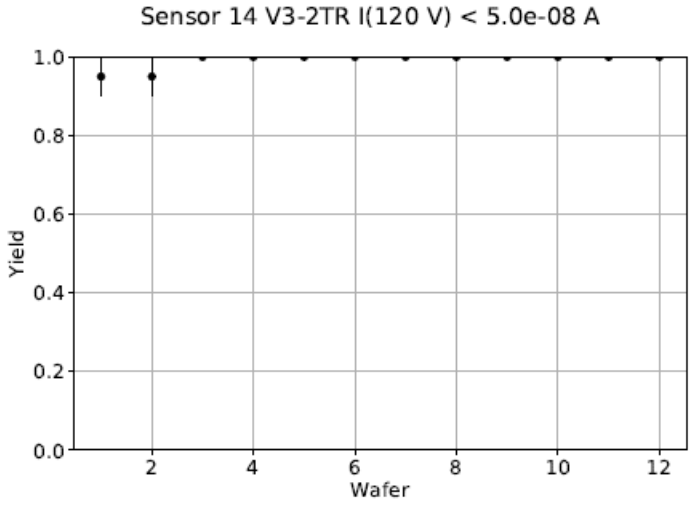


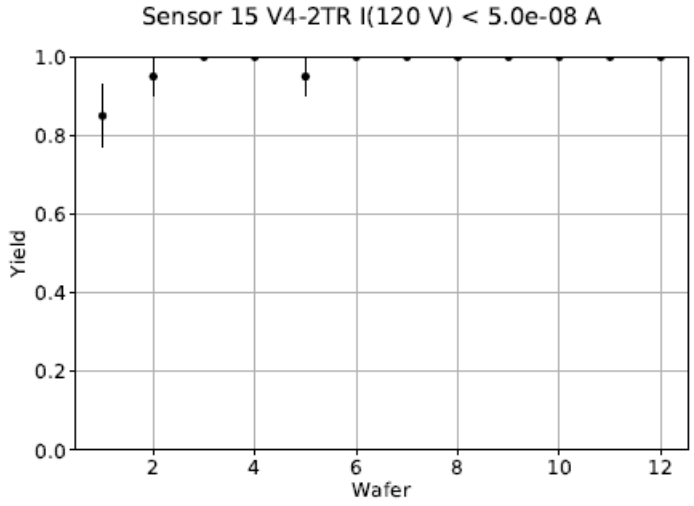


Yield Small Sensors

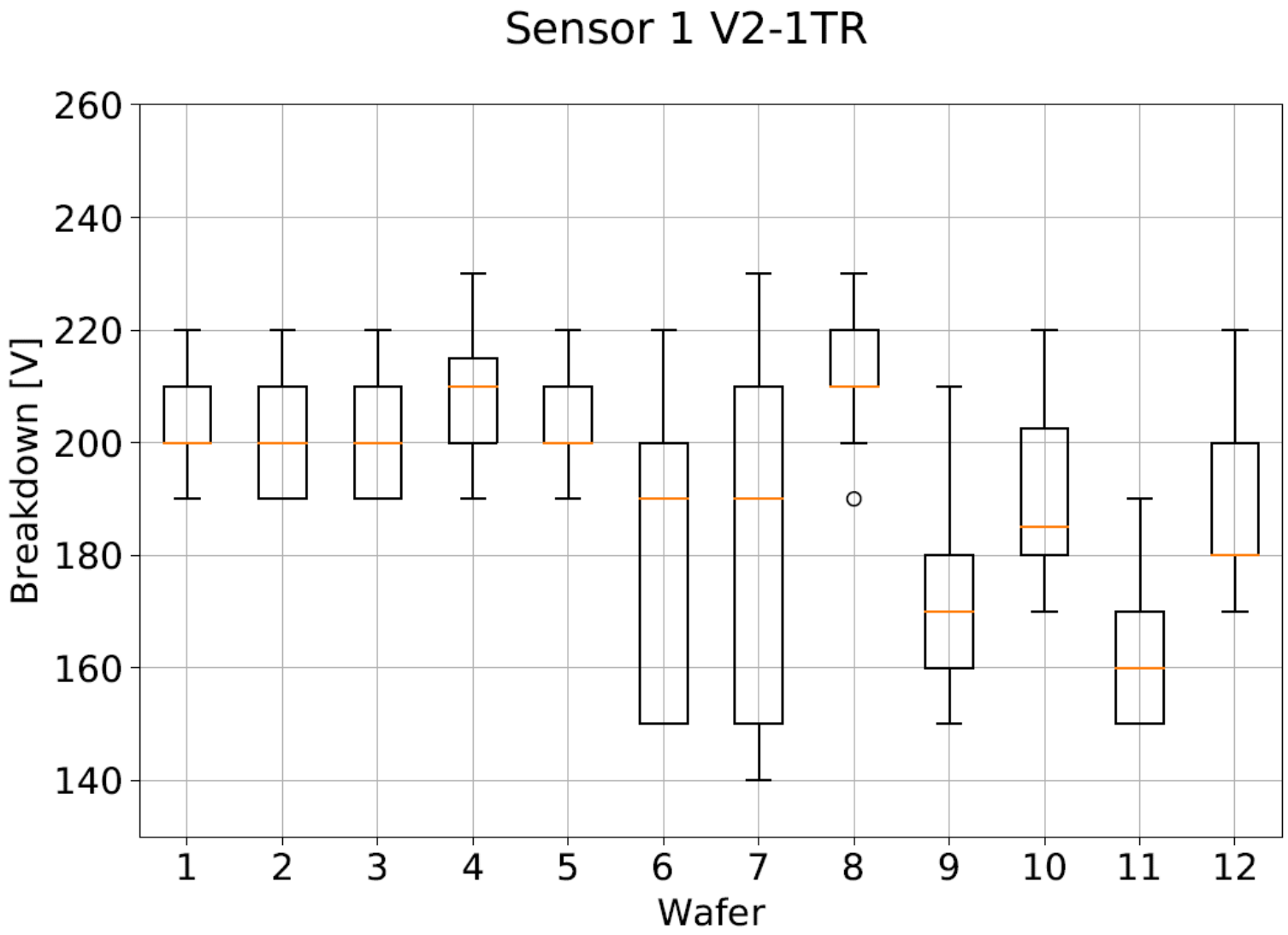




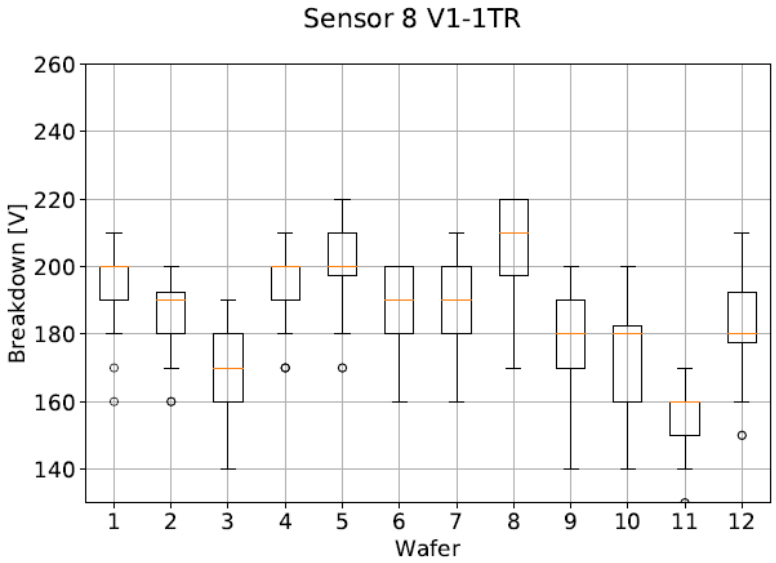


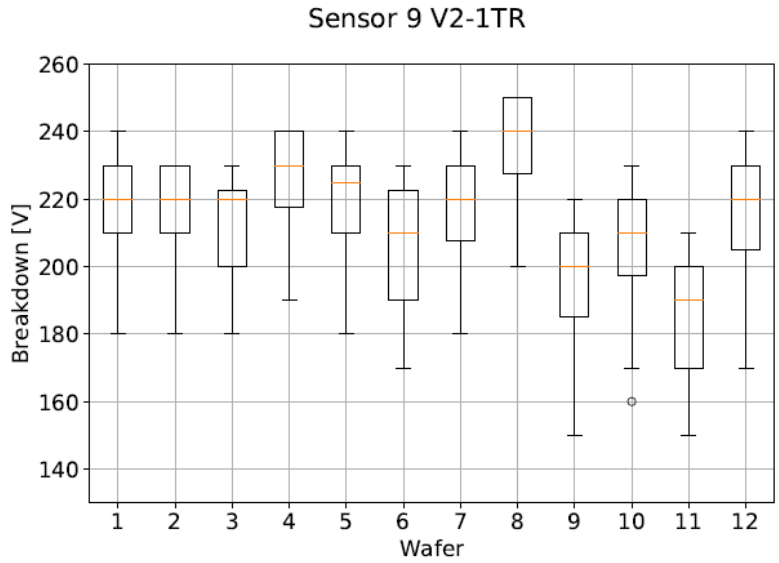


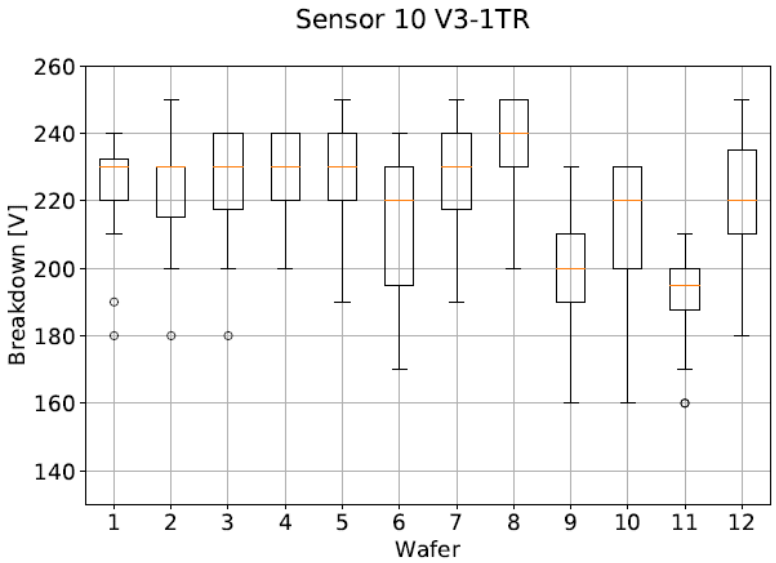
Breakdown Large Sensors

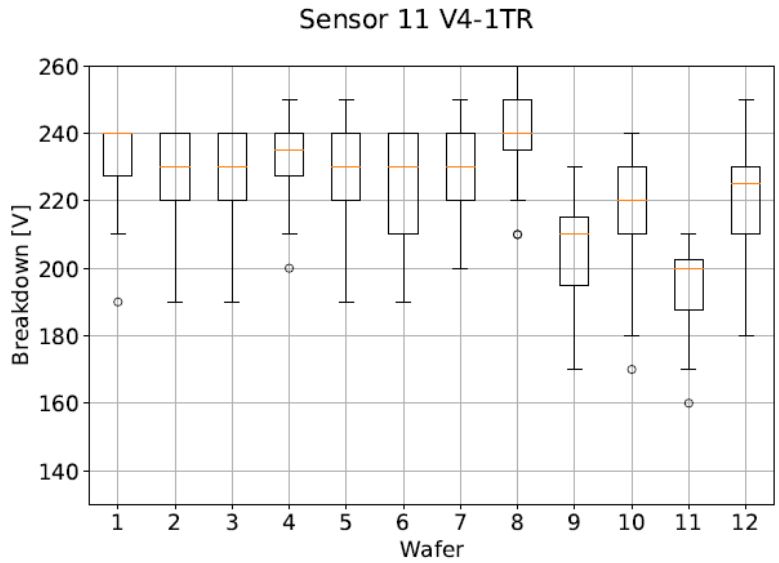


Breakdown Small Sensors









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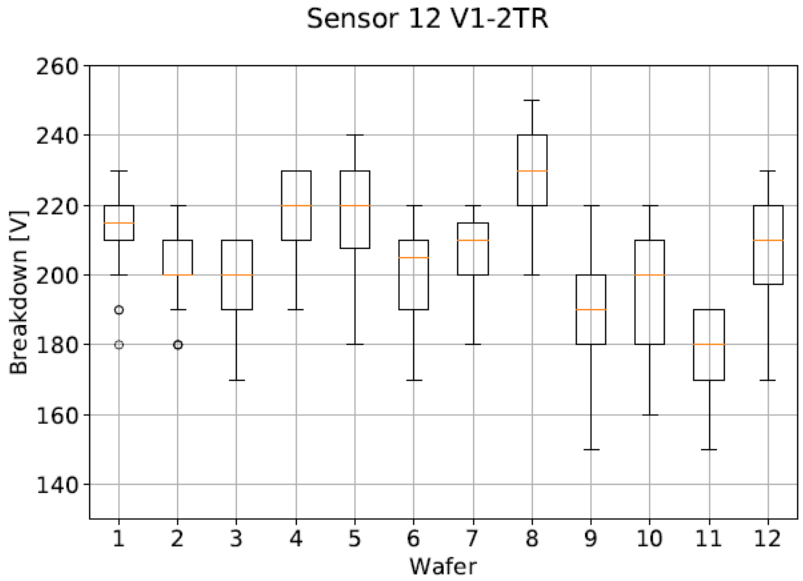
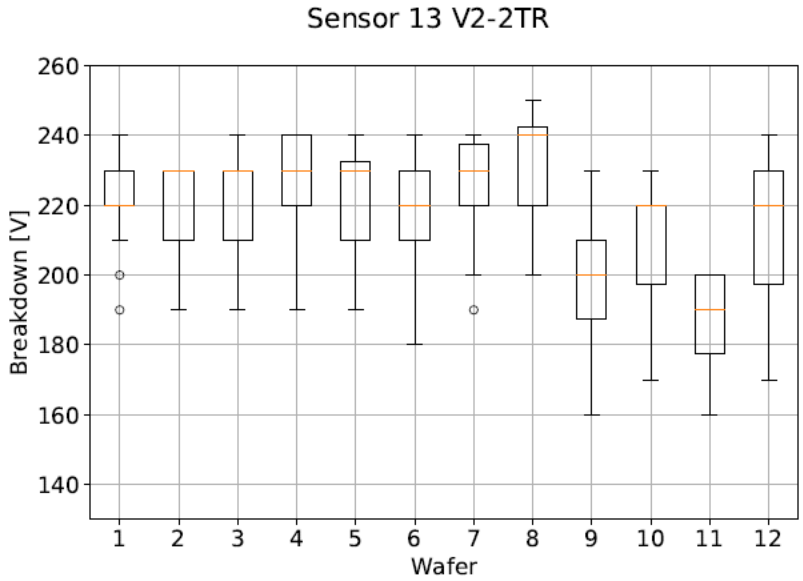
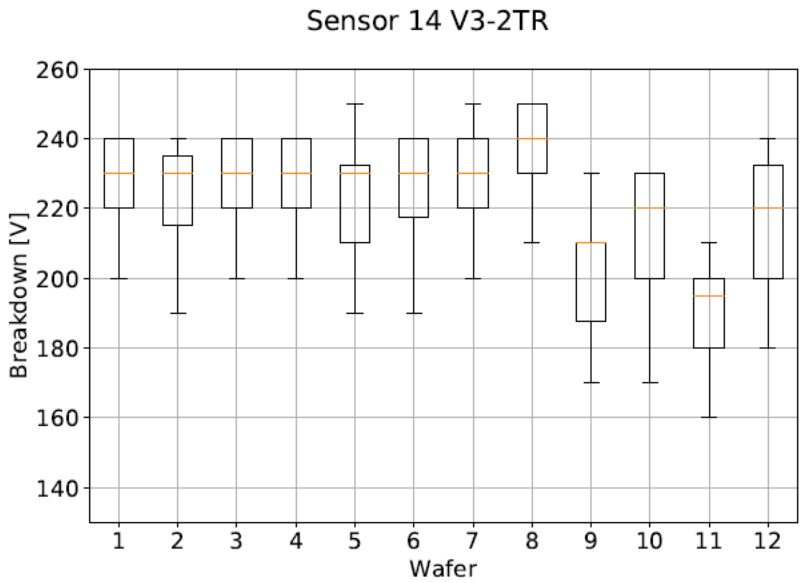
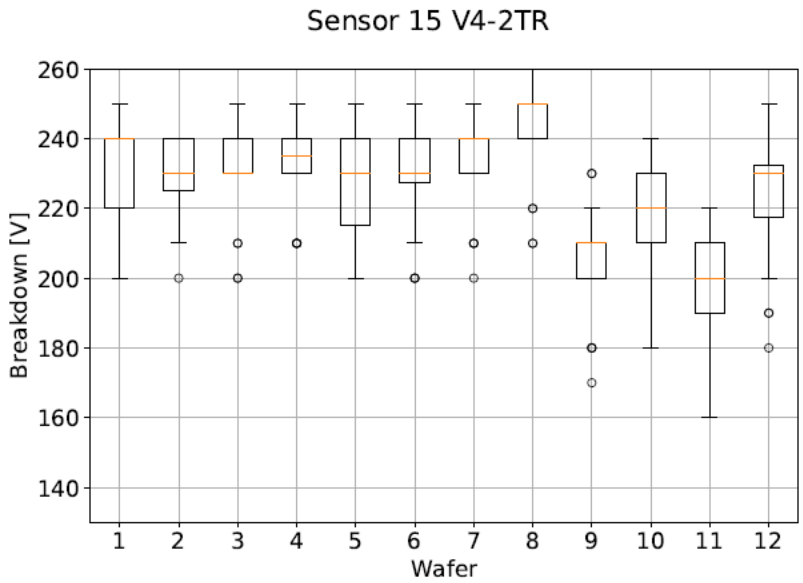
Breakdown Small Sensors



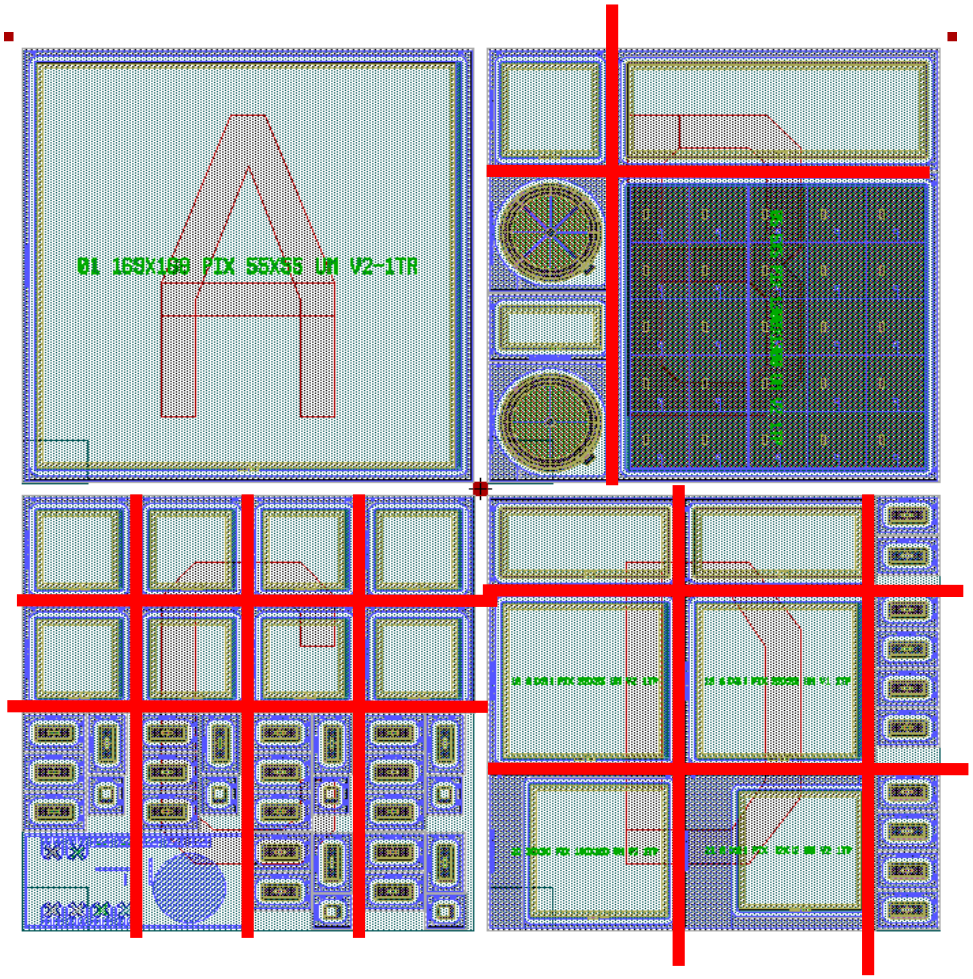






TiLGAD conclusion

- W1 diced and distributed
- W6 and w10 are dicing
- If you need samples ask Anna



SENSORS AND DEVICES
FONDAZIONE BRUNO KESSLER

FONDAZIONE BRUNO KESSLER | SENSORS AND DEVICES

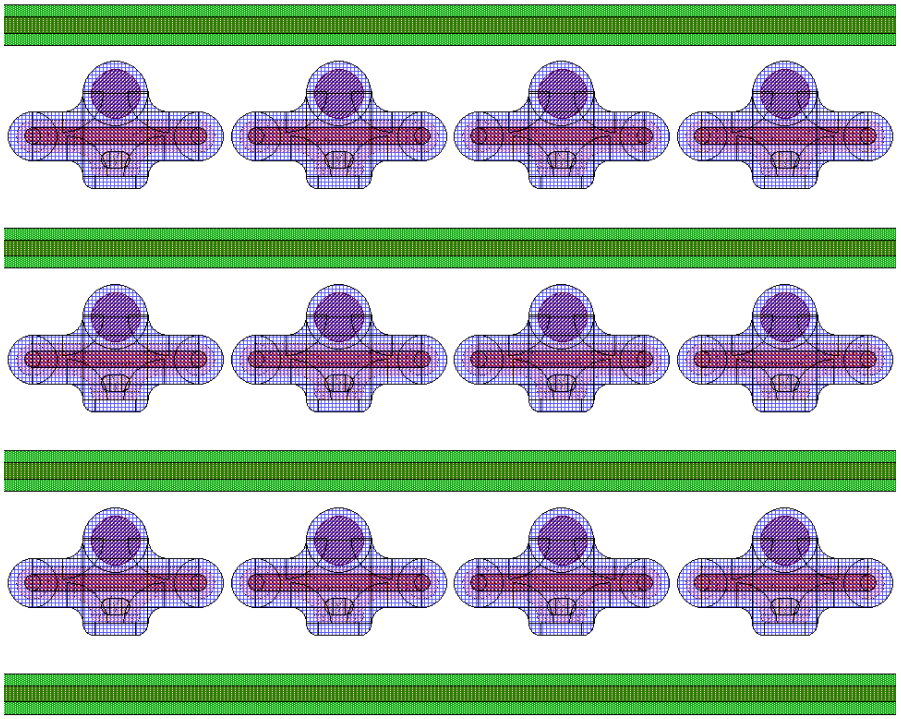
AIDA innova

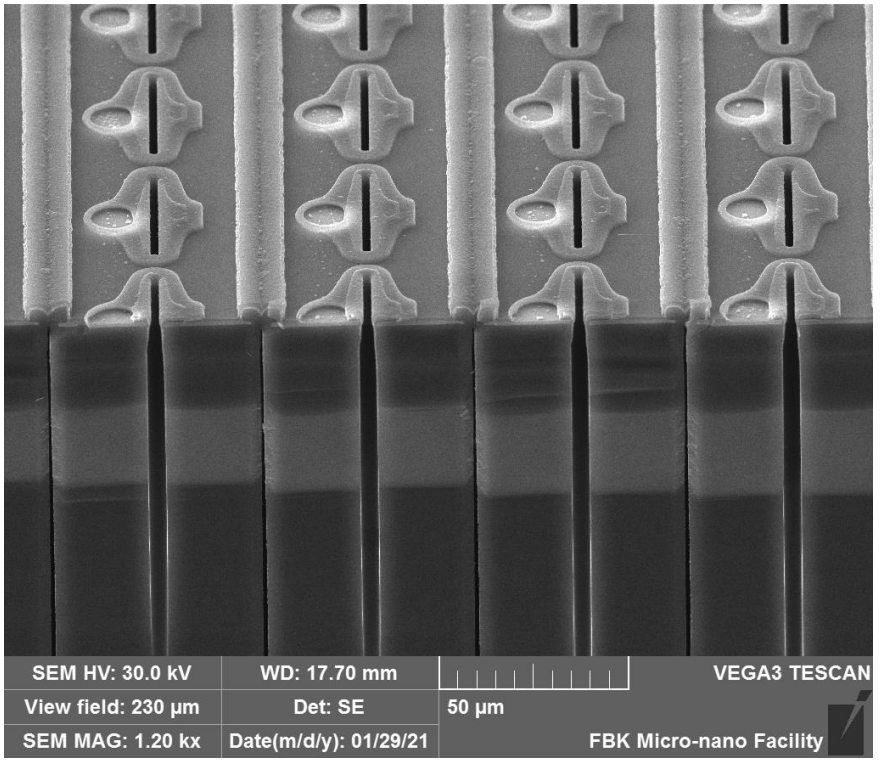
Si 3D
FBK@AIDAinnova

Laura Parellada Monreal
Sabina Ronchin
Maurizio Boscardin

Si-3D @ AIDAinnova

- Based on trench electrode
- Best performance for timing
- Develop in partnership with INFN Collaboration

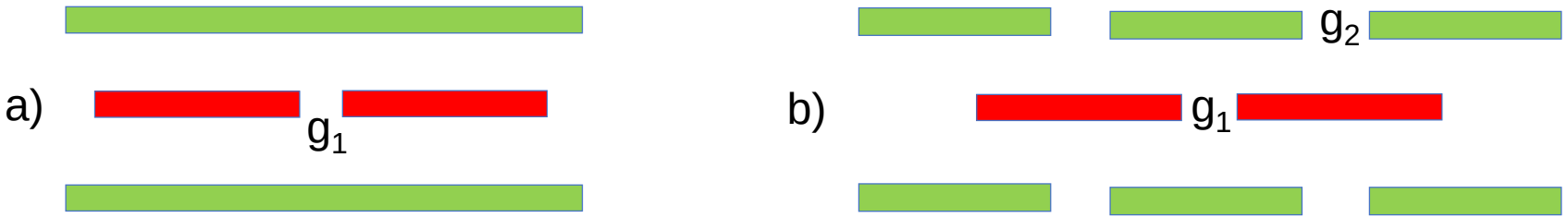




SENSORS AND DEVICES
FONDAZIONE BRUNO KESSLER

Si-3D @ AIDAinnova
Layout 1

- 3D-trenched pixels only (no columns)
- Continuous ohmic trench (a) vs dashed ohmic trench (b)

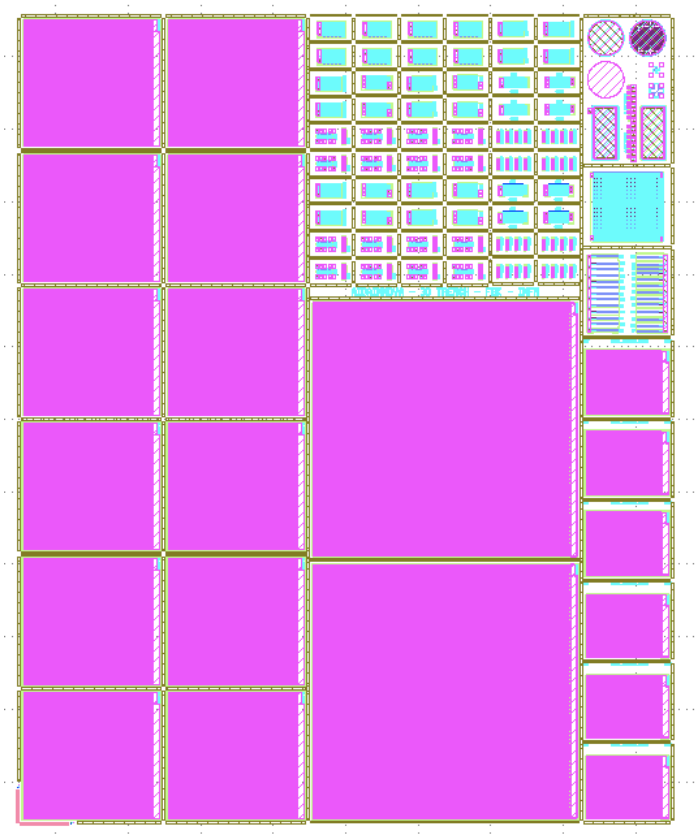


- Test structures (single/multiple pixels, strips, diodes, including 42 μm pitch)
- Pixel sensors (55 μm pitch)

Thanks to G.F. Dalla Betta

Si-3D @ AIDAinnova
Layout 2

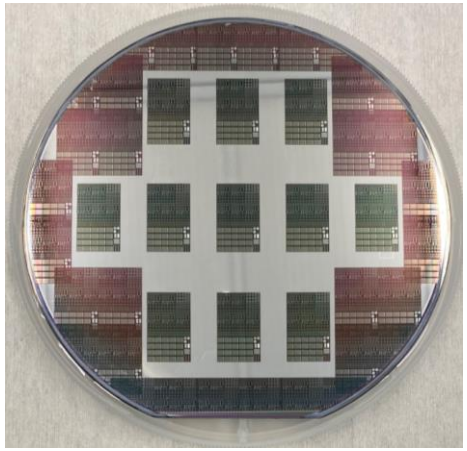
- **Pixel sensors (55 μm pitch)**
  - 32x32 pixels, multiplicity = 6 (3 std, 3 dashed)
  - 64x64 pixels, multiplicity = 12 (6 std, 6 dashed)
  - 128x128 pixels, multiplicity = 2 (1 std, 1 dashed)
- **Device test structures (55 μm pitch and 42 μm pitch, std and dashed)**
  - Groups of individual pixels
  - Strips
  - Diodes
- **Technological test structures**



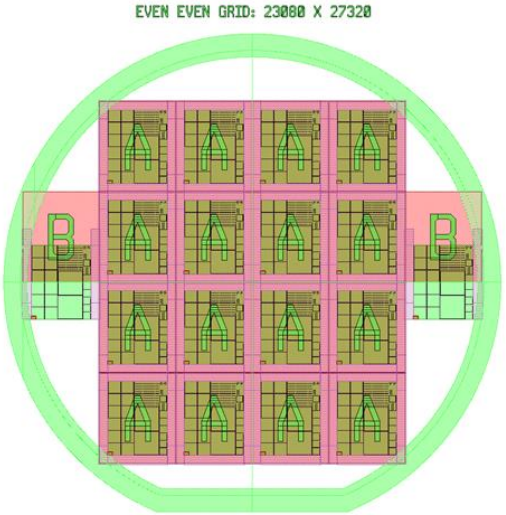
Thanks to G.F. Dalla Betta

Si-3D @ AIDAinnova
wafer layout

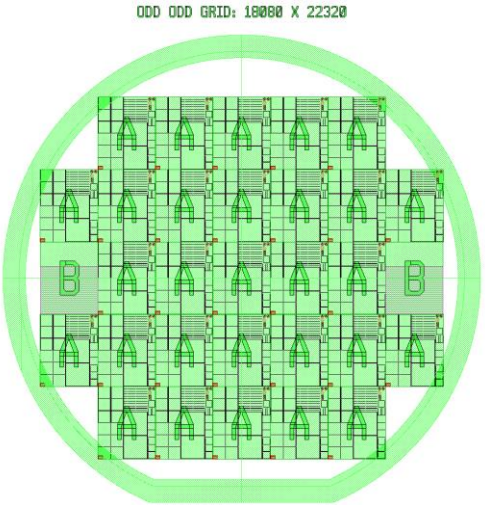
- Test on going to increase the exposure shot on wafers
- Increase the trench density increase the wafer bow
- Wafer layout split
  - 4 «full» : 2BPSG +2poly



Old wafer layout
11 shot exposure



18 shot exposure



29 shot exposure

Sabina Ronchin, Tredi 2024

p-holes: two geometries

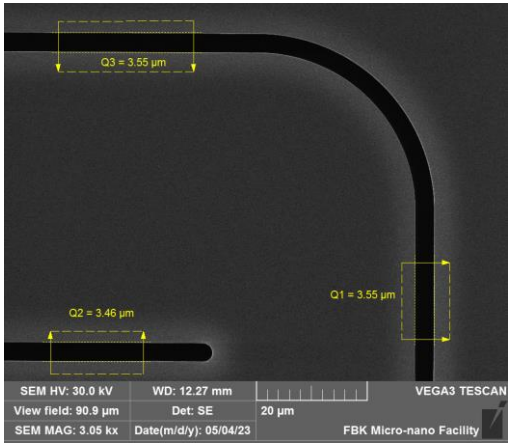
Short and narrow trenches to improve subsequent lithography process

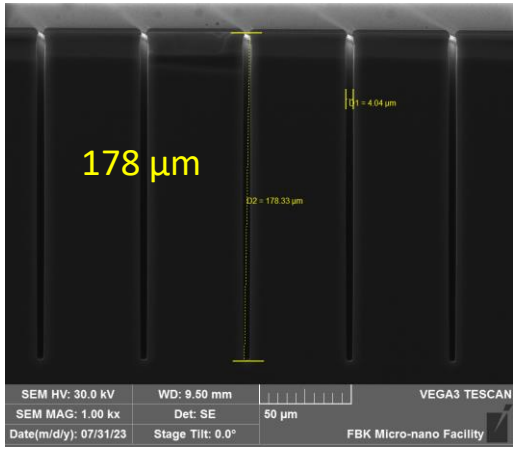
3D AIDA

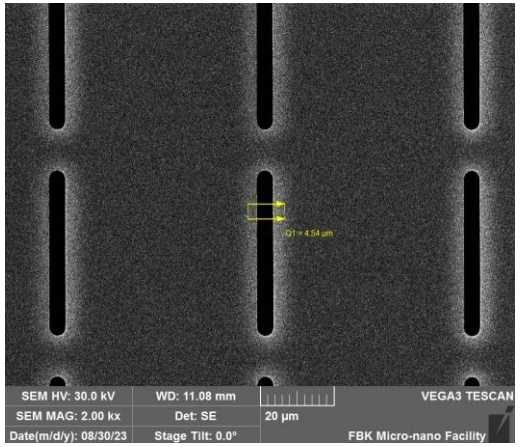
Previous process:
trenches
4µm x ∞

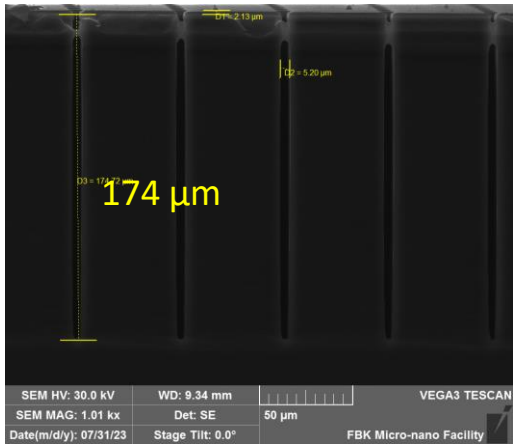
Long trenches:
3µm x ∞

Short trenches:
4 µm x 40 µm





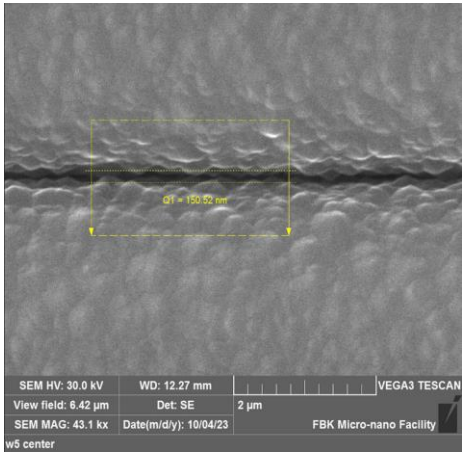




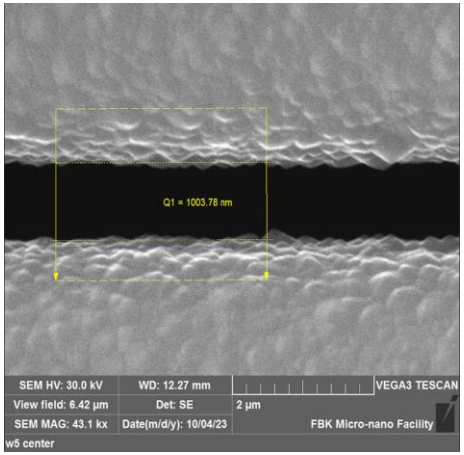
Sabina Ronchin, Tredi 2024

p-holes filling with poly silicon

Long wide trenches and thick poly cap induce lithography issues



Long 3um trench

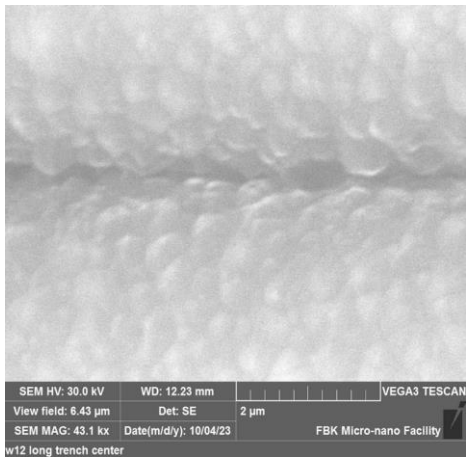


Short 4um trench

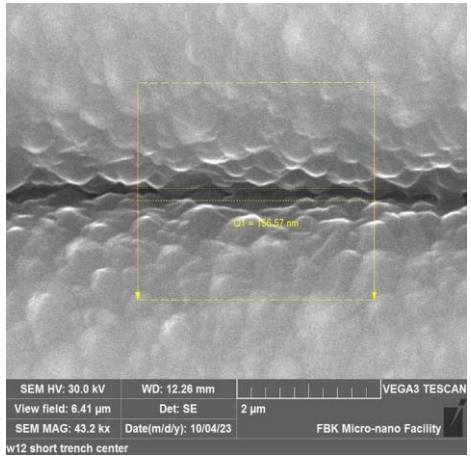
Poly-Si 2 µm

- Long 3um trenches: almost completely closed.
- Short 4um trenches: open. Remaining opening width of **1um**.

Added other 1 µm of poly-Si and all trenches have been closed



Long 3um trench



Short 4um trench

Poly-Si 2.5 µm

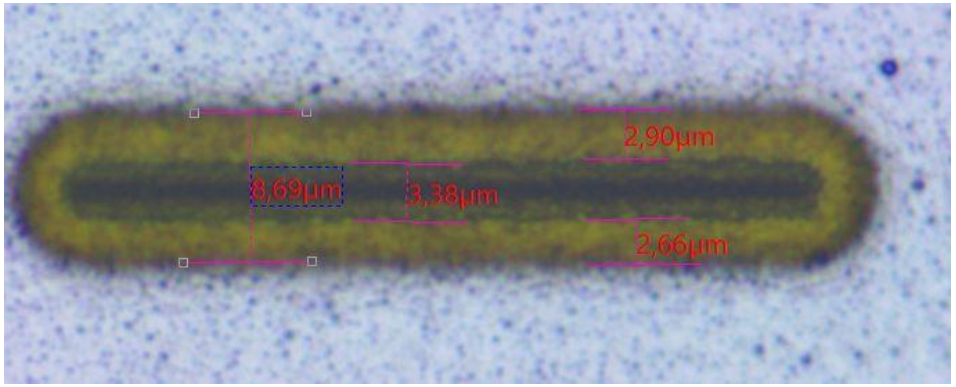
- Long 3um trenches: closed.
- Short 4um trenches: almost completely closed.

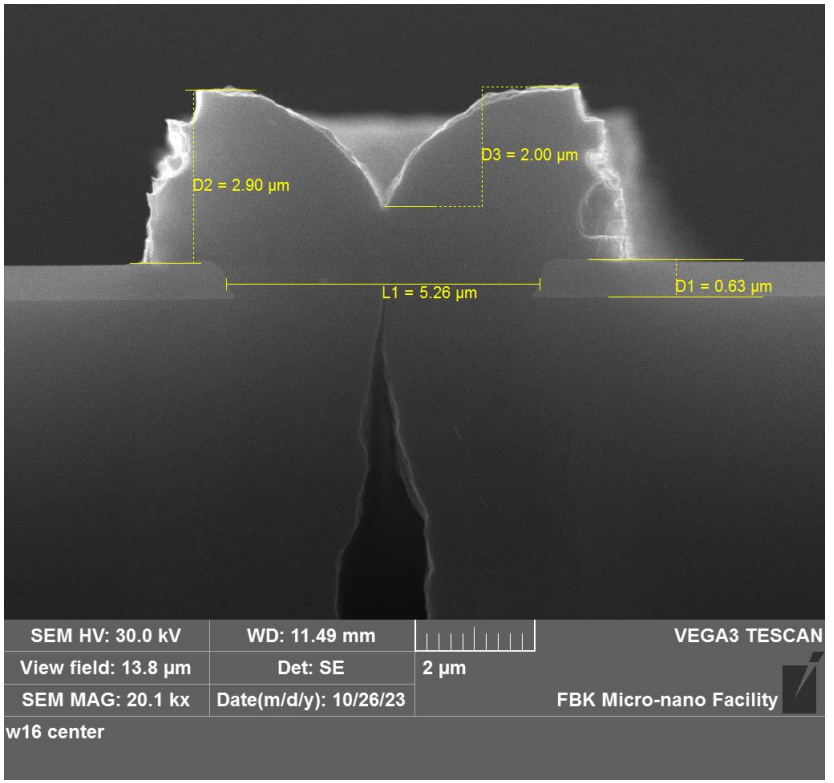
We kept them as they were at the first deposition

Poly Trench filling and definition
Cross section

W16 (broken) layout 29 DIE with:

3 µm thickness on 4 µm trenches





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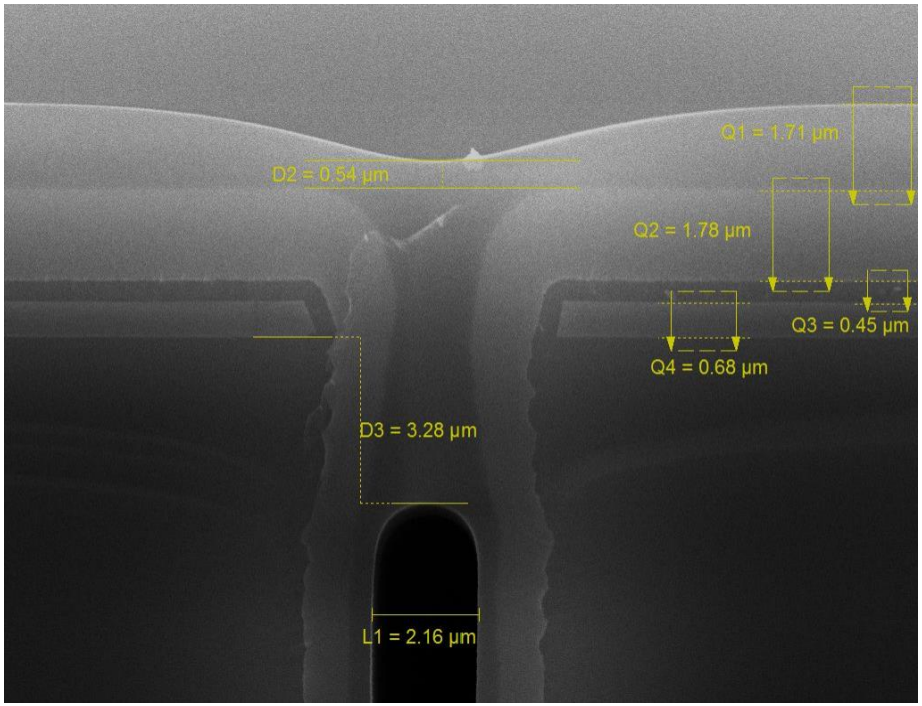
BPSG Trench filling Cross section

Test wafer with:

2.3 µm thickness on 4 µm trenches

“poly cap” is less thick and smoother with

the trench better closed



BPSG filling

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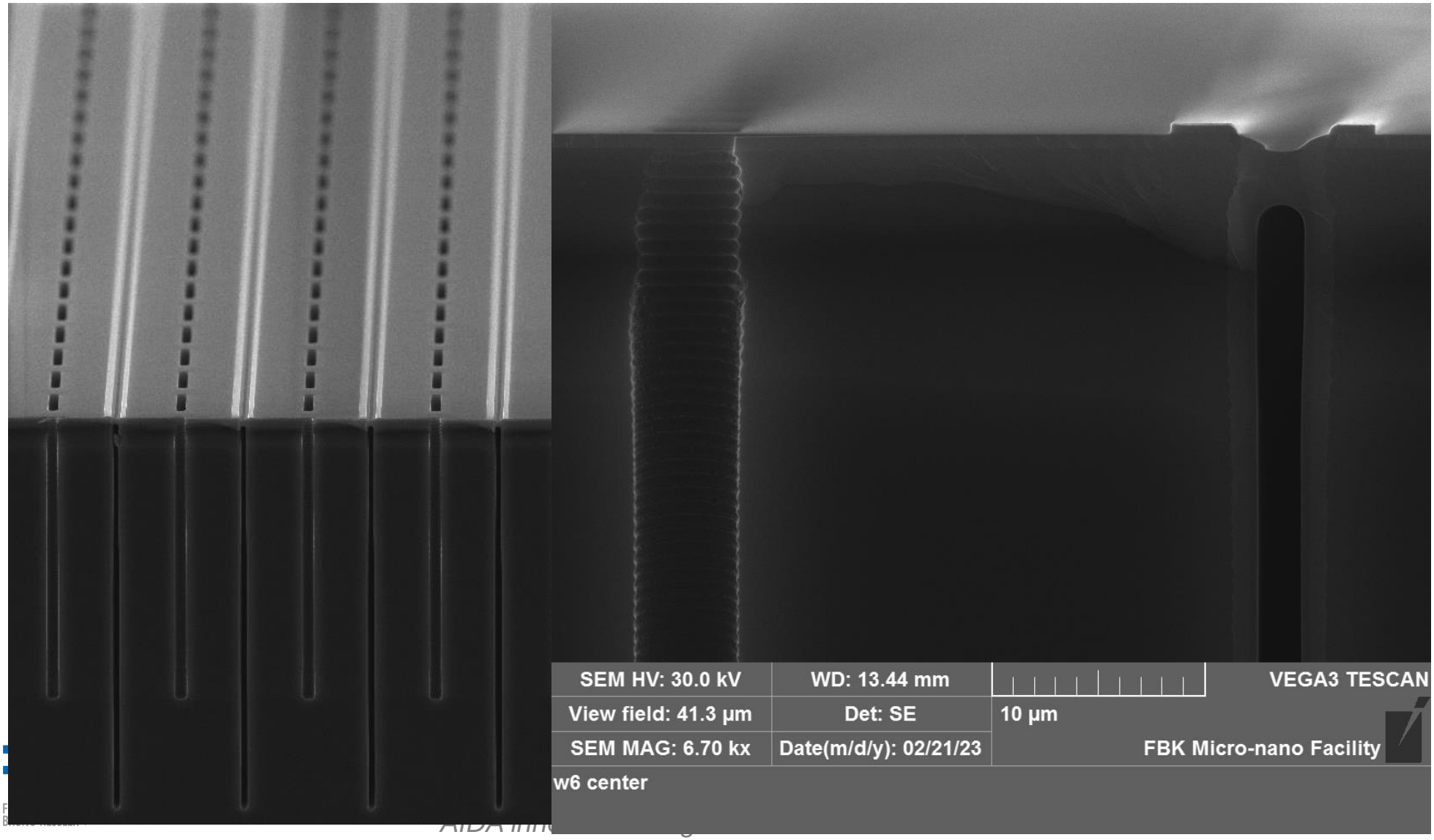
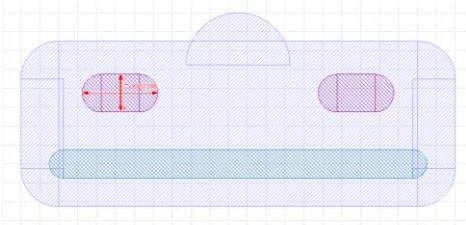
Si-3D @ AIDAinnova
test : p-trenches filling

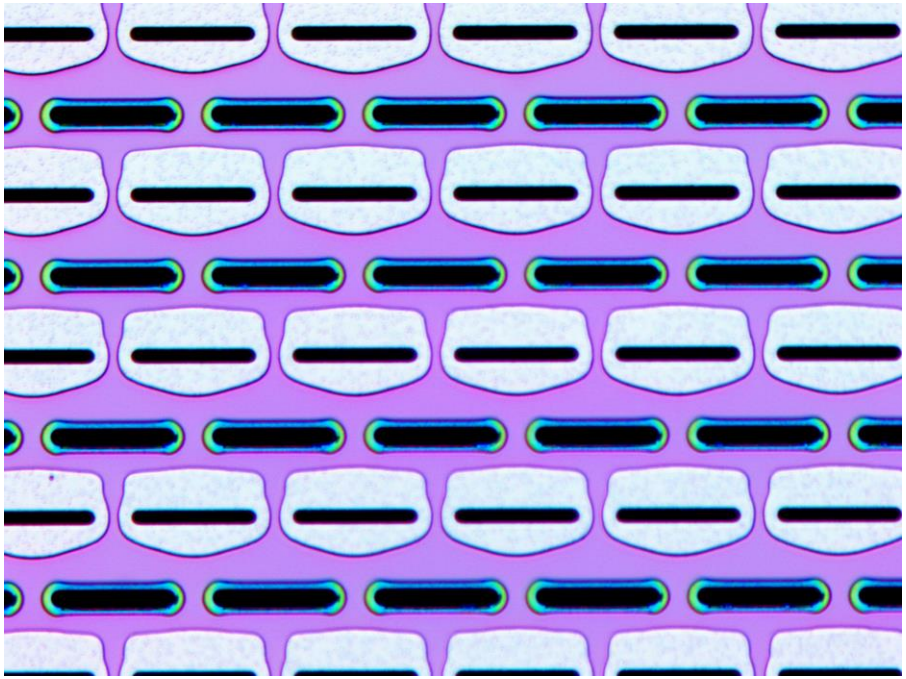


N-Poly Litho Optimization & Contact lithography

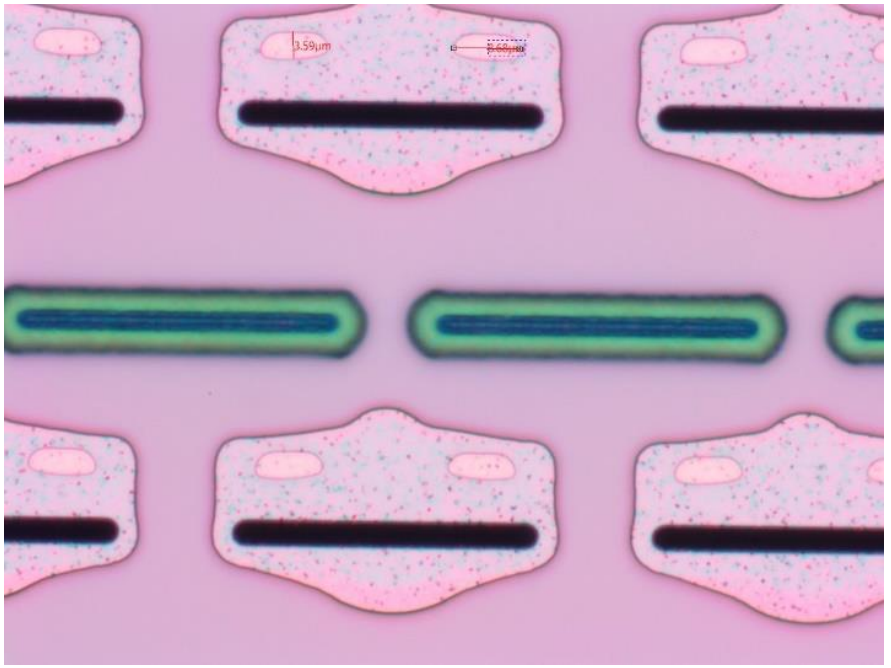
Designed pixel layout



Poly Definition



Contact Definition



We had to accept a slight deformation, obtaining really nice frog!

Contact from 4x8 to 3.5x8.7 → **Ok for device!!**

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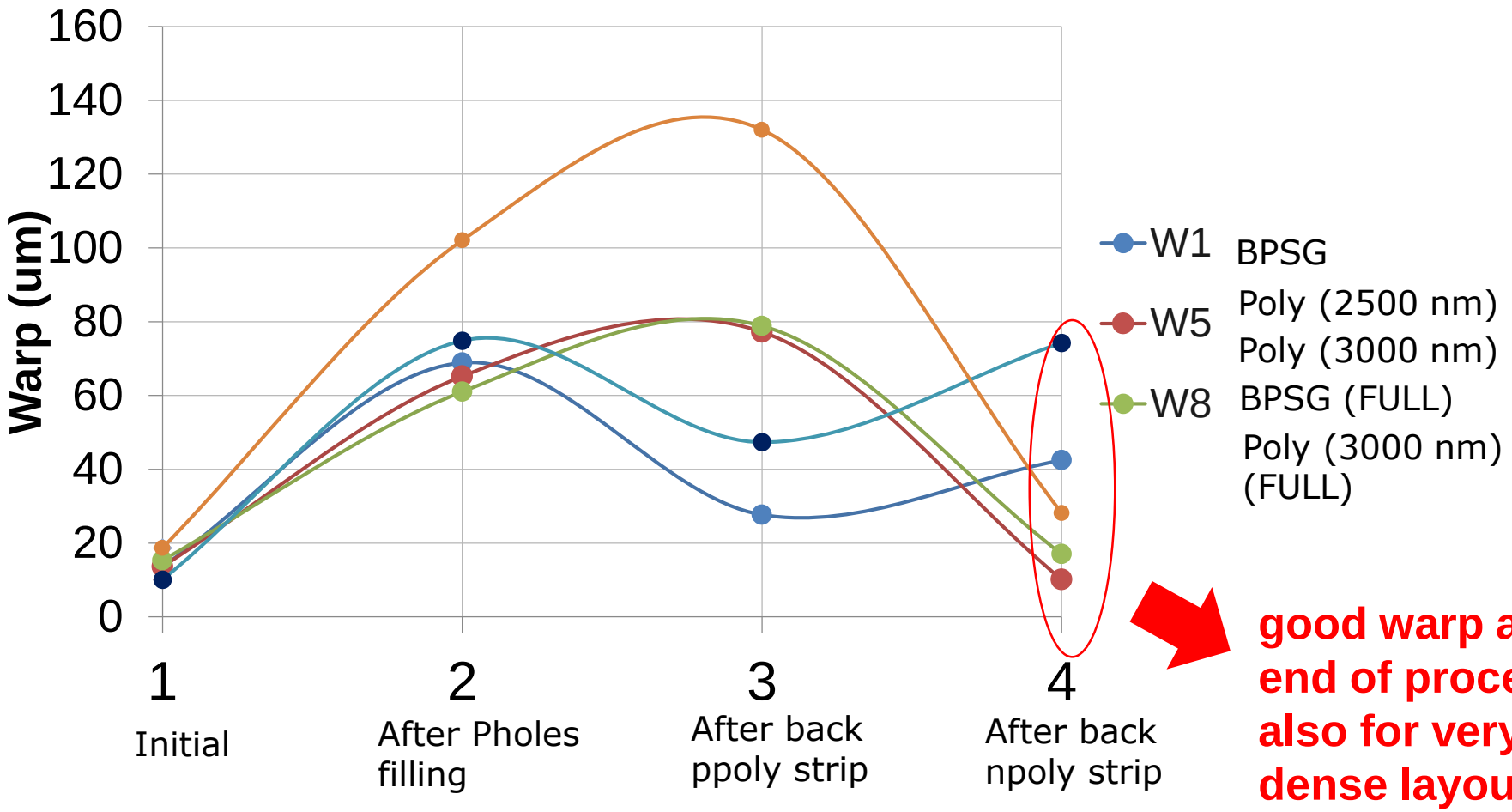
(measured with MicroProf® FRT GmbH system, on a matrix of 76x73 points)

Warp 3D_AIDA231



good warp at the end of process also for very dense layout!

Waiting for finish process…

- We expect to complete the process in two months.
  - *Now the stepper is out of service*
- We need to plan a parametric characterisation with TM (IV)
  - *Optimise time demand*
- TM removal
- Distribution of wafers/devices

Thanks

PIXEL and STRIP

Number	N pix/strip	Pitch [um]	Timepix 4 compatible	Border version	Number of Trenches
CHIP A					
1	169X168	55X55	Y	V2	1TR
CHIP B					
2	50X50	42X42		V1	1TR
3	21	100		V2	1TR
4	8	Circular		V2	2TR
5	5X5	1300X1300		V2	1TR
6	18	50		V1	1TR
7	4	Circular		V2	2TR
CHIP C					
8	32X32	55X55	Y	V1	1TR
9	32X32	55X55	Y	V2	1TR
10	32X32	55X55	Y	V3	1TR
11	32X32	55X55	Y	V4	1TR
12	32X32	55X55	Y	V1	2TR
13	32X32	55X55	Y	V2	2TR
14	32X32	55X55	Y	V3	2TR
15	32X32	55X55	Y	V4	2TR
CHIP D					
16	15	100		V1	1TR
17	15	100		V1	2TR
18	64X64	55X55		V2	1TR
19	64X64	55X55		V1	1TR
20	30X30	100X100		V2	1TR
21	64X64	42X42		V2	1TR

2X2 Test

Number	Border version	Number of Trenches	Trench Width	is PIN	
CHIP C					
1	V1	1TR	TW5		
2	V2	1TR	TW5		
3	V3	1TR	TW5		
4	V1	2TR	TW5		
5	V2	2TR	TW5		
6	V3	2TR	TW5		

TEST 2x1

Number	Border version	Number of Trenches	Trench Width	is PIN	NOND
CHIP C					
1	V2	1TR	TW1		
2	V2	1TR	TW2		
3	V2	1TR	TW3		
4	-	1TR	TW1	Y	
5	V2	1TR	TW4		
6	V2	1TR	TW6		
7	V2	1TR	TW7		
8	-	1TR	TW7	Y	
9	V2	2TR	TW1		
10	V2	2TR	TW2		
11	V2	2TR	TW3		
12	-	1TR	TW2	Y	
13	V2	2TR	TW4		
14	V2	2TR	TW6		
15	V2	2TR	TW7		
16	-	1TR	TW6	Y	
17	V1	1TR	TW5		
18	V2	1TR	TW5		
19	-	1TR	TW5	Y	
20	V3	1TR	TW5		
21	V4	1TR	TW5		
22	-	1TR	TW4		
CHIP D					
23	V1	2TR	TW5		
24	-	2TR	TW5	Y	
25	V2	2TR	TW5		
26	-	2TR	TW2	Y	
27	V3	2TR	TW5		
28	V4	2TR	TW5		
29	V2	1TR	TW5		Y
30	-	1TR	TW5	Y	Y
31	V2	2TR	TW5		Y
32	-	2TR	TW5	Y	Y

Bow and warp

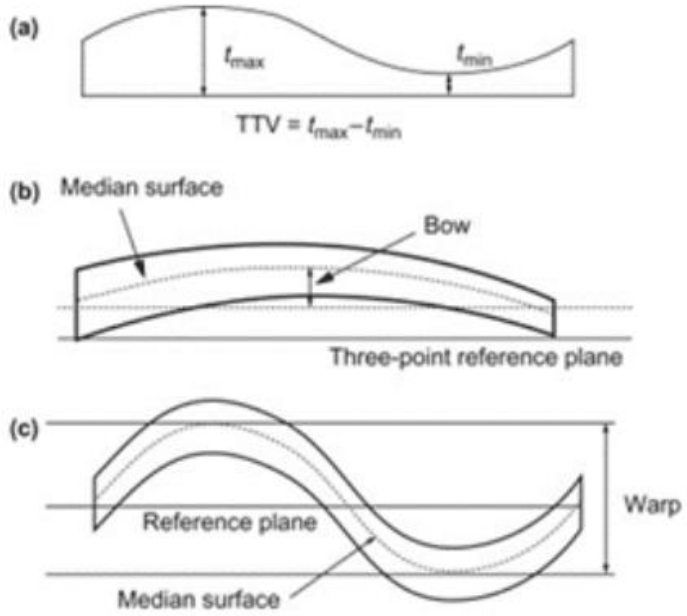


Fig 1 Representation of Wafer TTV, Bow and Warp