

Advancement and Innovation for Detectors at Accelerators

Status of DMAPS (WP5) Activities

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3rd Annual Meeting Valencia – 20 Mar 2024 https://indico.cern.ch/event/1307202/



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□ 7 projects are (partially, not exclusively) supported by the AIDAinnova framework using 4 different processes provided by 2 foundries: LFoundry (Wuxi Xichanweixin Semiconductor) and TowerJazz → Tower Semiconductor (Intel as of 2022)

□ All developments have samples, characterisation in full swing



Submission	Process	Availability	Target	Comments	Contact Institute	Task Contact
TJ-MALTA 2 /3	TowerJazz 180 nm	Beginning 2021 MPW Q1 2022	High-gran./ Rad. hard Task 5.2/5.3	LHC	CERN	Carlos Solans Sanchez
TJ-Monopix 2 /3 (OBELIX)	TowerJazz 180 nm	Spring 2021 Initiating design	High-granularity Task 5.2	Belle II	Bonn	Jochen Dingfelder
TJ 65	TowerJazz 65 nm	September 2021	High-granularity Task 5.2	Generic R&D / ALICE	IPHC	Jerome Baudot
ARCADIA	LFoundry 110 nm	Summer 2021	High-granularity Task 5.2	Demonstrator chip	INFN	Manuel Rolo
LF-Monopix 2	LFoundry 150 nm	Beginning 2021	Radiation hard Task 5.3	High granularity foreseen	Bonn/CPPM	Marlon Barbero
RD50-MPW 3 /4	LFoundry 150 nm	Spring 2022/ late 2023	High-granularity/ Radiation hard Task 5.3	R&D	Liverpool	Eva Vilella
MiniCactus 1 / 2	LFoundry 150 nm	Beginning 2021 / 2024	Radiation hard Task 5.3	Timing R&D	IRFU	Philippe Schwemling





WP5 Deliverables consist of reports, which are the responsibility of the institutes in the last column.

 Next deliverable is D5.3 in April: sufficient material from TJ-Malta and LF-Monopix projects are available, see later slides



See also: https://aidainnova.web.cern.ch/wp5



WP5 Milestones



Milestones have short associated reports and are within the responsibility of the institutes in the last column.

• Next Milestone is MS19 in April: structures from Arcadia project are available.



See also: https://aidainnova.web.cern.ch/wp5



Publications & Meetings

TJ-MALTA

- JINST 2021 <u>https://doi.org/10.5281/zenodo.6951327</u>
- TWEPP 2021 https://doi.org/10.1088/1748-0221/17/04/C04034
- IEEE TNS 2022 <u>https://doi.org/10.1109/TNS.2022.3170729</u>
- NIM A 2022 https://doi.org/10.1016/j.nima.2022.167390
- NIM A 2022 <u>https://doi.org/10.1016/j.nima.2022.167226</u>
- NIM A 2023 <u>https://doi.org/10.1016/j.nima.2022.167809</u>
- EPJ-C 2023: <u>https://doi.org/10.1140/epjc/s10052-023-11760-z</u> RD50-MPW
- JINST 2023: <u>https://doi.org/10.1088/1748-0221/18/03/C03011</u>
- JINST 2023: https://doi.org/10.1088/1748-0221/18/03/C03013
- EPJ-C 2023: <u>https://arxiv.org/abs/2308.13231</u>
- HSTD23 proceedings in preparation

TJ-Monopix

- NIM A 2022 <u>https://doi.org/10.1016/j.nima.2022.167189</u>
- arXiv 2023 <u>https://doi.org/10.48550/arXiv.2301.13638</u>
- IEEE proceedings PACET2024 submitted

LF-Monopix

- NIM A 2022 <u>https://doi.org/10.1016/j.nima.2022.167224</u>
- NIM A 2022 <u>https://doi.org/10.1016/j.nima.2022.166747</u>
- Vertex 2022 proceedings accepted, to be published
- Vertex 2023 <u>https://doi.org/10.22323/1.448.0043</u>
- HSTD23 Submitted, under revision

CACTUS

- NIM A 2022 <u>https://doi.org/10.1016/j.nima.2022.167022</u>
- NSS 2022: IEEE Trans.Nucl.Sci. 70 (2023) 11, 2471-2478
- TJ 65nm
 - NIM A 2022 <u>https://doi.org/10.1016/j.nima.2022.167213</u>
 - NIM A 2022 https://doi.org/10.1016/j.nima.2022.166826
 - NIM A 2022 https://doi.org/10.1016/j.nima.2022.167020
 - JINST 2023 <u>https://doi.org/10.1088/1748-0221/17/12/C12017</u>
 - 27 publications
 - 9 new since Sept. 2023 published or in work
 - Update of web-site and database in progress

WP5 meetings at:

https://indico.cern.ch/category/13503/



Summary of Activities

- Next slides are a brief summary of recent achievements as presented during our session yesterday
- See more details on the WP5 session agenda on indico:
 - https://indico.cern.ch/ event/1307202/





Tower 180 nm TJ-MALTA-2&3 TJ-Monopix-2 <u>Goal:</u> large (1x2 cm² (Malta2) -> 3x2 cm² (Malta3)) radhard sensor/chip w/ small electrode and high granularity, HL-LHC-layer-5 compatible with low power asynchonous readout architecture. Sensor&FE same as TJ-Monopix.

CERN and others (Bonn, CPPM, Oxford ...) - 180 nm technology -

- main objective of TJ-MALTA2:
 - make design radhard (> 1e15 neq/cm2):
 - i. shape charge collection geometry
 - ii. optimize FE against RTS noise
 - iii. use high resistive Cz-Si substrate (100 μm) rather than epi-Si (25 μm).
 - improve asynchronous readout
- <u>objective</u> **TJ-MALTA3**:
 - exploit full reticle size: 3x2 cm²
 - improve on remaining MALTA2 issues
 - add 1.28 GHz local clock
 - target: mini-MALTA MPW in Q2 2023

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TJ-MALTA High granularity, small electrode



TJ-MALTA A Hop granularity, small electrode

Goals of MALTA2 achieved:

- radhard up to 3E15 n_{eq}/cm² (at least)
- Higher doping of n-layer helps
- RTS noise mitigated



• excellent matrix homogeneity

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TJ-MALTA High granularity, small electrode

- Mini-MALTA 3
 - 5x4 mm2 demonstrator for full MALTA3
 - Same FE as MALTA2
- Chip arrived in late
 2023
- Chip is alive and systematic testing including test beams starts now





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TJ-Monopix 2 High granularity, small electrode

<u>Goal</u>: mature large (2x2 cm²) high granularity (small electrode) fully functional, HL-LHC compatible (5th layer) DMAPS sensor with column drain readout, w/ low noise and low power consumption

	TJ-Monopix1	TJ-Monopix2
Chip Size	1x2 cm ² (224x448 pix)	2x2 cm ² (512x512 pix)
Pixel size	$36\times 40~\mu m^2$	$33.04 \times 33.04 \ \mu m^2$
Total matrix power	130 mW/cm ²	170 mW/cm ²
Noise	≅11 e ⁻	< 8 e ⁻ (improved FE)
LE/TE time stamp	6-bit	7-bit
Threshold Dispersion	≅ 30 e ⁻ rm s	< 10 e ⁻ rms (improved FE + tuning)
Minim um threshold	≅ 300 - 400 e ⁻	< 200 e ⁻
In-time threshold	≅ 350 - 450 e ⁻	< 250 - 300 e ⁻
Efficiency at 10 ¹⁵ n _{eq} /cm ² , 30 μm epi	≅ 87 %	> 97 %
Efficiency at 10 ¹⁵ n _{eq} /cm ² , Cz	≅ 98.6 %	> 99 %

Clear improvements wrt TJ-M1
 before and after irradiation

Bonn, CERN, CPPM, IRFU

- 180 nm technology -
- sensor and chip working
- assembly problems (wire bonding sensibility) reduce yield, is now manageable, but still problematic
- a temporary major problem at 5 MHz BC-ID clock interfering now understood and circumvented
- characterisation finally in full swing
- baseline for Belle II VTX upgrade → Obelix chip:
 - Uses analog part from TJ Monopix 2
 - New digital periphery with several additional features

20 March 2024

1.00

0.95

0.90

Catio 0.85

0.80

0.75

of in-time hits

C. Bespin, J. Baudot, A. Kumar et al.

SuperPixel inpixel efficiency



Most recently added detailed timing performance and post irradiation measurements:

- >99% eff. after 5E10¹⁴ n_{eq} /cm² irradiated with 24 MeV p
- ~1-2 ns time resolution limited by TDC (1.5625 ns bin size, 93.7 ps time resolution from FE)
- > 99% in-time efficiency for 25 ns window and for 15 ns window for epi-Si (26 µm depl. volume)
- Delay difference of up to 3.5 ns depending on in-pixel track position







AIDA Innova High granularity, small electrode



Pitch Signal ToT	33 μm 7 bits	OBELIX-1 matrix: 896x464 pixels overall size 30.2x18.8 mm ²
Integration time	50 To 100 ns	
Time stamping	~5 ns for hit rate < 10 MHz/cm ²	matrix matrix
Hit rate max for 100% eff.	120 MHz/cm ²	analogue periphery
Trigger handling	30 KHz with 10 μs delay	
Trigger output	~10 ns resolution with low granularity	periphery
Power (with hit rate)	120 to 200 mW/cm ² (1 to 120 MHz/cm2)	
Bandwidth	1 output 320 MHz	



TPSCo 65 nm process of Tower (new window of opportunity)

Tower 65nm



TPSCo 65 nm (Tower)

<u>Goal:</u> exploring the new technology (large collaboration effort, CERN + 24 institutions) including <u>stitching,</u> small electrode designs

1+2 submissions so far: MLR1 (2020), ER1 (2022) each containing several structures and designs ER2 is expected for 2025



^{19 March 2024} J. Baudot, A. Kumar et al.



TPSCo 65 nm (Tower)

Detailed position resolution studies done CE65v1/v2 chip family form MLR1 and ER1



Very good results achieved:

- spatial resolution of ~2.7 +/- 0.3 μm for standard 25 μm pixel
- spatial resolution of ~1.3 +/- 0.3 μm for standard 15μm pixel
- to be compared with DPTS with modified process and 15 μ m pixel: 4 4.2 μ m

J. Baudot, A. Kumar et al.

19 March 2024 J. Baudot, et al

19

2nd submission: Engineer Run 1 (ER1)

- Main goal = exercise stitching (in 1D) to assess yield
- Submission November 2022
- Back from fab April 2023
- 2 long (~26 cm) sensors
 - MOSS: priority-encoder readout (ALPIDE-like)
 - 1.4 cm wide
 - 18 & 22.5 µm pitch
 - MOST: low power asynchronous readout
 - 0.25 cm wide

Many (51) chiplets

- Pixel prototypes
- SEU test chips
- Functional blocks (PLL, serial links)
- New metal staks
- New methodology for submission
 - Digital-on-top



12"





TPSCo 65 nm (Tower)



TPSCo 65 nm (Tower)



Ramp supplies slowly and monitor currents

OK -> all supplies ramped to full voltage and currents less than compliance *limit*

Wafer maps reconstructed from power ramps data of MOSS on carriers

Wafer to wafer differences

Detailed investigation of units with high current ongoing







Stitched sensor MOSS from ER1:

- Design is functional
- Sensor works 26 cm long!
- Learning about yield and waferto-wafer variations

^{20 March 2024} J. Baudot, A. Kumar et al.



LFoundry 150 nm

- LF-Monopix-2
- RD50 MPW2/3
- CACTUS



<u>Goal</u>: mature large (1x2 cm²) (very) radhard, <u>large</u> electrode fully functional, HL-LHC compatible (5th layer) DMAPS sensor with column drain readout

irradiated devices (1 and 2e15 n_{eq}/cm² @ Bonn Cyclotron)

• no significant degradation at this level except for leakage current increase





fully depleted @ ~200 V bias (15 V unirr.)

Lars Schall, C. Bespin, et al.



<u>Goal</u>: mature large (1x2 cm²) (very) radhard, <u>large</u> electrode fully functional, HL-LHC compatible (5th layer) DMAPS sensor with column drain readout

- intensive test beam characterisations
- very high (>99%) efficiency (in-time) after 1 and 2e15 n_{eq}/cm²
- ~no efficiency degradation wrt unirradiated devices
- New: devices irradiated to 2e15 n_{eq} tested:
 - still >99% efficiency but more pixel disabled due to leakage current induced ENC increase, higher gain of pre-amp helps for in-time eff.







RD50-MPW2/3

<u>Goal:</u> series of MPWs (1 ... 4) to achieve very small pixels (60 x 60 μm²) radhard @ HL-LHC level 5th layer by large electrode design (all electronics inside deep well)

MPW2: small prototype

- pixels: 60 x 60 μm2
- in-pix CSA + discriminator, analog R/O
- testbeams performed
- charge collection ok

MPW3: added digital R/O (column drain)

- V_{breakdown} ~ 150V
- very high noise (> 2000 e) due to noise coupling from digital periphery
- Poor test beam efficiency due to high thresholds

MPW4 (2023/24): backside processing to improve radiation hardness, eliminate high noise and increase breakdown







RD50-MPW2/3

MPW4 (2023/24):

- Initial tests indicate that noise elimination and breakdown voltage increase was achieved
- Tests with backside processed wafers proved improved leakage current behaviour





20 March 2024

 ENC of 200e⁻ over whole matrix and small threshold dispersion

Goal: Develop CMOS pixels for timing applications (~50 ps)

Mini CACTUS = small prototype to address limitations of CACTUS (low S/N)

- 65 ps mip time resolution achieved in test beams
- compared calibrations and resolutions using photons of different energies (²⁴¹Am and @SOLEIL)
 - \succ calibrations \checkmark
 - \succ $\sigma_{\rm t}$ for photons (understandably) worse (320 ps)
- characterisation after 1e14:
 - Time resolution worsens at room temperature but with low leakage current at -15°C recovers

Sensor	HV bias (V)	Conditions	Temp. (°C)	Time res. (ps)	MPV (mV)
Unirradiated 300 u	400	testbeam, MCPMT time reference	room	78.97 ± 1.36	201.9 ± 0.5
Unirradiated 300 u	400	90Sr, PMT time reference*	room	104.5 ± 2.30	195.7 ± 2.3
Unirradiated 300 u	280	testbeam, MCPMT time reference	room	89.11 ± 1.56	200.9 ± 0.5
Irradiated 300 u	280	90 Sr, PMT time reference	20	108.2 ± 3.2 (PMT subt.)	108.2 ± 3.2
Irradiated 300 u	320	90 Sr, PMT time reference	20	132.9 ± 5.0 (PMT subt.)	113.5 ± 0.8
Irradiated 300 u	320	90 Sr, PMT time reference	-15	87.9 ± 4.7 (PMT subt.)	132.7 ± 0.6





CACTUS large electrode



MiniCACTUS V2

CACTUS large electrode

- ~ 2 times larger than MiniCACTUS
- 0.5 mm x 1 mm (baseline), 1 mm x 1 mm and 0.5 mm x 0.5 mm diodes
- 50 µm x 150 µm and 2 50 µm x 50 µm small test diodes
- 3 different preamps
- New multistage discriminator with programmable hysteresis ≈ 5 mm
- Improved layout for better mixedsignal coupling rejection
- CEA-IRFU & IFAE-Barcelona coll.
- Submitted in May 2023, waiting for samples to
- come back from post-processing





LFoundry 110 nm



ARCADIA Tests

<u>Goal:</u> Develop DMAPS technology platform in 110 nm technology. Largely funded by INFN. Targeting small pixels, very low power, various thicknesses

- MD3 main-demonstrator with system-grade full chip Fully Depleted MAPS (FDMAPS with 512x512 pixel matrix, pitch 25 μ m, low power, high event rate)
- Scalable FDMAPS architecture with very low power of 10 mW/cm²
- adding gain layer for LC3 (MADPIX), small prototype (4 x 16 mm²)
- Structures from both are available and first results looks reasonable





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ARCADIA Tests Main Demonstrator

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Main Demonstrator - acquisition setup

Total power consumption: 10 mW/cm² at low event rates
 Design specification: 20 mW/cm² at rates up to 100 Mevents/cm²

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20 March 2024



ARCADIA Tests



Noise and slew-rate characterization First data with **beta source** (⁹⁰Sr) with external test-pulse injection 250 SNR ≈ 20 Noise map 600 200 550 [\n] 500 superior Signal S 150 100 50 350 0.01 0.02 0.00 0.03 0.04 0.05 0.06 0.07 0.08 V [V] 0.012 Slew rate (20% - 80%) kV/s 0.010 1000 0.008 ≥ 0.006 900 0.004 800 0.002 700 0.000 Data Simulation 600 0 **U. Follo** 16-8 Time [s]

- But gain layer turned out to be too low (~3 instead of 10 30) due to mismatch in p-gain implant energy
- Will be fixed now with new short loop engineering run
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LFoundrxy 110 nm, TSI PSI developments



A. Ebrahimi et al.



Goal: Generic R&D on DM ´ provided by ARCADI^

- Encouraging
- TSI devc'











ents



Summary

- Lots of activity at all fronts: high granularity, radiation hardness and timing
- Fabrication of devices completed in all lines
- All research lines are currently intensively characterizing their devices
- ^D 2 Milestones (MS18, MS20) and 1 Deliverable (D5.1) achieved
- Next Milestone MS19 & Deliverable D5.3 due in April but sufficient material is already available
- Many publications

BACK UP SLIDES



Contact Persons and email list

One contact person per institution:

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- Let us know of changes above.
- The <u>AIDAinnova-WP5@cern.ch</u> mailing list is used for general announcements and information.