WP5: Activities on TPSCo 65 nm process

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3rd AIDAinnova Meeting
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Catania, Italy

Outline

- Introduction
- Revisiting 1st TPSCo 65 nm submission
  - CE-65 sensor design and tests
- ER1 submission
  - MOSS design and test
  - CE65v2 design and test
- Summary and outlook

People involved in CE65 sensors

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Prague: P. Stanek, L. Tomasez, A. Kostina
Hiroshima: Y. Yamaguchi, T. Katsuno
Tokyo: H. Baba, T. Gunji
Tsukuba: T. Chujo, J. Park, D.Shibata, S.Sakai

+

Larger community contributed globaly on TPSCo 65 nm development (backup **slide 20**)

WP5 Requirements

-- Goal of WP5 is to develop high granular and radiation hard depleted monolithic active pixel sensors

Sensor spatial resolution	$\sigma_{sp} \lesssim 3$ µm → for Higgs-factories ~ 5 µm → for ALICE ~ 5-10 µm → for Belle II	⇐ critical benefit of small feature size in 65nm for task 5.2
Hit rate and time resolution (depends on experiment)	-- few 10 MHz/cm^2/s for Higss-factories -- 100 MHz/cm^2/s for Belle II -- Time resolution ~ns for CLIC -- time resolution in 10-100ps range (Specific for PID or 4D tracking)	⇐ requires new readout architectures, critical for both tasks 5.2+5.3 ⇐ benefit of thin sensitive layer in 65nm, critical for task 5.3
Radiation tolerence and NIEL fluence	-- Up to 10^{12} $n_{eq(1MeV)}$/cm^2 for task 5.2 -- Mimimum 10^{15} $n_{eq(1MeV)}$/cm^2 and beyond for task 5.3	⇐ 65nm tolerance to be checked, critical for task 5.3

Roadmap

- 1st submission: MLR1 Pre-AIDAinnova
  - Test structures + Functional blocs
  - Various pixel structures

- 2nd submission: ER1 2021-2022
  - Test structures + Functional blocs
  - Various pixel structures
  - 1st stitched sensor

Activities in synergy with
CERN EP R&D WP1.2 & ALICE-ITS3

Design work

2023

- Preparation for ER2
  - ALICE-ITS3 stitched sensors
  - Still some chiplets

2024

- **3rd submission Q4: ER2**
- Preparing **4th submission: MPR2**
  - Large prototype addressing future vertex detectors & trackers
  - New ideas (amplification, …)

2025

- Preparation for **MPR2** (Q4 2024)
  - Seeds to ECFA-DRD3/7 projects

Testing work

- Finalise tests on MLR1
- Start ER1 tests
  - 1st test on stitched sensors
  - Tests on chiplets
- **Finalise tests on ER1**
- Preparartion of **ER2** tests
- Tests of **ER2** may not start before end-of-AIDAinnova

Question addressed

⇨ Techno validation

- Yield with stitching
- Handling/bending of thin & large (<100cm²) area
- Performance optimisation (space & time resolution)

⇨ Techno exploration

- **OUTCOME of AIDAinnova**
  - Readiness for ALICE-ITS3
  - Readiness for future plans

Slide: Jerome Baudot

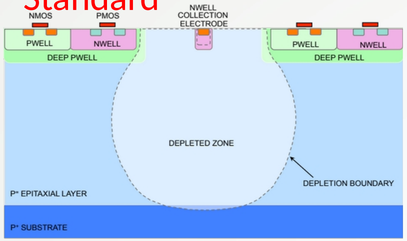
MLR1: Recap on 1st TPSCo submission

standard + 2 modified for better depletion

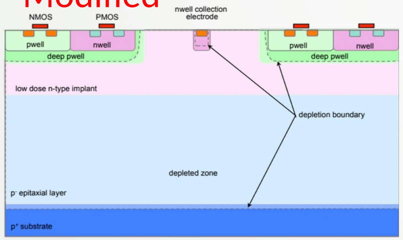
-- **“modified”**: low dose n-type blanket

-- **“modified with gap”**: same as above + gap on pixel edge.

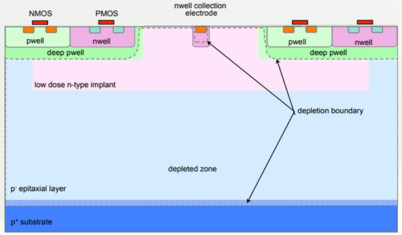
Standard



Modified



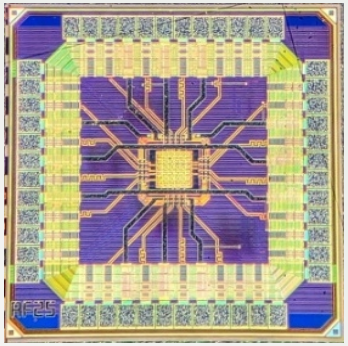
Modified with gap



APTS (Analogue Pixel Test Structure)

- 6×6 pixel matrix
- Direct analogue readout
- 4 pitches: 10, 15, 20, 25 µm
- 3 process variations

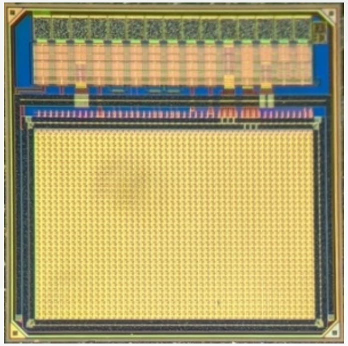
Ref: APTS



CE65 (Circuit Exploratoire 65 nm)

- 2 matrix sizes (64x32 & 48x32)
- Rolling shutter readout
- 2 pitches: 15, 25 µm

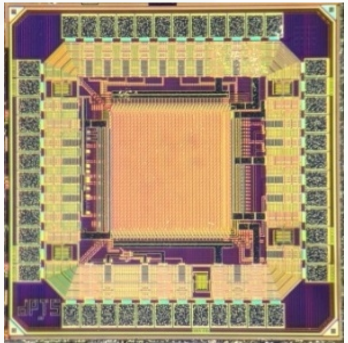
Ref: CE65



DPTS (Digital Pixel Test Structure)

- 32×32 pixel matrix
- Asynchronous digital readout
- Time-over-Threshold information
- pitche: 15µm
-Only “modified with gap” process modification

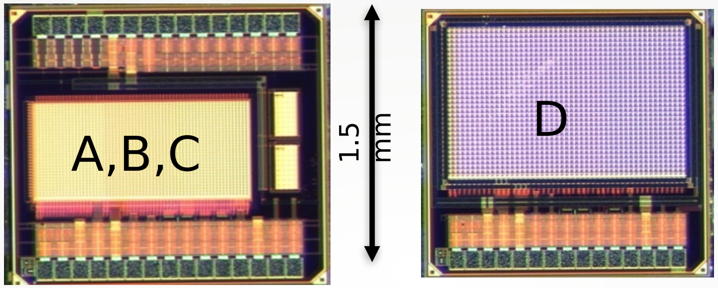
Ref: DPTS

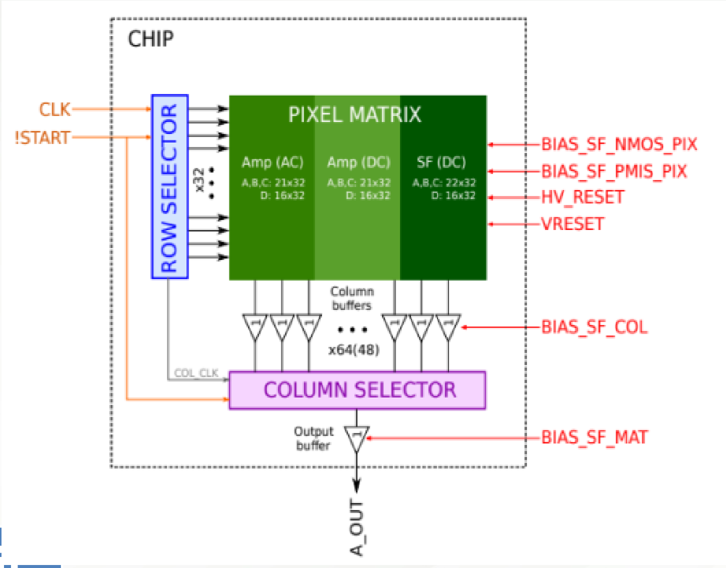


CE-65 Sensors (v1)

Contribution from IPHC

- Analogue output
- Rolling shutter readout
- Readout 10 to 40 MHz





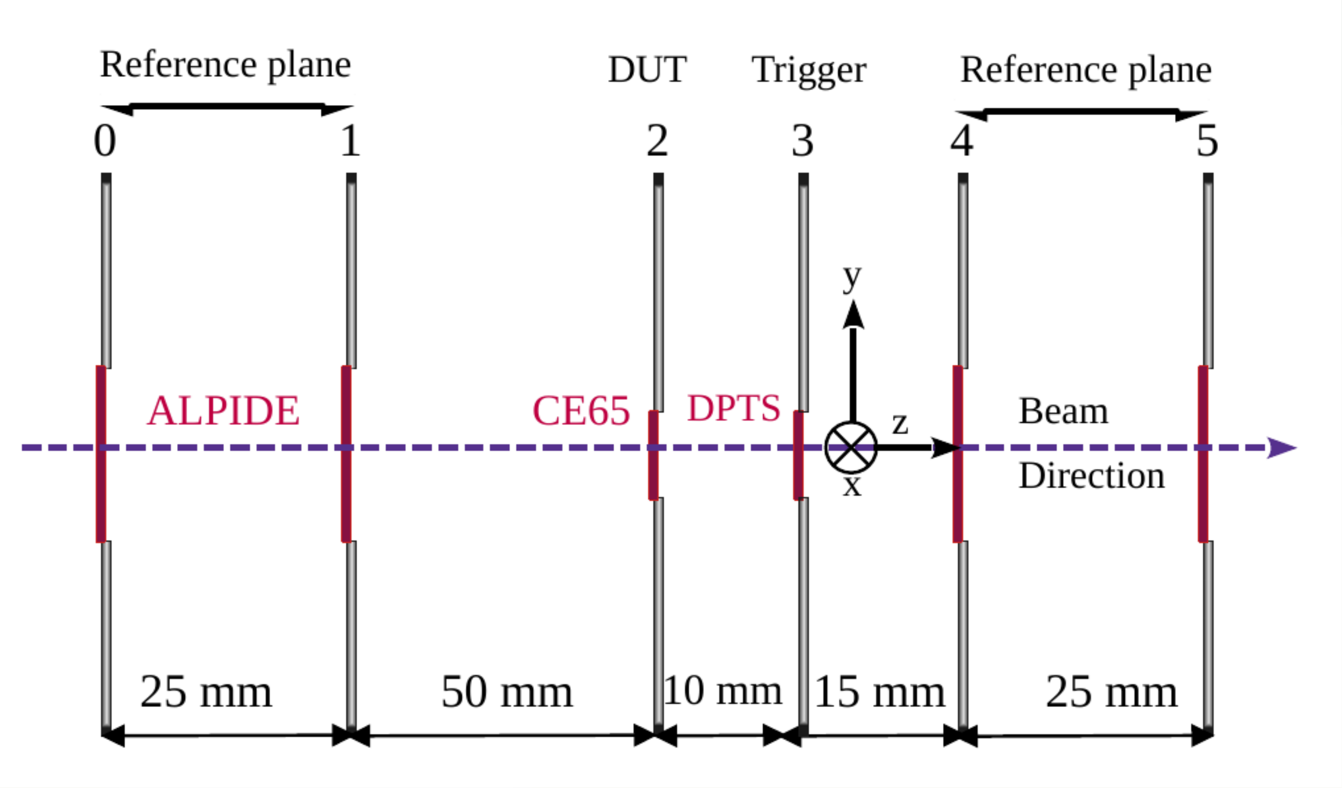
Variant	Pitch	Matrix size	Front-ends	Collection diode structure	Split
A	15 µm	64x32	DC-SF, DC-Amp, AC-Amp	Standard	1-4
B				Blanket w gaps	
C				Blanket	
D	25 µm	48x32		Basic	

<u>Note:</u> AC-coupled front-end allows sensitive volume biasing without backside voltage

Results from CE65v1 testbeam

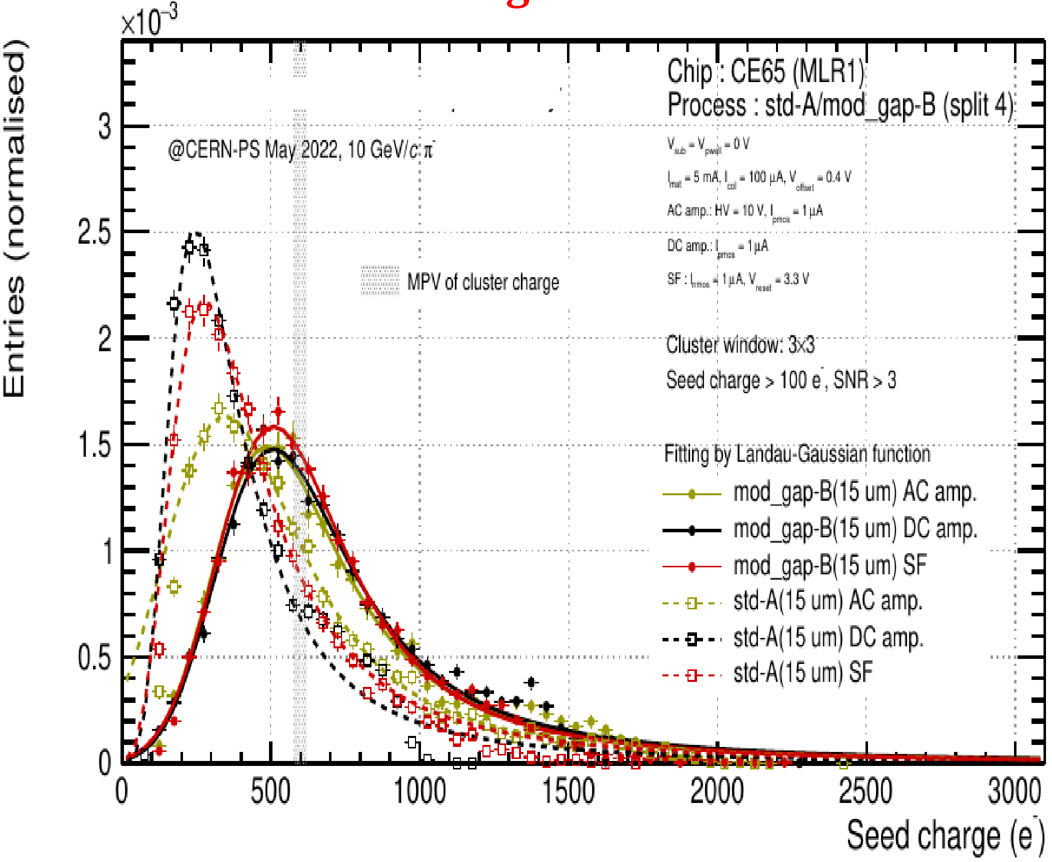
Telescope and DAQ:
Reference Arms: 4 ALPIDE planes for track reconstruction
DUT: CE65
TRG: DPTS

Test beam:
-- EUDAQ2
-- Analysis using corryvreckan
-- May 2022 at CERN-PS
-- 4 frames for each event
-- Pedestal map Noise map
-- Calibration file

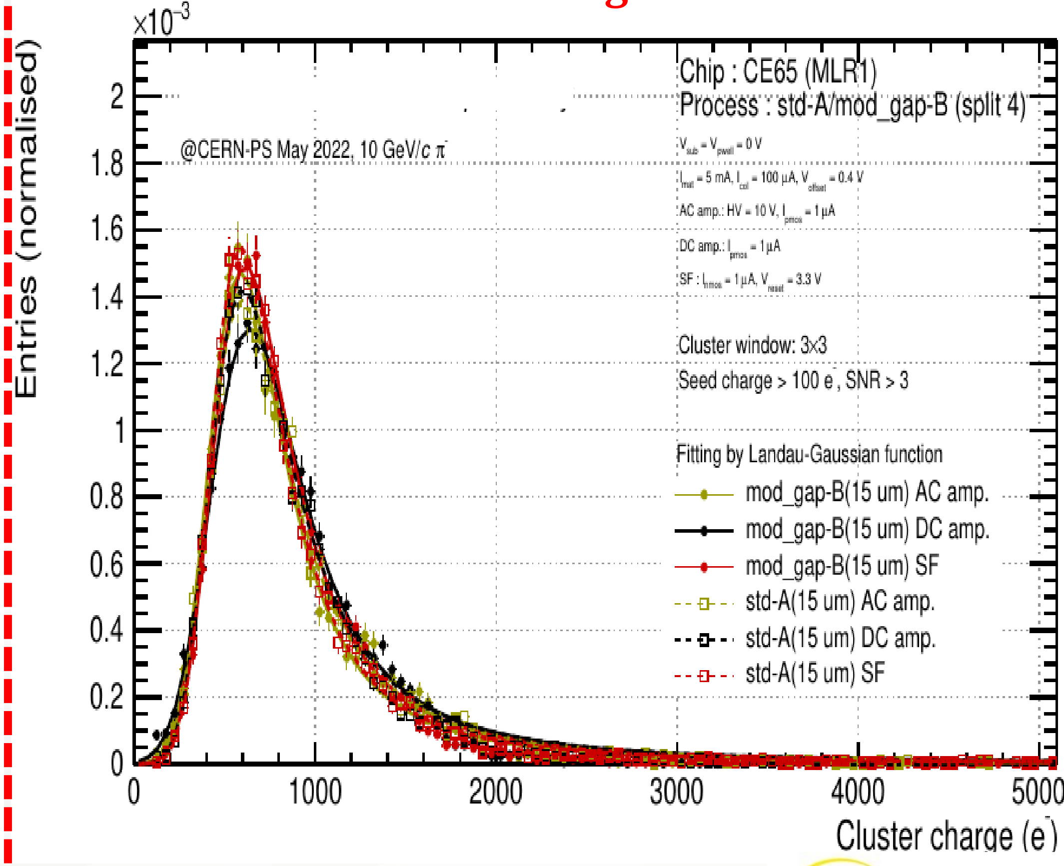


Comparing charge sharing (‘std’ and ‘mod_gap’)

Seed Charge Distribution



Cluster Charge Distribution

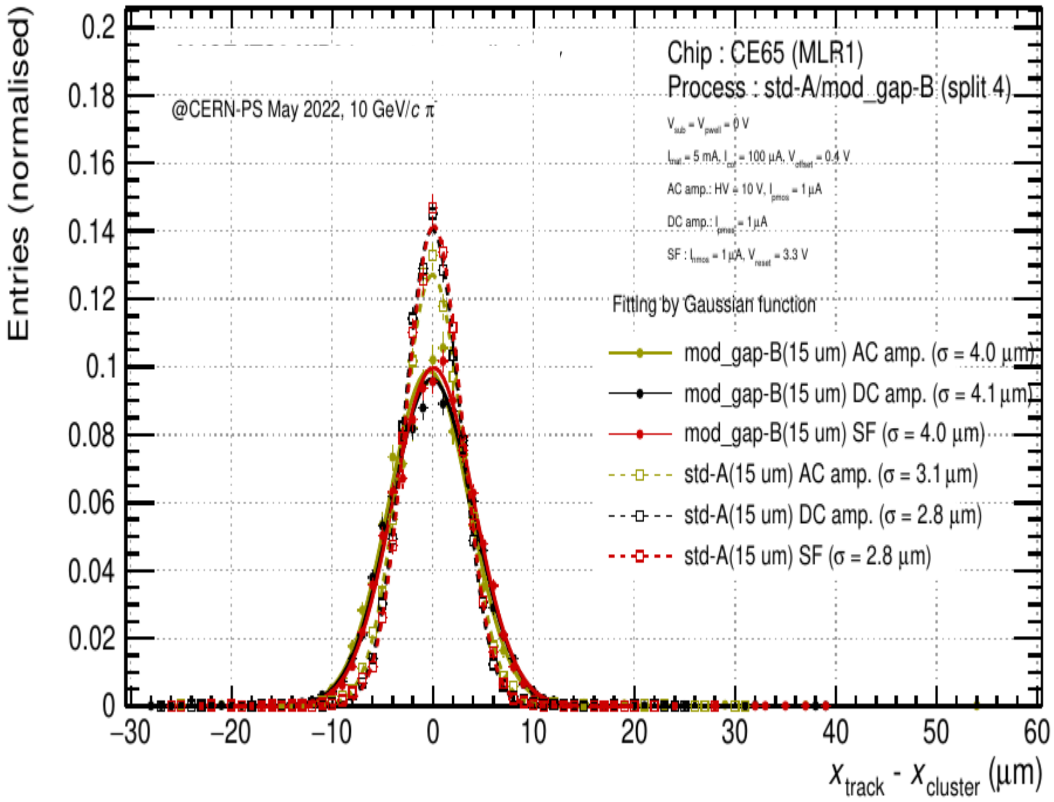


-- Charge sharing is large in “**std**” compare to “**mod_gap**”.

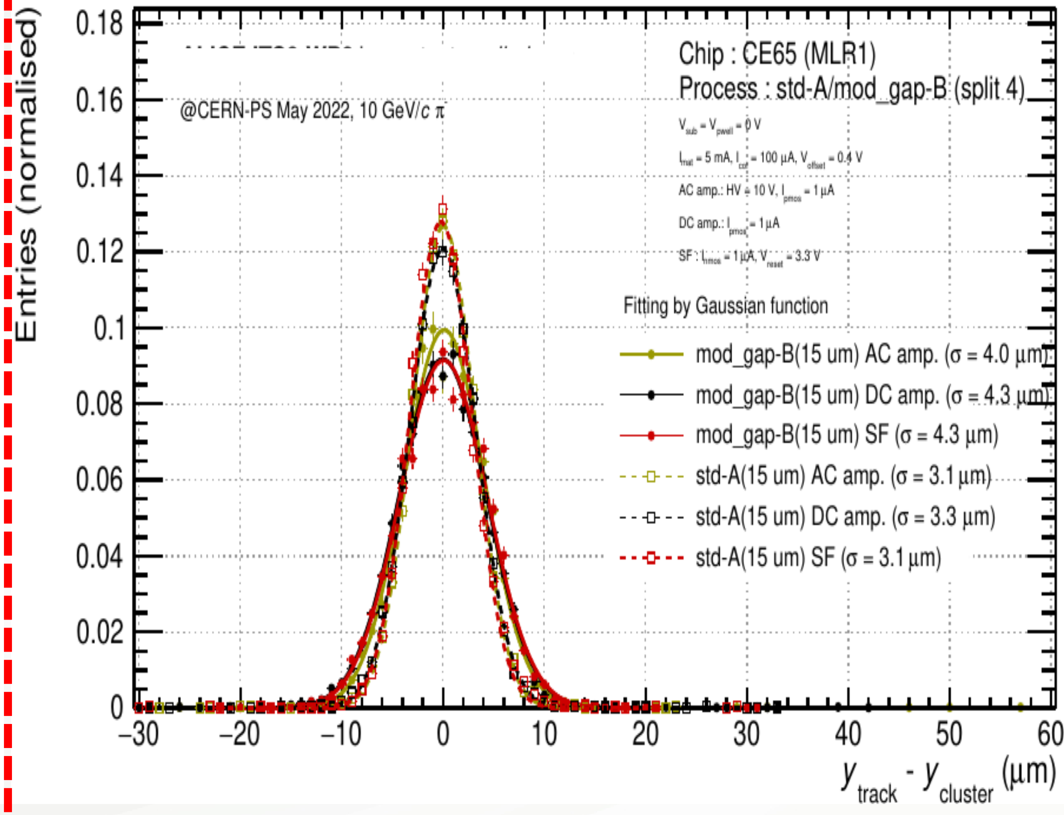
EURO-LABS EUROPEAN LABORATORIES FOR ACCELERATOR BASED SCIENCES

Comparing residuals ('std' and 'mod_gap')

X residuals



Y residuals



-- Spatial resolution **~3.0+/-0.3 (mod_gap)**, **~1.3+/-0.3 um (std)**

-- **modified** process makes us loose about 1.7 um for the same pitch of 15 um.

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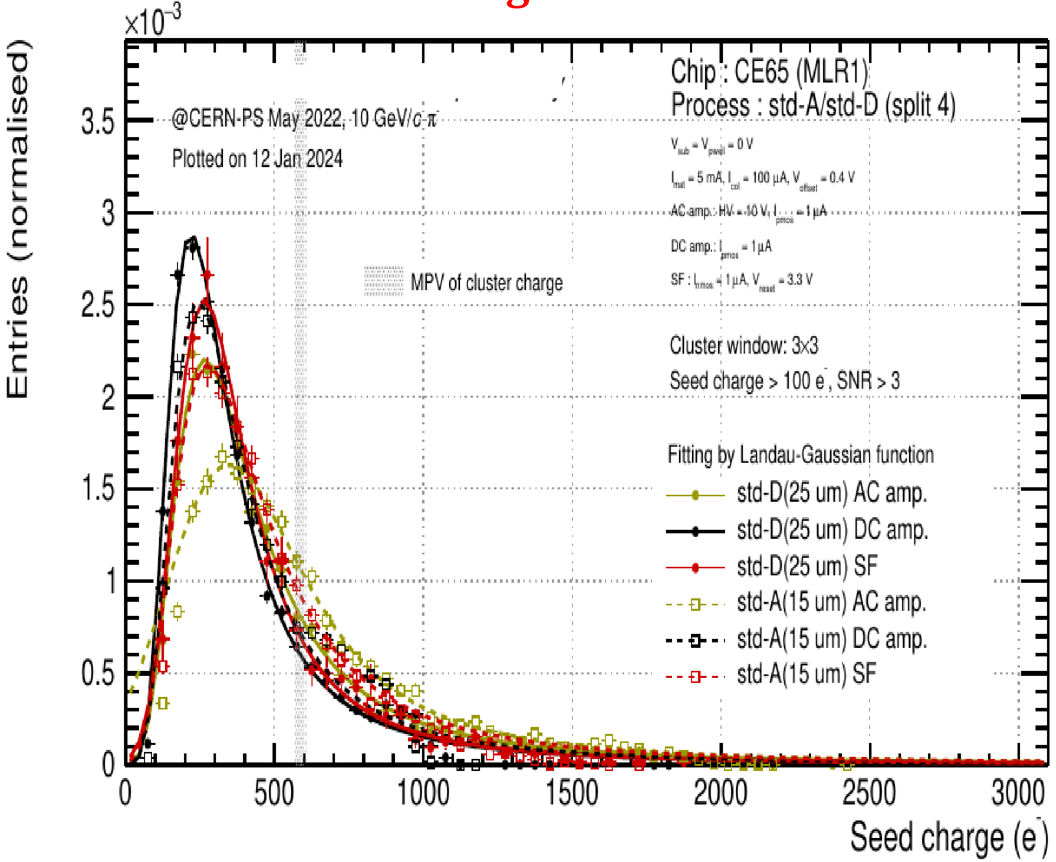
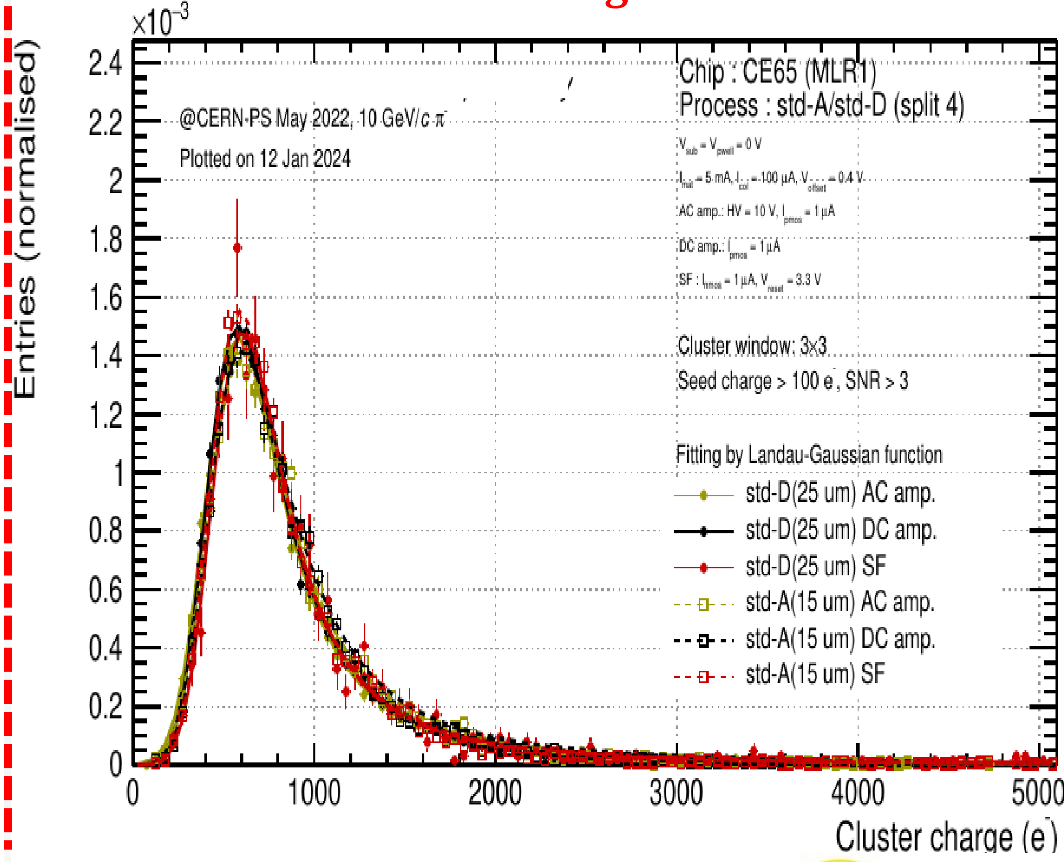
Comparing charge sharing (15um and 25um for ‘std’)

Seed Charge Distribution



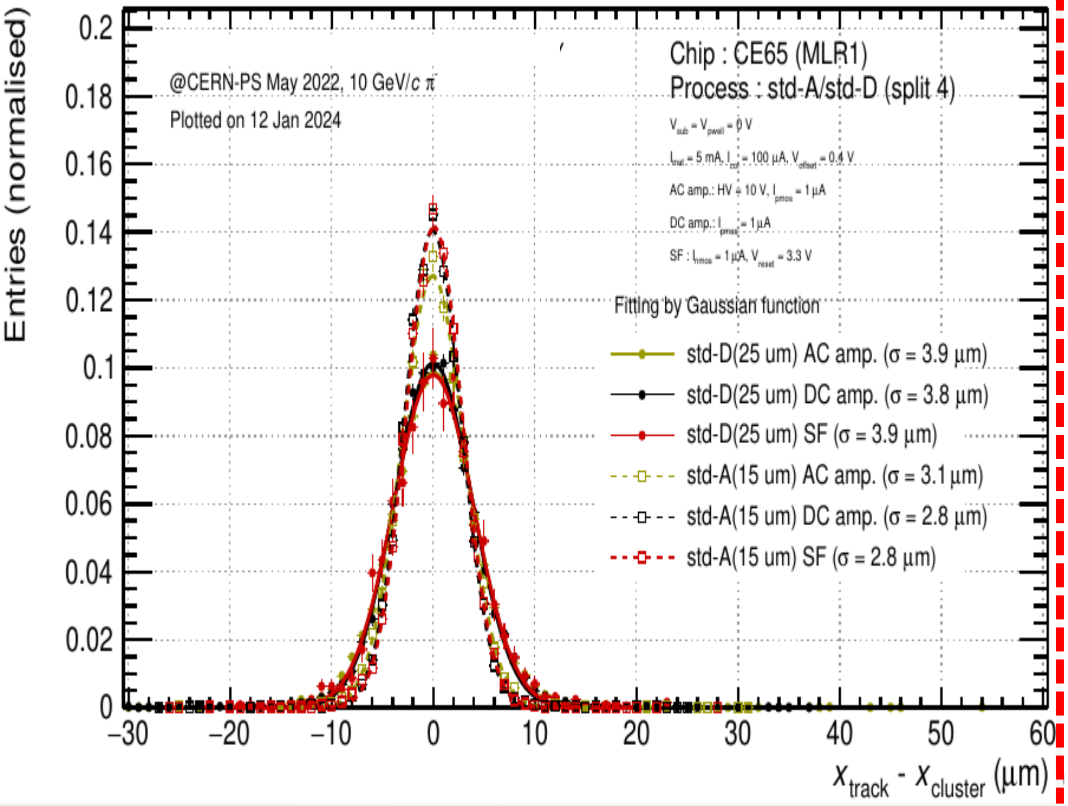
Cluster Charge Distribution



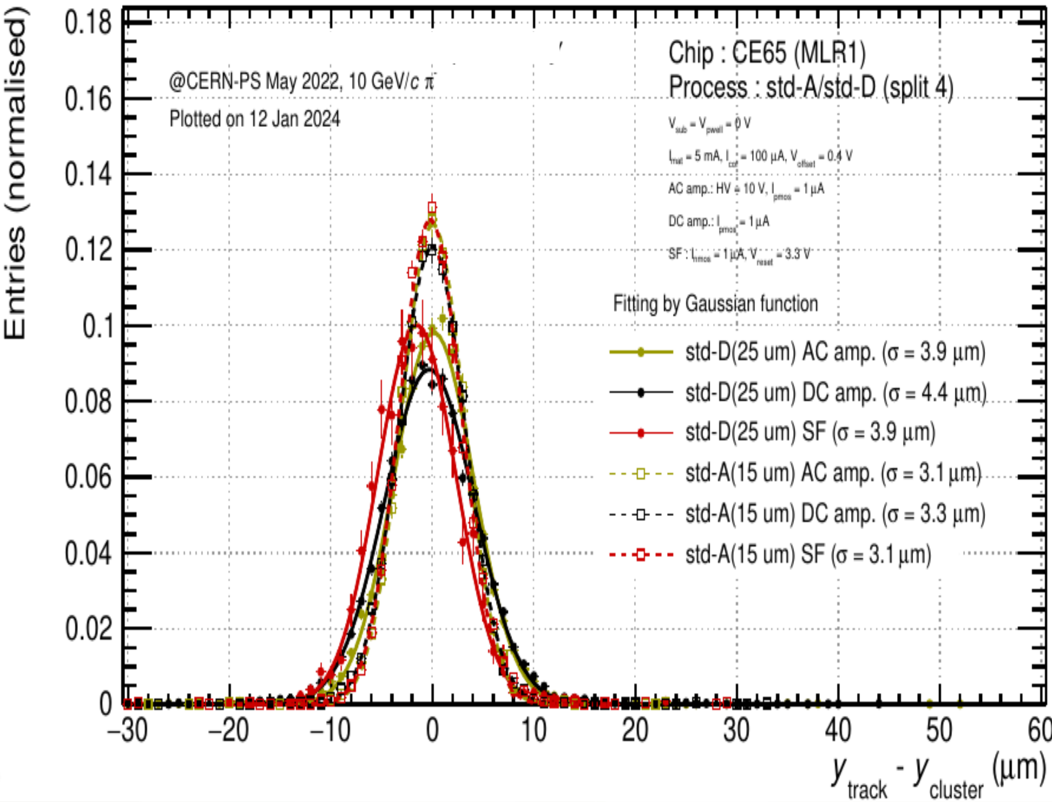
-- Charge sharing is increasing with the pitch in the “**std**” process (contrary to “**modified**” process) ---- diffusion dominate depletion!

Comparing residuals (15um and 25um for ‘std’)

X residuals



Y residuals



-- Spatial resolution **~2.7+/-0.3um (std-25um)**, **~1.3+/-0.3 um (std-15um)**.

-- We loose about 1.4 um from 15 to 25 um

-- **DPTS** with **modified** process and **15 um pitch:** about 4 to 4.2 um

ER1 submission

-- Learn and prove **stitching**

-Methodology, Constraints, Yield

-- “**MOSS**”: 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18 µm2)

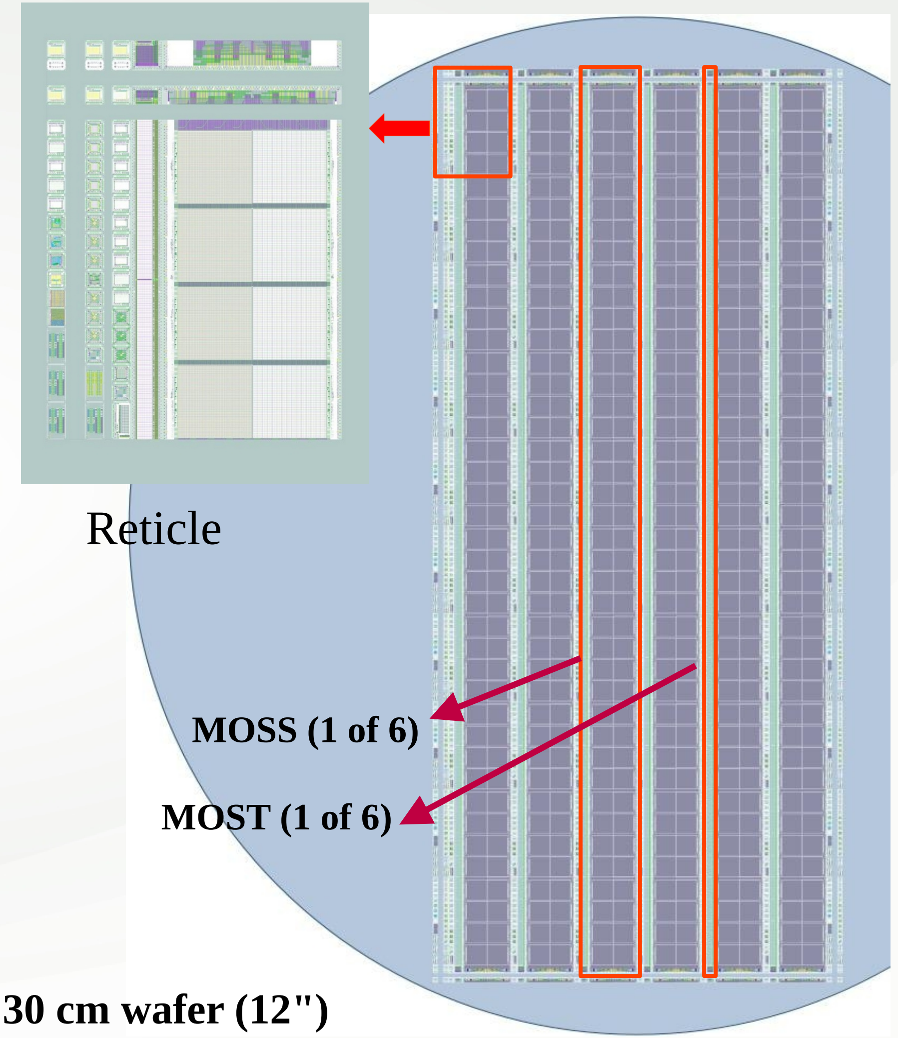
- conservative design, different pitches

“**MOST**”: 2.5 x 259 mm, , 0.9 Mpixel (18 x 18 µm2)

- more dense design, higher power granularity

-- Small prototype and test chips (like MLR1)

- Pixel Prototypes (**New versions of APTS, DPTS, CE65(v2)**)
- Fast Serial Links, PLL, I/Os, SEU



Slide: EP RD WP1.2 meeting | 20230515

CE-65 Sensors (v2)

- AC-coupled only
- three types (STD, GAP, BLANKET)
- pitches (15um, 18um, 22.5um)
- geometry (regular and staggered)
- option for window readout

- Tested at **DESY** in **Nov. 2023**

- planned to test at **SPS** in **Apr. 2024** (mainly to study apatial resolution)

- planned to test at **DESY** in **May 2024** (Irradiation study)

Pitch / process

				3 GeV	4 GeV	5 GeV
22.5	GAP	SQ	PCB08	10V & 4V (50k ev)		10V (90k events)
18	GAP	SQ	PCB02	10V (17k ev)	10,4 & 0V (55k Ev) & 2V (~30k)	
15	GAP	SQ	PCB19		10,4,2 & 0V (75k Ev)	
22.5	GAP	HSQ	PCB05		10,4,2 & 0V (50k Ev)	
18	GAP	HSQ	PCB03		10,4,2 & 0V (85k Ev)	
22.5	STD	SQ	PCB18		10,4,2 & 0V (50k Ev)	
15	STD	SQ	PCB06		10,4,2 & 0V (85k Ev)	
18	STD	SQ	PCB23		15, 10, 4 & 0V (55k Ev)	
22.5	GAP	SQ	PCB07		10V (100k Ev) 4,2 & 0V (50k Ev) + 3 frames mode (50k Ev)	

Test done at DESY, Nov. 2023

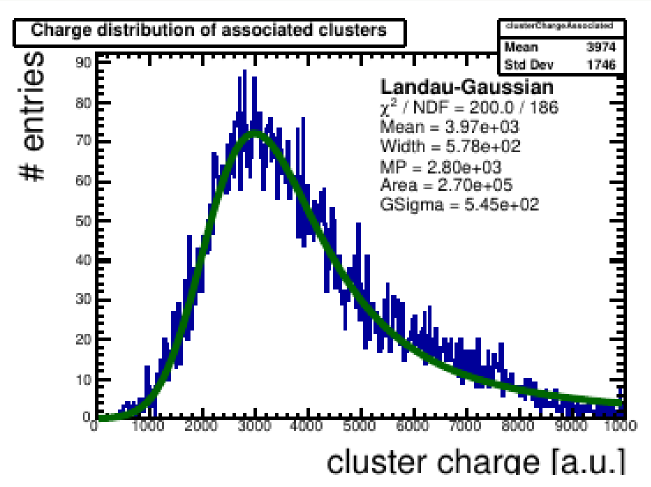
CE65v2 test beam

-- Tested at DESY in November 2023
-- ALPIDE telescope
-- Beam e^{-}4GeV

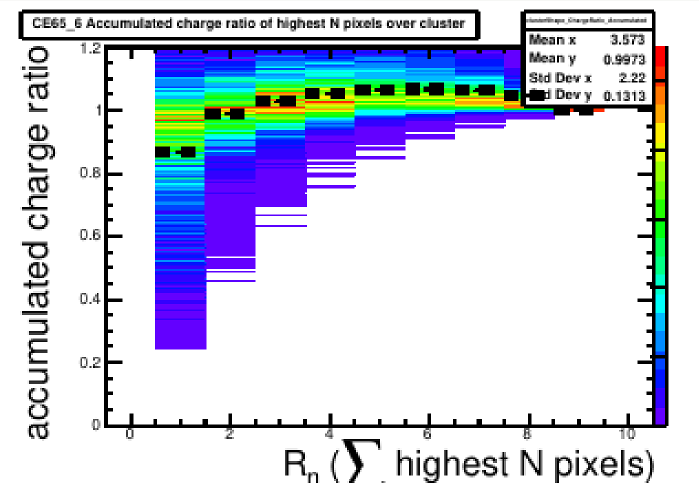
-- Analysis with Corry
  - cluster (3x3)

-- Modified with gap
-- Square pixels
-- Pitch → 22.5 um

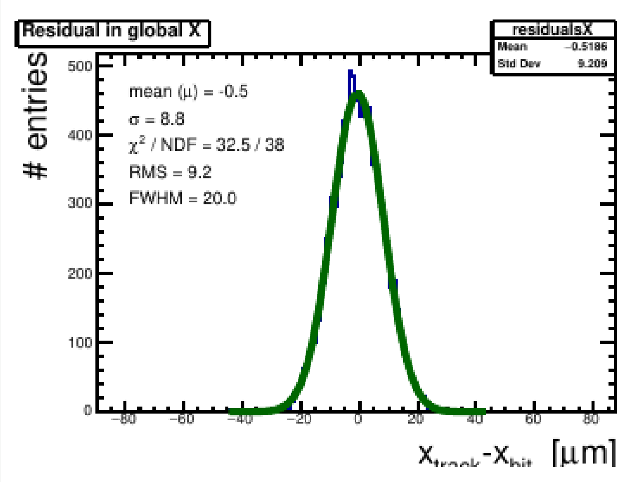
Cluster Distribution

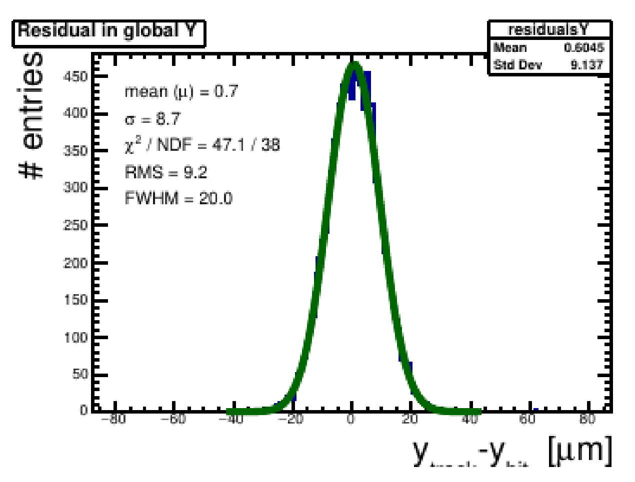


Charge sharing



Very small charge sharing

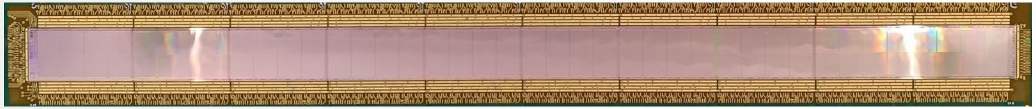


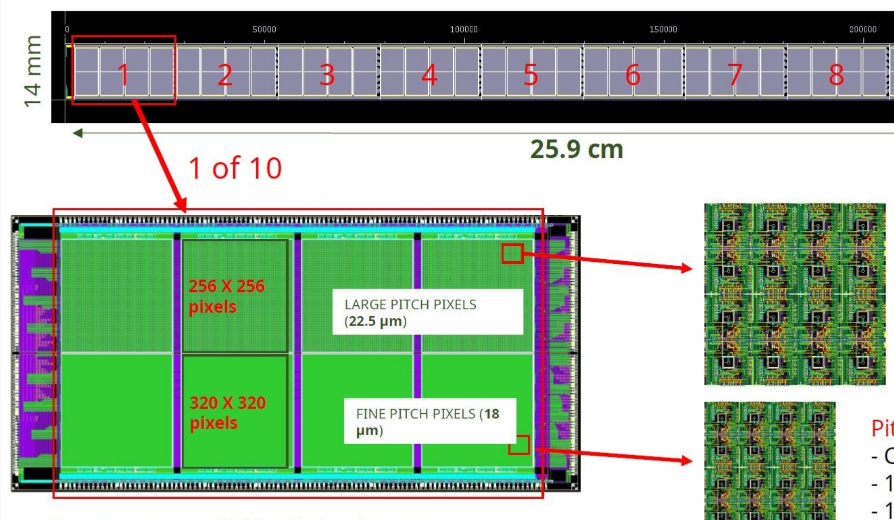


-- σ of residuals is large
-- investigation is ongoing
-- detailed analysis for all the runs is underway

MOSS design

-- 10 repeated sensor units (RSU)
-- top and bottom halves with different pitch (18 and 22.5 um)
-- 4 different sub-matrices. 6 different analogue designs, 3 of the bottom regions have the same FE
-- Each half RSU can be tested independently
-- Stitched “back-bone” allows to control and readout the sensor from left short side

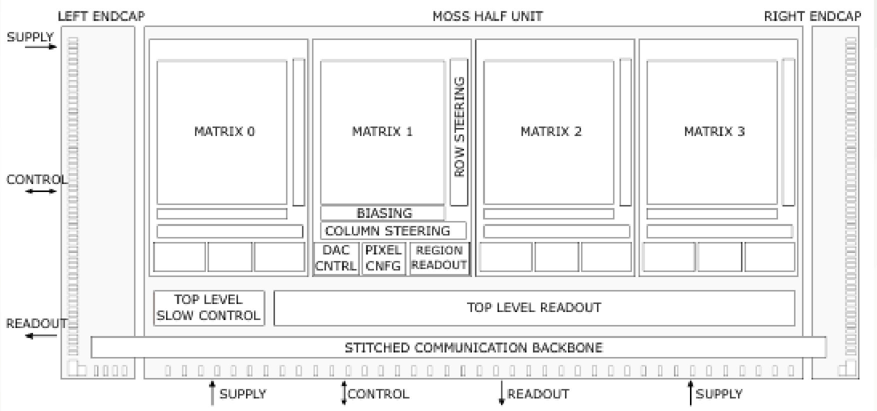


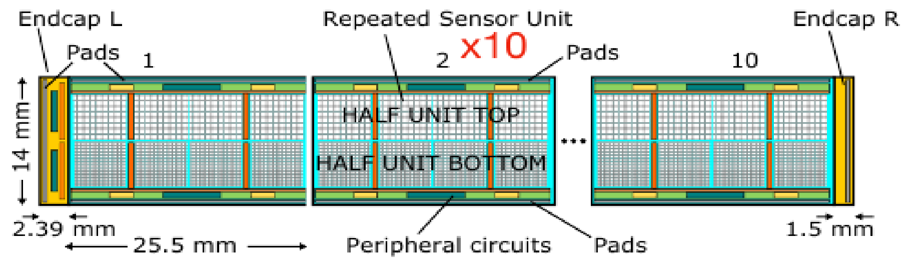


Pitch 22.5 µm
- Conservative layout
- 7 mW/cm2 (analog FE)
- 1us peaking time

Pitch 18 µm
- Compact layout
- 11 mW/cm2 (analog FE)
- 1us peaking time

- 1.4 x 26 cm monolithic stitched sensor



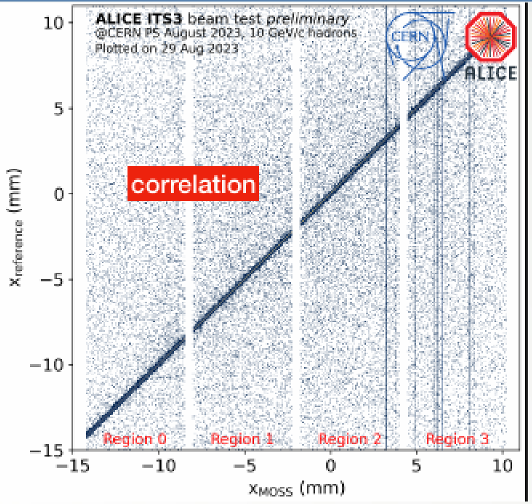


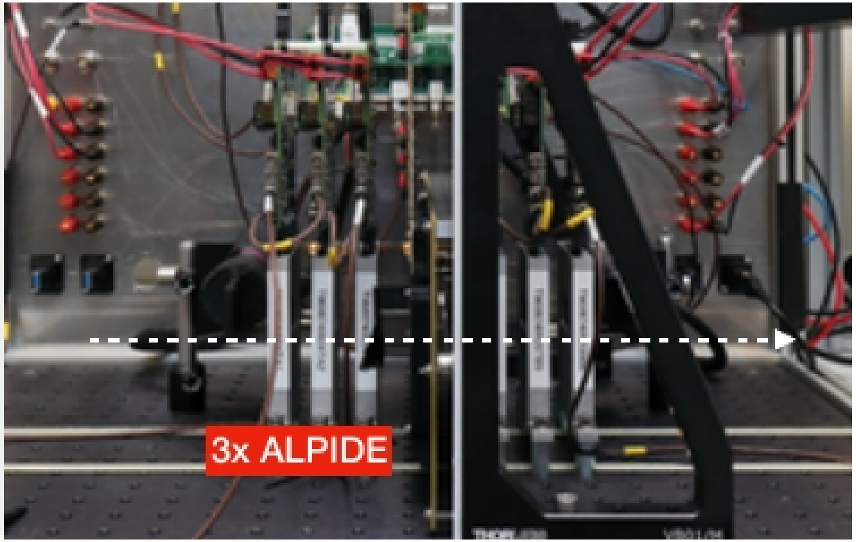
MOSS test beams

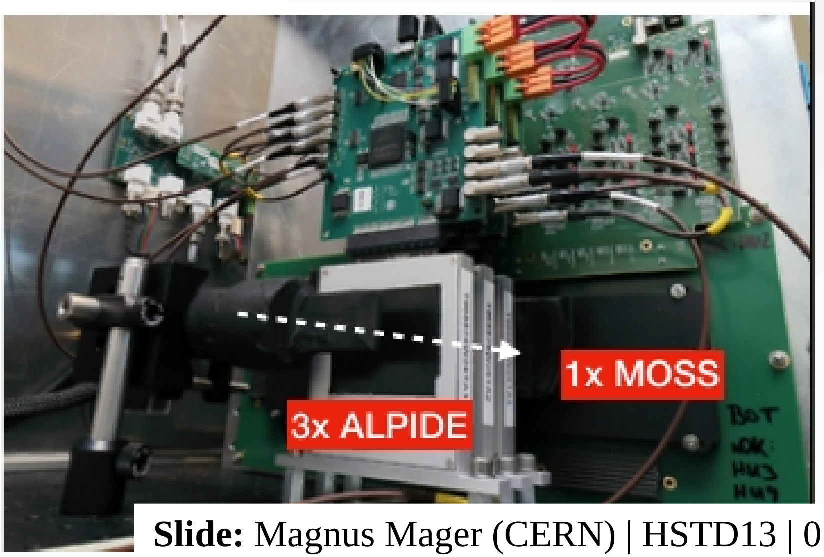
-- Several test beams in 2023

-- Parameters still to be optimised and detailed data analysis is ongoing

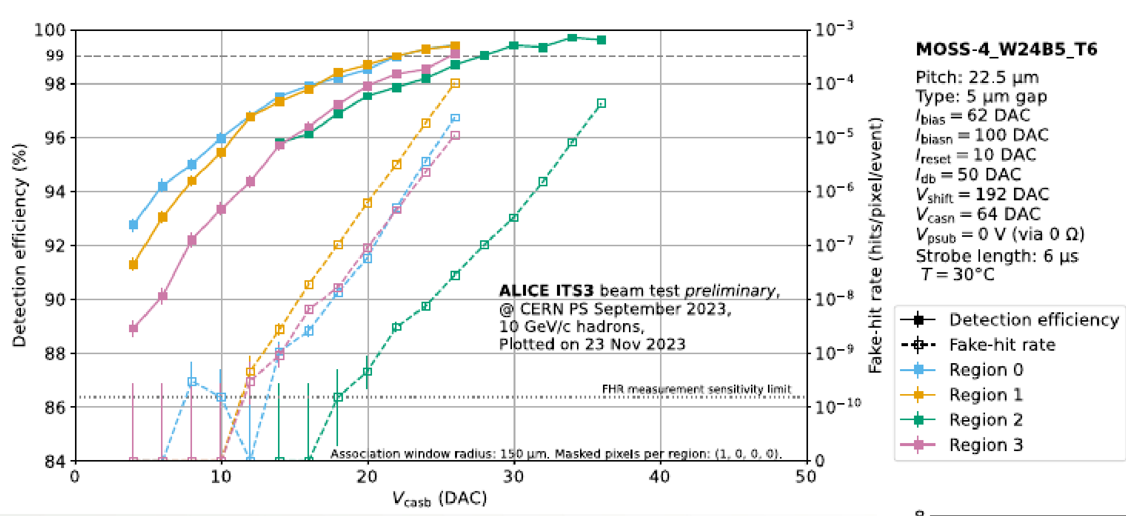
-- Very encouraging results







MOSS test beams...

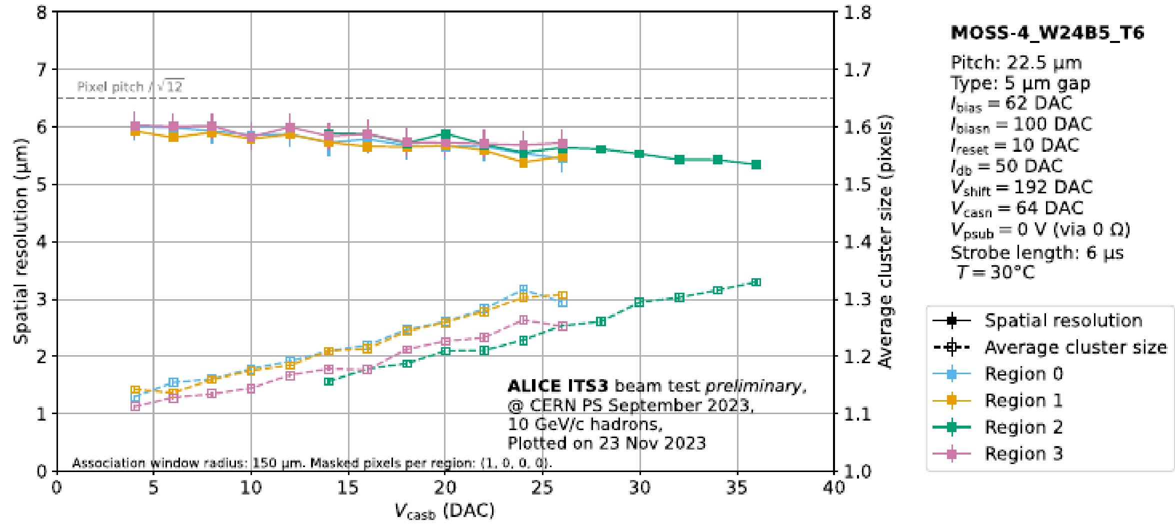


Efficiencies and fake hit rate

NB: analogue bias settings are still being optimised

Spatial resolution and cluster size

-- matches with those of small prototypes



Summary and outlook

- TPSCo 65 nm is validated for detection and stitching seems doable.
  - Full characterization of MOS-S and MOS-T needed to assess more precisely (yield) stitching

- CE-65 sensor family focuses on charge sharing & position resolution studies
  - Position resolution behaviour with pitch & process modification qualitatively understood with charge sharing
    - TCAD & Allpix2 on-going for quantitative intepretation
  - 25 um pitch in standard process using full analogue information yields better resolution (~2.7 um against ~4 um) than 15 um pitch with binary output in modified process

- CE65v2 was tested at DESY. Preliminary results are shown. Detailed analysis is underway

- Planned to test CE65v2 sensors:
  - Studying spatial resolution at **SPS in April 2024** . Important to compare for various **pitch** and **pixel geometries (regular & staggered)**

Thank you for your kind attention!

Backup slides

Large collaboration

Many contributors

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ER1 submission

ER1 Submission (12/2022)

Learn and prove **stitching**

- Methodology, Constraints, Yield

“**MOSS**”: 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18 μm^2)

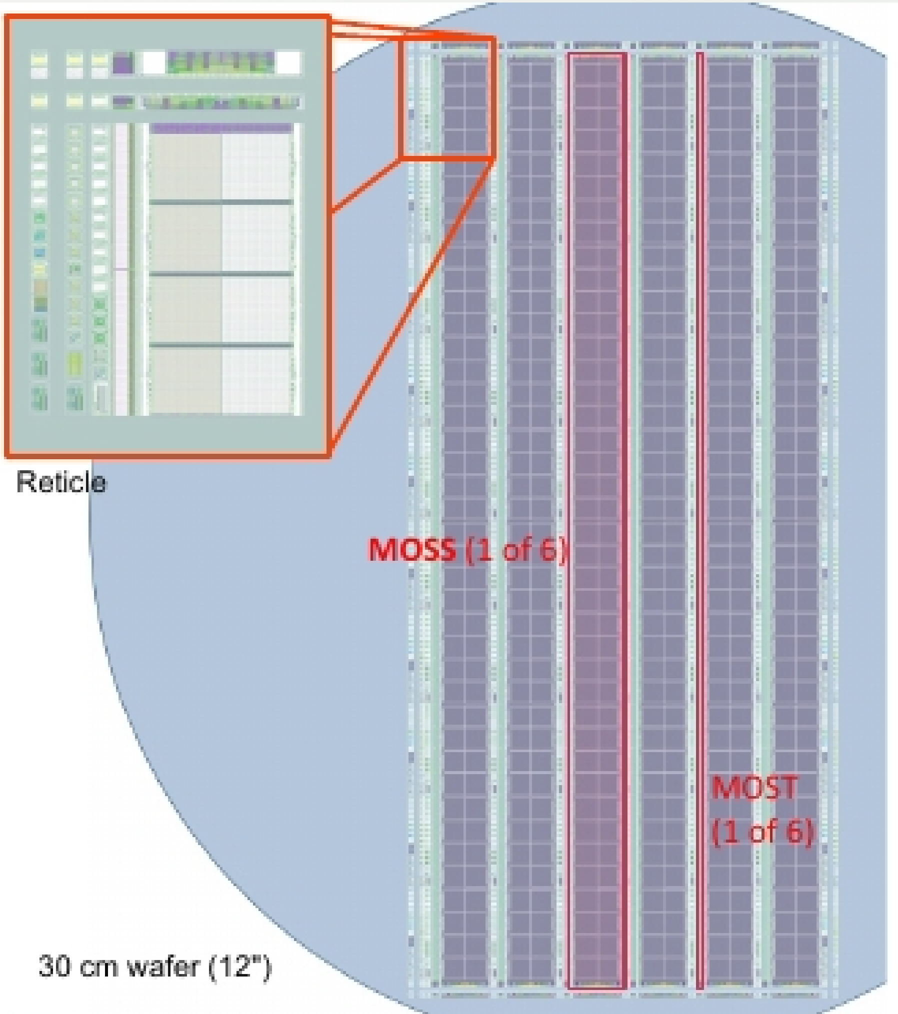
- conservative design, different pitches

“**MOST**”: 2.5 x 259 mm, , 0.9 MPixel (18 x 18 μm^2)

- more dense design, higher power granularity

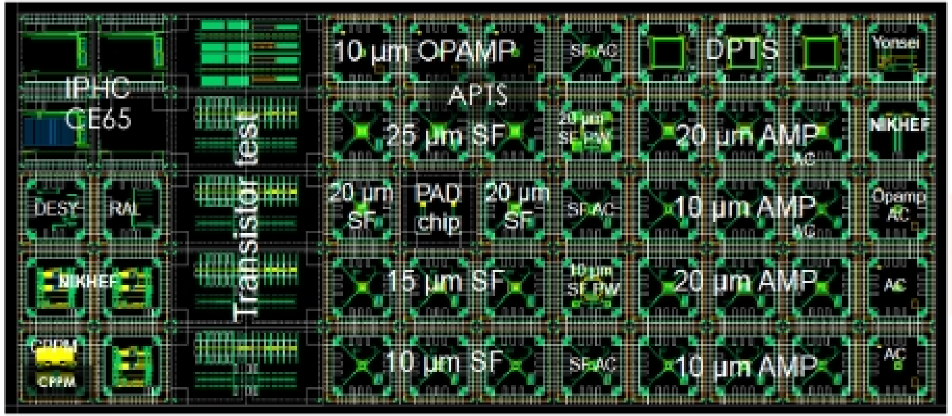
Small prototype and test chips (like MLR1)

- Pixel Prototypes
- Fast Serial Links, PLL, I/Os, SEU



Recap on 1st submission

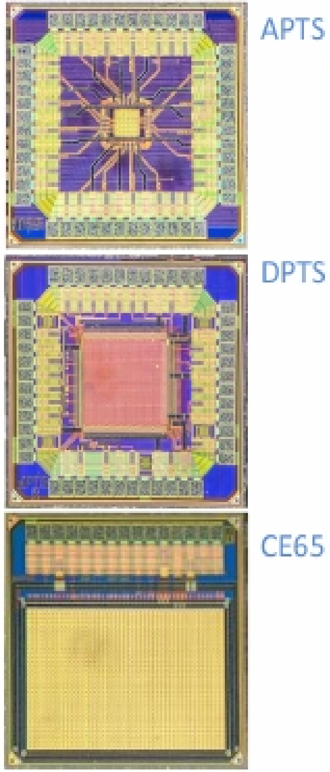
- Multi-Layer Reticule (MLR1)
  - 5 metal layers, HR thin (~10µm) epi layer



- IPHC: rolling shutter larger matrices, DESY: pixel test structure (using charge amplifier with Krummenacher feedback, RAL: LVDS/CML receiver/driver, NIKHEF: bandgap, T-sensor, VCO, CPPM: ring-oscillators, Yonsei: amplifier structures
- Transistor test structures, analog pixel (4x4 matrix) test matrices in several versions (in collaboration with IPHC with special amplifier), digital pixel test matrix (DPTS) (32x32), pad structure for assembly testing.
- After final GDS placement, GDS1 is instantiated twice.
- Converged with 4 splits of 3 wafers

CERN { (Transistor test structures … GDS1 is instantiated twice.)

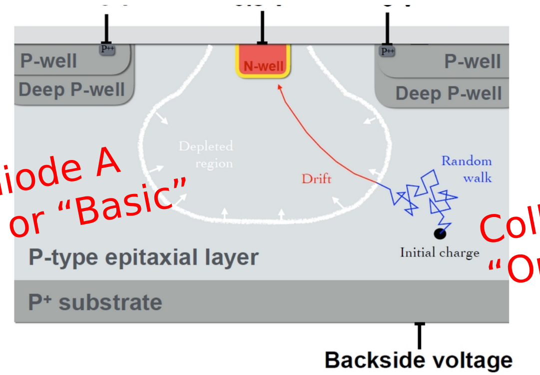
⇒ Sensors
- 10-25 µm pitch
- APTS = analogue outputs with OpAmp
- DPTS = digital outputs
- CE65 = analogue outputs with DC/AC and no-Amp/Amp



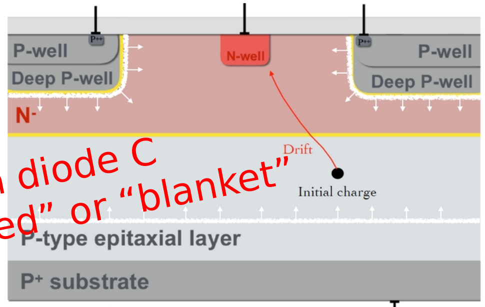
Slide: Jerome Baudot

TPSCo 65nm process modification

- 4 process splits
  - Doping modifications:
    1. Default process
    2. First intermediate process
    3. Second intermediate process
    4. Optimized process



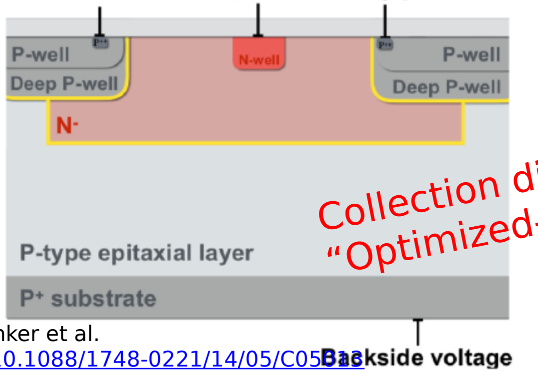
Collection diode A
“standard” or “Basic”



Collection diode C
“Optimized” or “blanket”

W. Snoeys et al.:
DOI: 10.1016/j.nima.2017.07.046.

- 3 collection diode structures
  - Following successful modifications in Tower 180 nm
  - Standard => Optimized(gap) structures



Collection diode B
“Optimized-gap” or “gap”

M.Munker et al.
DOI: 10.1088/1748-0221/14/05/C05013

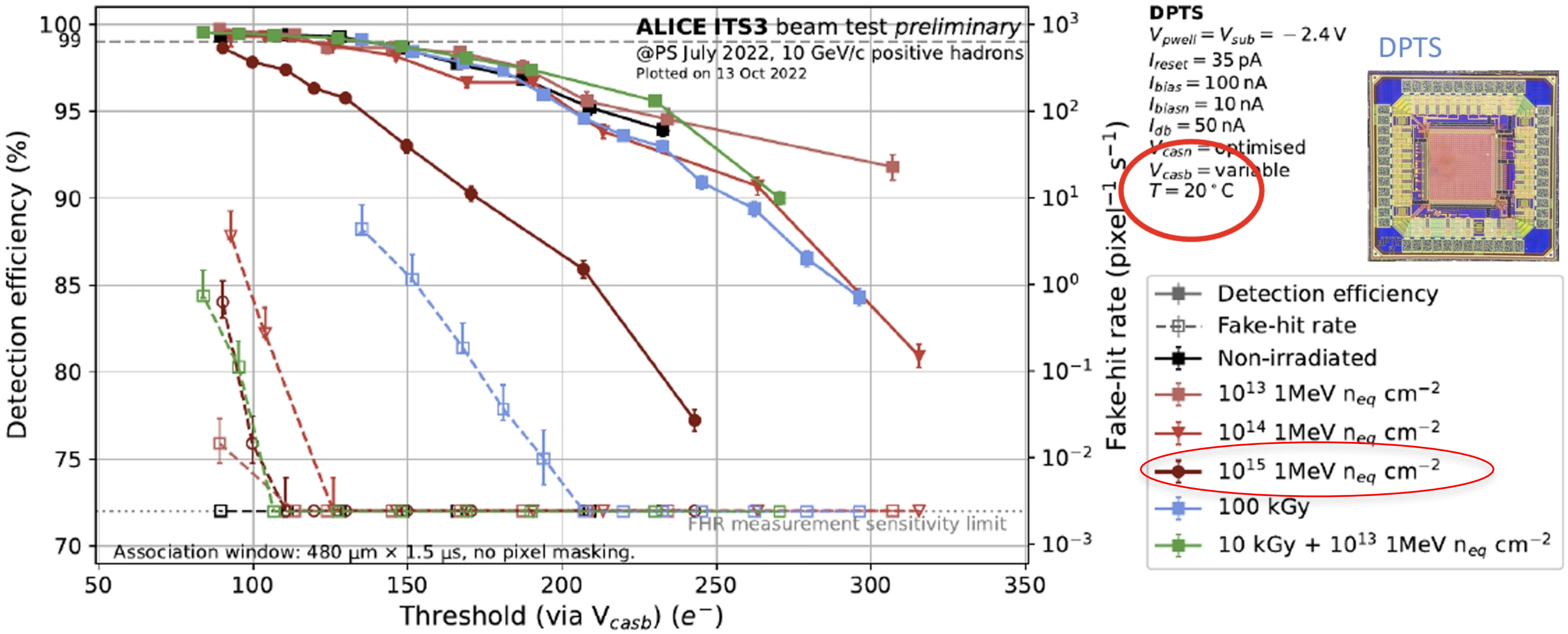
⇒ Both modifications based on TCAD studies

Stll on-going for subsequent submissions

MLR1 findings

- Promising radiation tolerance
  - DPTS (digital) with 15 µm pitch
  - Beam test results

S.Perciballi @ TREDI2023 https://indi.to/yD2ZF

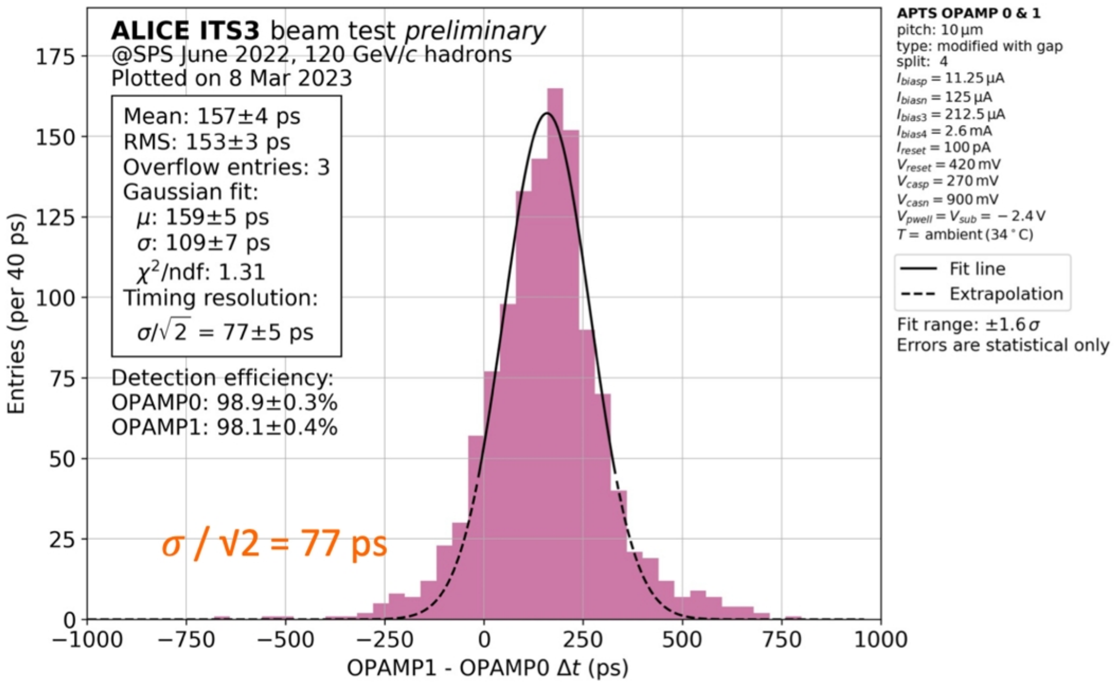


MLR1 findings

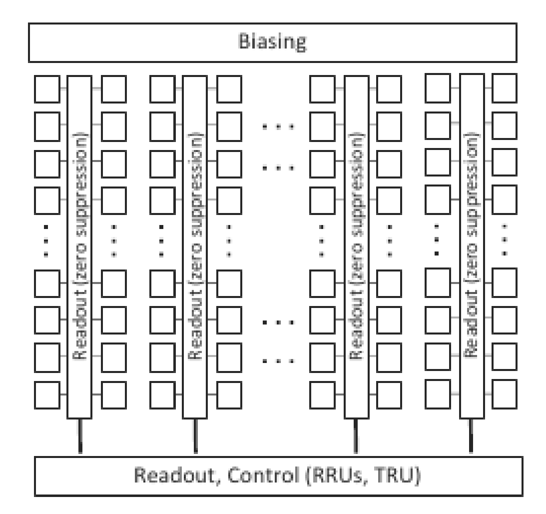
- Timing resolution

C. Ferrero @ TWEPP 2023

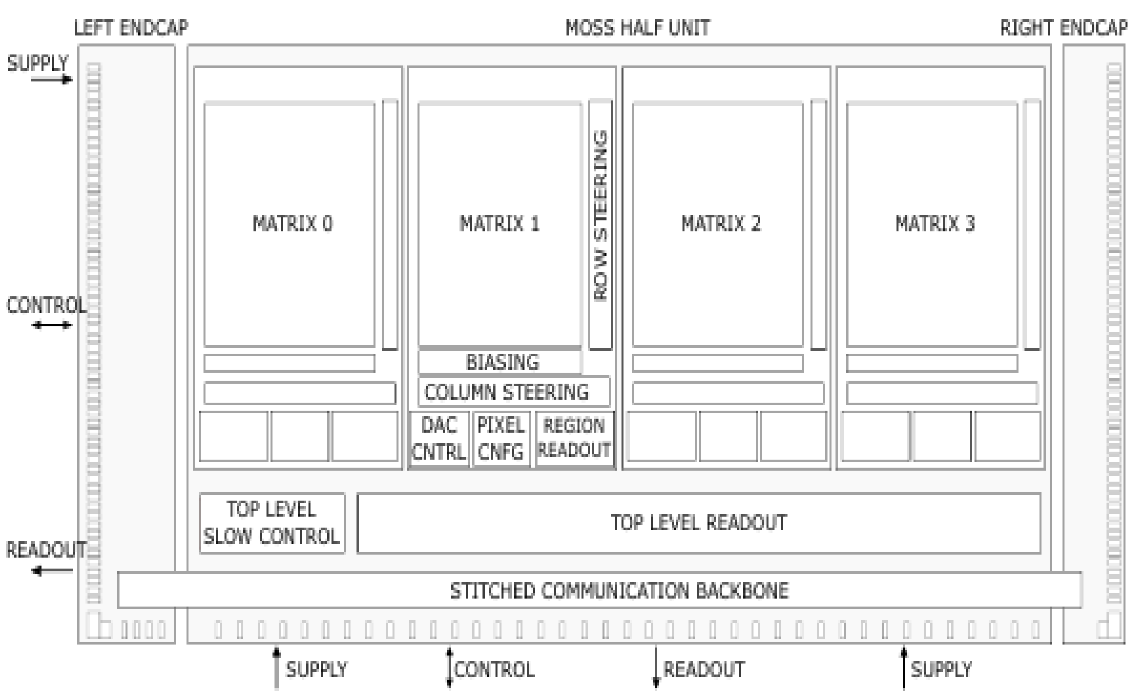
- Based on APTS, CE-65, DPTS: talks at IWoRiD2022, TREDI 2023, ULTIMA 2023
- Variety of pixel pitches: 10-25 µm
- Successful sensitive layer depletion
- Promising radiation tolerance
- Promising time resolution



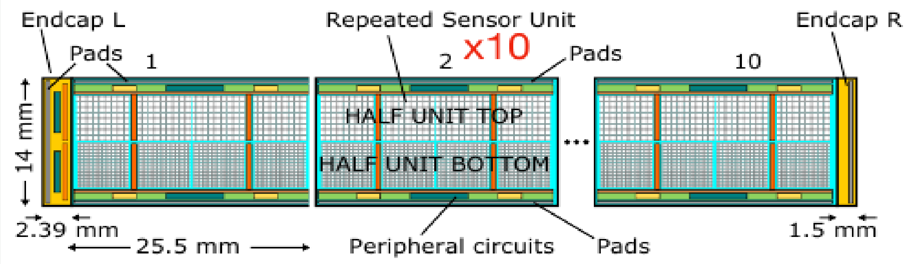
MOSS design



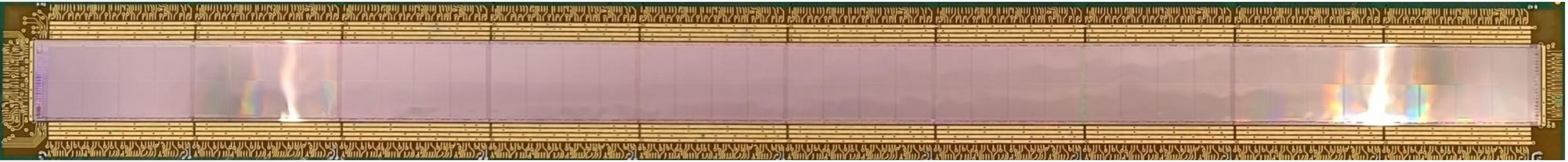
Biasing
Readout (zero suppression)
Readout (zero suppression)
Readout (zero suppression)
Readout (zero suppression)
Readout, Control (RRUs, TRU)



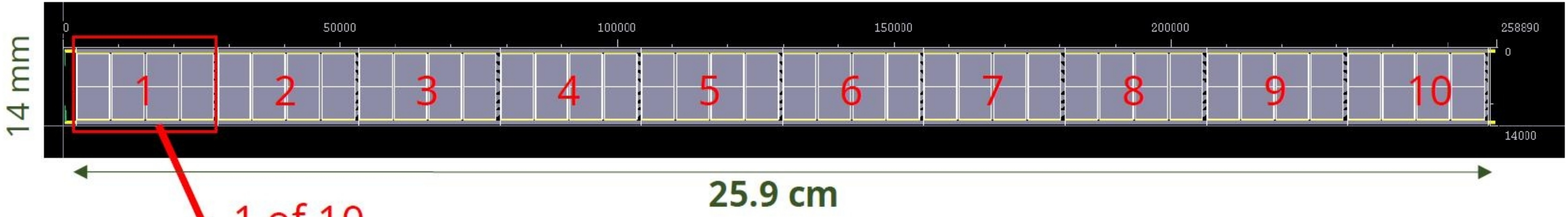
LEFT ENDCAP
MOSS HALF UNIT
RIGHT ENDCAP
SUPPLY
CONTROL
READOUT
MATRIX 0
MATRIX 1
ROW STEERING
MATRIX 2
MATRIX 3
BIASING
COLUMN STEERING
DAC CNTRL
PIXEL CNFG
REGION READOUT
TOP LEVEL SLOW CONTROL
TOP LEVEL READOUT
STITCHED COMMUNICATION BACKBONE
SUPPLY
CONTROL
READOUT
SUPPLY

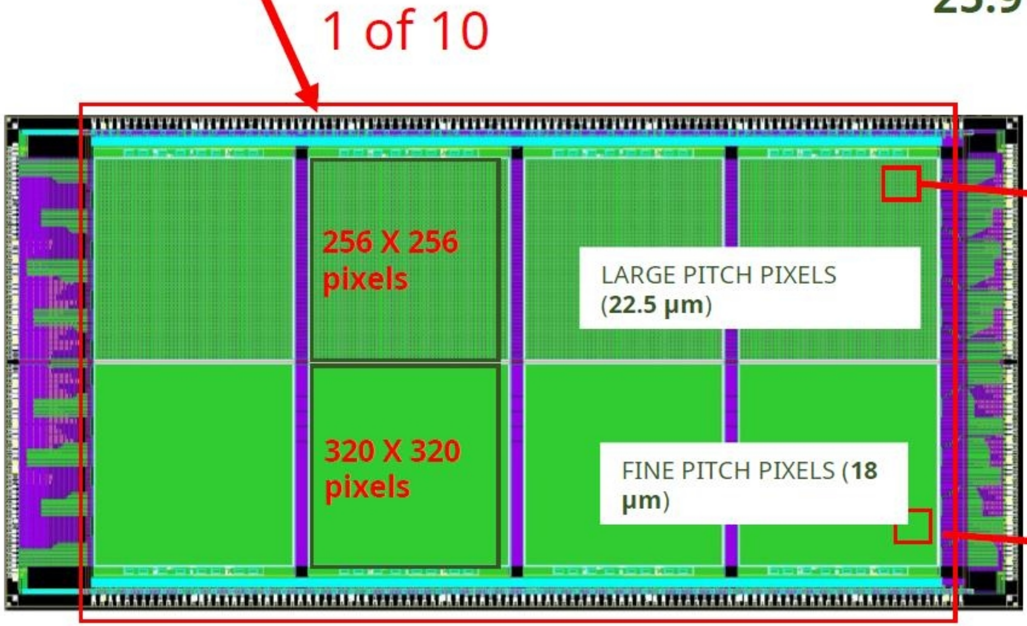


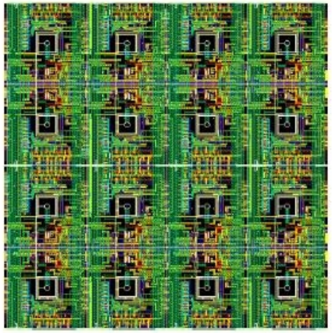
Endcap L
Repeated Sensor Unit
Endcap R
Pads
1
2
x10
Pads
10
HALF UNIT TOP
HALF UNIT BOTTOM
14 mm
2.39 mm
25.5 mm
Peripheral circuits
Pads
1.5 mm



MOSS design





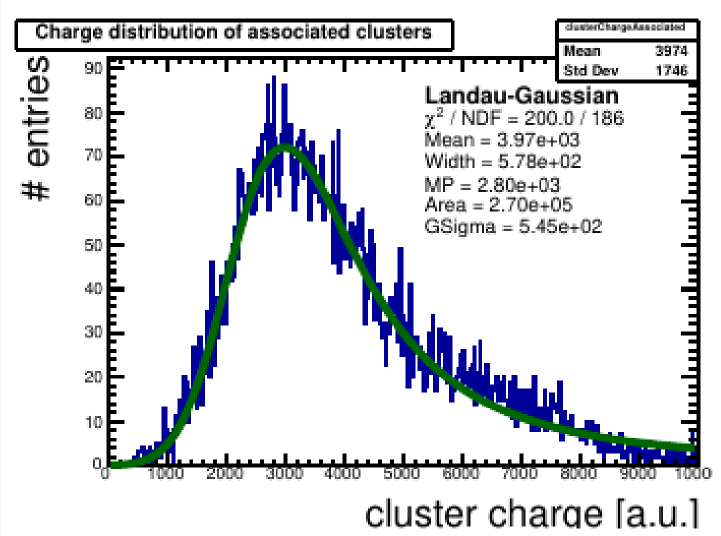


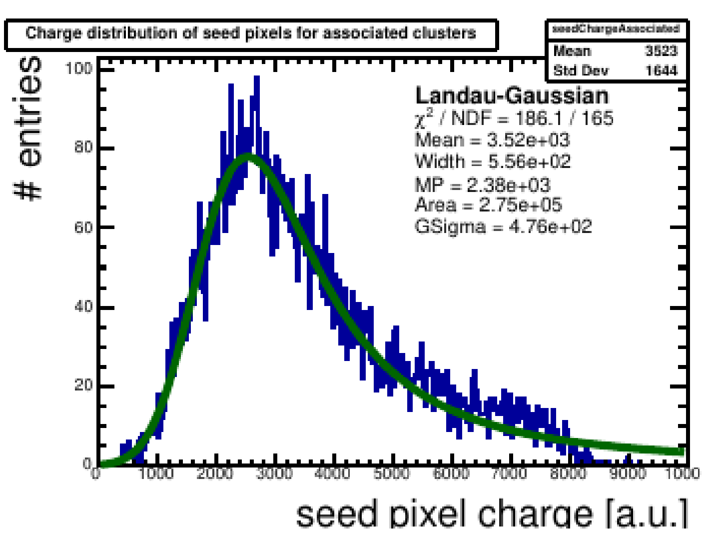
Pitch 22.5 µm
- Conservative layout
- 7 mW/cm2 (analog FE)
- 1us peaking time

Pitch 18 µm
- Compact layout
- 11 mW/cm2 (analog FE)
- 1us peaking time

- 1.4 x 26 cm monolithic stitched sensor

CE65v2 test beam





CE65v1 setup

Telescope:

Reference Arms : 4 ALPIDE planes for track reconstruction
DUT : CE65
TRG : DPTS

Test beam:

May 2022 at CERN-PS

Data acquisition:
EUDAQ2
Event reconstruction algorithm and data analysis framework:
Corryvreckan

Noise run-**Beam** run:
correlated double sampling method (**CDS**)

Support provided by Alice Collaboration