

#### Advancement and Innovation for Detectors at Accelerators

#### **Subtask 8.4.2:**

# Development of highly granular dual-readout fibre-sampling calorimeter

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On behalf of the IDEA dual-readout calorimeter group







- Status report on the ongoing activities to build the demonstrator
- Test beam plans and more

Deliverable Number <sup>14</sup>	Deliverable Title	WP number <sup>9</sup>	Lead beneficiary	Type <sup>15</sup>	Dissemination level <sup>16</sup>	Due Date (in months) <sup>17</sup>
1 1 X /1	Construction and qualification with beam of 10×10 cm <sup>2</sup> , 2 m long, prototypes	WP8	22 - INFN	Demonstrator	Public	46



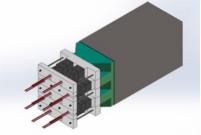
### New geometry of the HiDRa detector

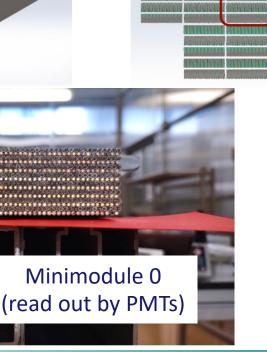
5-Minimodules = 1 Module

Outer shell: Each minimodule is read out by 2 PMTs (1 for Cherenkov and 1 for scintillation)

High granularity core: fibres individually read out by SiPMs











# Material procurement and assembly program

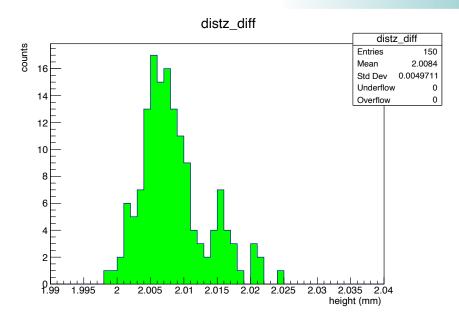
- Capillary tubes: arrived
- Cherenkov fibres: arrived
- Scintillating fibres: 7 batches arrived -> next, 1 batch/month
- PMTs: 100/140 available (others to be ordered in 2024)
- SiPMs: order completed (delivery time delayed -> will be estimated soon)
- High granularity readout boards: 10/20 available (others to be ordered in 2024)
- Assembly (net) time for one minimodule
  - Gluing: half a day
  - Mechanics QAQC procedure: half a day
  - Threading the fibres: 2 days

Partially in parallel -> foreseen two minimodules/week

18 minimodules completed



#### QAQC on components



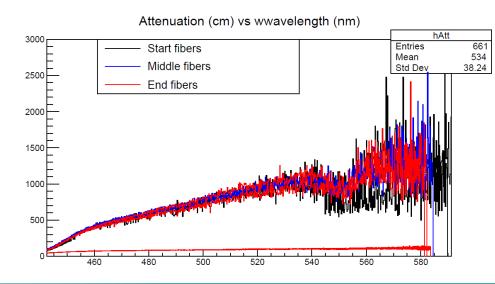
Scintillating fibres: sampling measurements of attenuation length

Rejected: 5-10 % (preliminary estimate)
Because of anomalous attenuation length,
air bubbles and damage during handling

Sampling measurements of tube outer diameter Other checks:

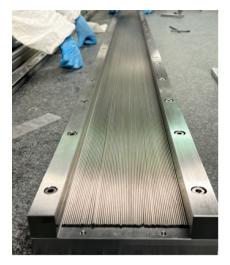
- Straightness
- Inner diameter (pass/fail test)
- length

Rejected: 5-10 % (preliminary estimate)
Mainly because of poor straightness

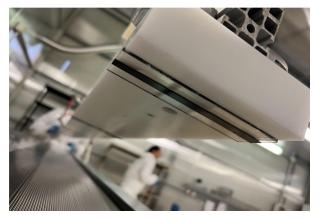




### Construction technique for the minimodule



Assembly reference structure anchored to the granite table with the 1<sup>st</sup> layer of tubes in place



Vacuum + double-sided tape for tube handling









Glue dispensing and tube alignment and positioning

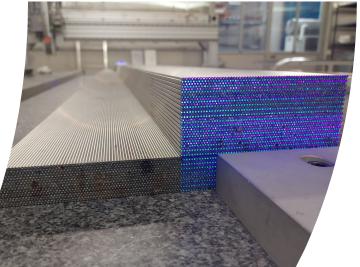


### Construction technique for the minimodule

- Measurement of modules planarity
- Fibre loading and grouping
- Preparation for PMT coupling

 next to come: qualification with the PMT





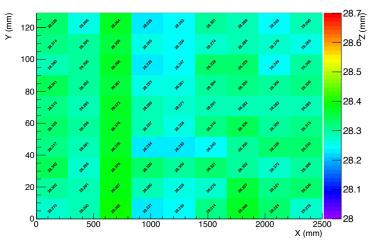


Semi-automatic system for planarity QAQC

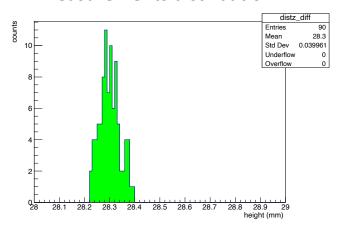


### Typical Result for a minimodule

9 measurements along the tubes (x-axis) and 10 measurements across the minimodule surface (y-axis)



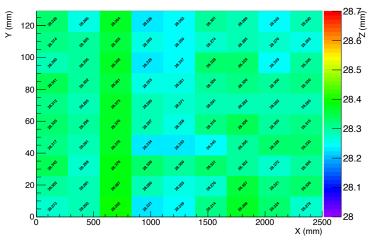
#### Measurements distribution



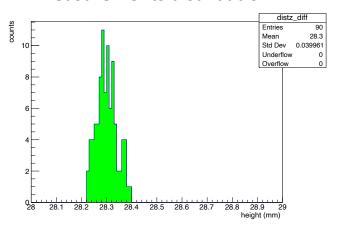


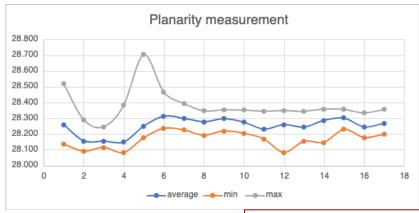
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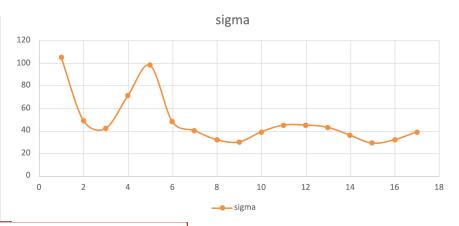
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#### Measurements distribution







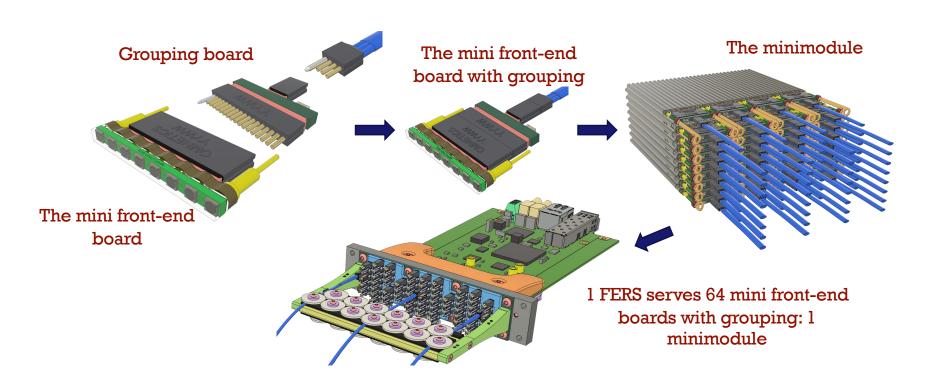
Summary from all mini-modules assembled so far

2024



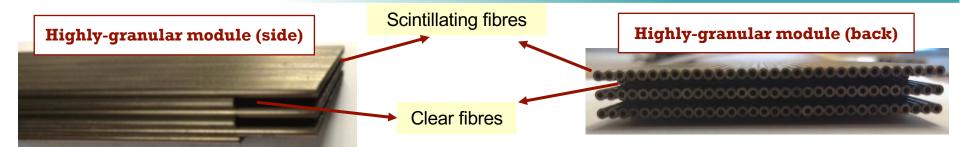
### Highly granular module in short

#### The original design



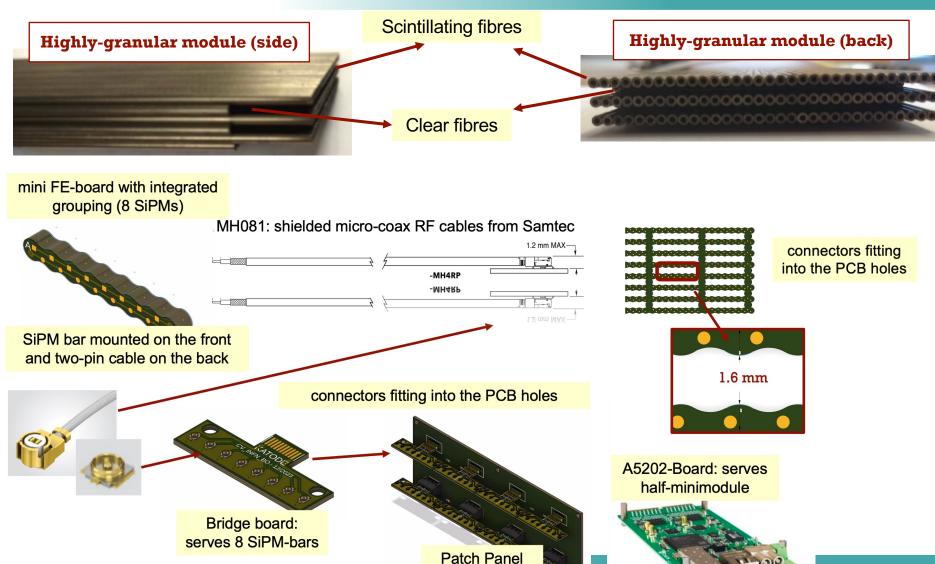


### Mechanical integration and cabling



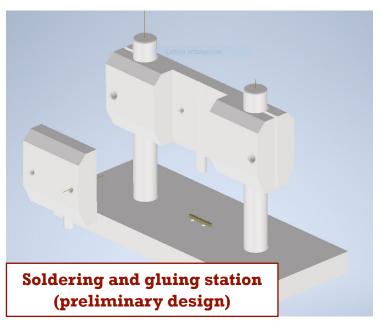


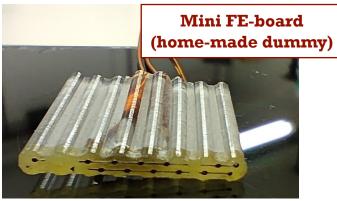
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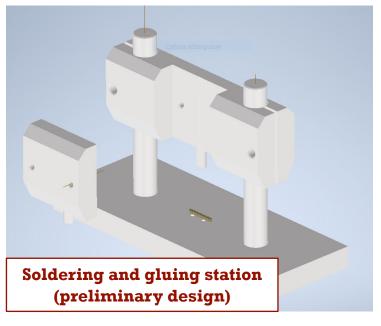
# Integration studies with dummy components

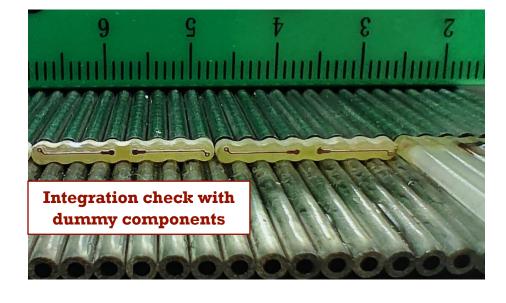


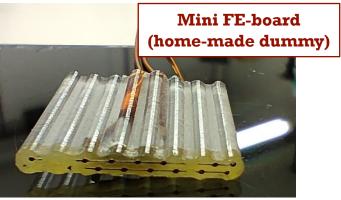




# Integration studies with dummy components





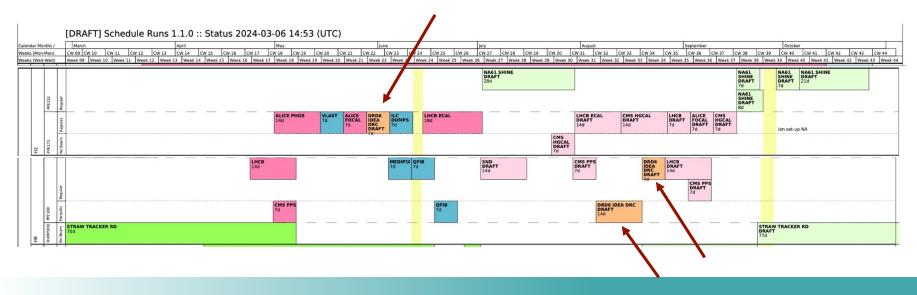






#### Test beam activities

- 4 weeks allocated (1 week in H2, 2+1 weeks in H8)
  - https://ps-sps-coordination.web.cern.ch/ps-spscoordination/schedules/ps/2024/v1.1.0/schedule runs v110 20240306 all.pdf
- Beam time will be shared internally based on the scientific program, hardware available and deadlines with funding agencies
  - Three main groups (DRD6-WP3, Task 3.3.1).
  - Details on the activities can be found here: https://indico.cern.ch/event/1386879/
- Schedule is still preliminary: there are two weeks with two groups running parasitic without a main user (to be fixed)





# Activity of interest (DRD4 – WP4.1)

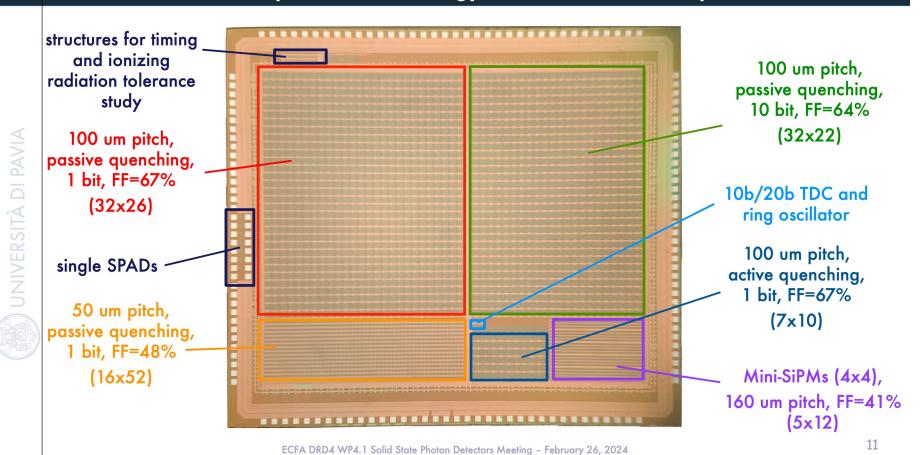
#### **Activity program**

- Development of a technology platform for digital SiPMs in applications to dual-readout calorimetry - activity extending over a 3-4 year span
- Involving some of the groups participating in DRD4, with possible contributions from other Italian groups - proposal to be presented to INFN at the beginning of Summer
- Characterization of the ASAP110LF test chip developed in a 110 nm CMOS technology, including different SPAD arrays with different features (passive and active quenching, different active area, structures for investigating timing properties and ionizing radiation tolerance) and mini-SiPMs
  - DCR, breakdown voltage, afterpulsing, electrical and optical cross-talk, also as a function of the temperature
  - QE and PDP/PDE
  - Time resolution
- Investigation of the cumulative damage from ionizing radiation (X-ray) and from atomic dislocation in the substrate (neutrons, protons)

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#### Activity of interest (DRD4 - WP4.1)

#### ASAP110LF chip - a technology characterization platform





## Activity of interest (DRD4 – WP4.1)

#### **Activity program**

- Development of small scale prototypes of CMOS SiPMs consisting of about 1000 SPADs with 15-20 um pitch
  - o for the readout, both a fully digital and a mixed analog and digital approach will be explored best compromise between detection efficiency (fill factor) and functional density
  - on sensor electronics to be provided with event detection, counting, thresholding and time stamping capabilities, possibly together with the ability to follow the time evolution of the light pulses reconstruction of the longitudinal shower and discrimination between Cherenkov and scintillation signals
  - specific structures included to test the chip functionalities
- o Development of a demonstrator chip including 8 SiPMs, each with a 1 mm<sup>2</sup> area
  - o inter-SiPM region used for integrating most of the electronics, to minimize the impact on the fill-factor
  - characterization to be performed in the lab and possibly in a beam test
- Possible extension to other applications with the involvement of other groups

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#### Thank you for your attention







### Activity of interest (DRD4 – WP4.1)

#### Mini-SiPM with parallel counter

- The SiPM contains 16 SPADs, arranged in a 4x4 array, and a processing circuit.
- The 16-bit input parallel counter provides in real time the number of simultaneously triggered SPADs.
- The count result is fed to the memory elements through an auto-triggering mechanism, which filters out spurious glitches coming from the counter.
- A SOT logic has been implemented.
- A noise rejection feedback network (NRFN) has been designed to filter out individual dark pulses.

