Integration aspects of highly granular calorimeters
WP8 T2.1

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for

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DESY-HH, FZU, JGU, TAU

materials from Y. Benhammou, A. Irles, K. Kruger, J. Maalmi E. Sicking *and others*

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WP8 Task 8.2/1

Task 8.2.1 Towards next generation highly granular calorimeters

Task 8.2.1

- Development of a common electromagnetic and hadronic calorimeter data concentration interface for minimised space and power consumption
- Demonstrator with functional active detector elements and full read-out chain (D8.1)

Integration aspects of highly granular calorimeters

Highly granular electromagnetic and hadronic calorimeters at future colliders will have up to 10^8 readout cells, calling for common solutions for services such as data concentrators interfacing the embedded front–end electronics and the data acquisition outside the detector.

⇨ *This subtask will develop* ***compact and innovative data concentrator and power distribution units****, serving more than 10^6 cells and satisfying the tightest space and power constraints.*

⇨ *The technical solutions will be embedded in* ***a demonstrator*** *that will be* ***applicable*** *to particle physics detectors at future e+e− colliders such as ILC, CLIC, CEPC, FCC-ee.*

For this demonstrator, mechanical structures and silicon and scintillator ***based active elements will also be provided***

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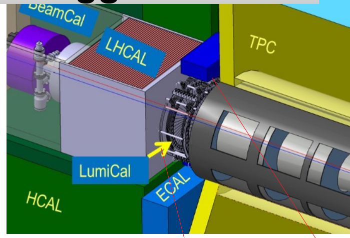
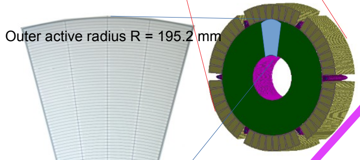
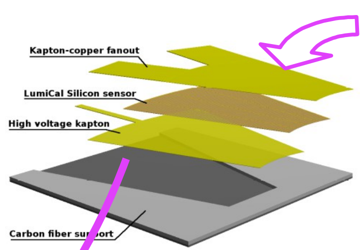
A Map to High-Granularity Calorimeter Prototypes

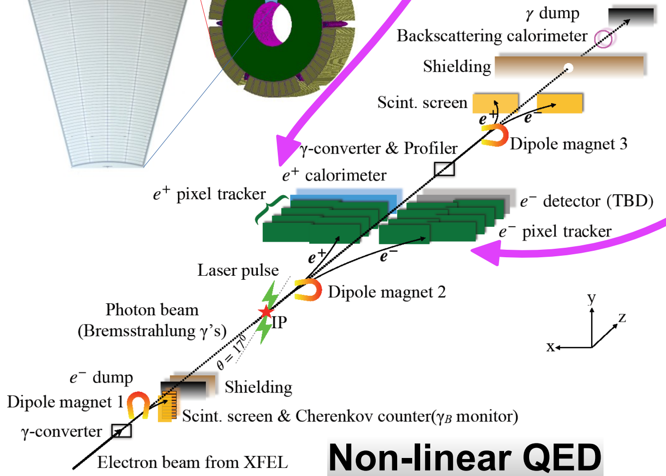
FCAL for ILD, LUXE

For Higgs Factories





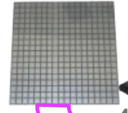




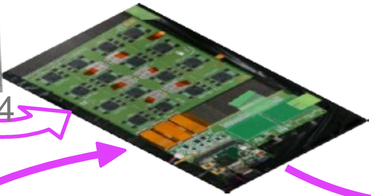
Non-linear QED

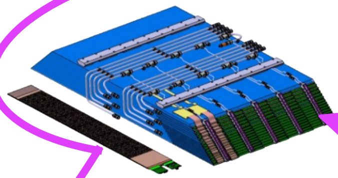
SiW-ECAL for ILD, LUXE

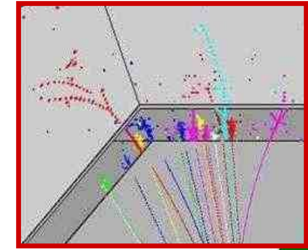
Si 5×5 mm²



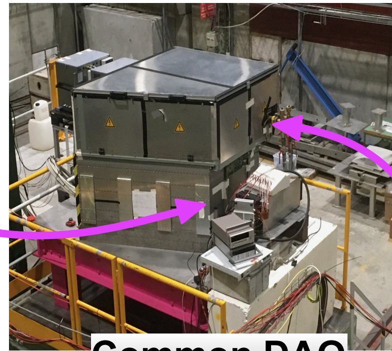
× 4



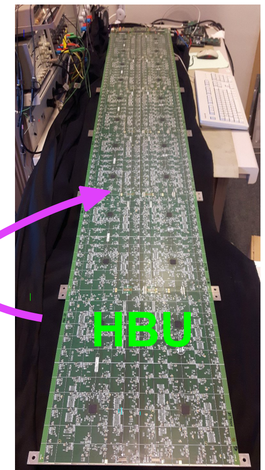


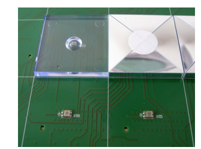


AHCAL for ILD

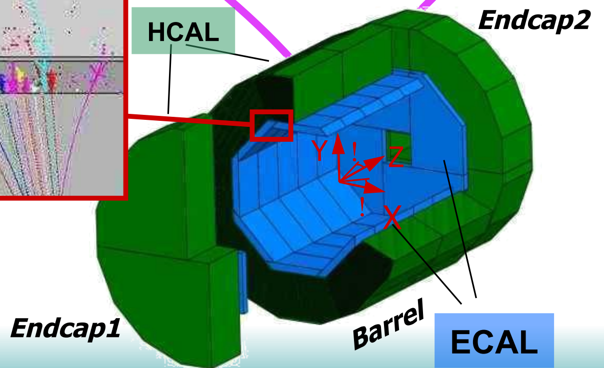


Common DAQ

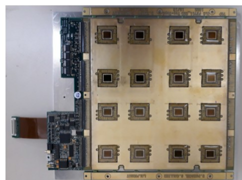


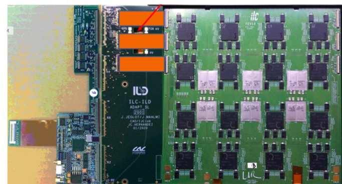


Scint 3×3 cm²



SiW-ECAL Technological Prototype beam test at DESY & CERN





FEV10, 11, 12

- BGA packaging
- Incremental modifications
- From v10 -> v12
- Main “Working horses” since 2014

FEV-COB

- Chip-On-Board : ASICs wirebonded in cavities
  - Thinner than FEV with BGA
- Based on FEV11
  - External connectivity compatible

FEV13

- BGA packaging
  - Improved routing
  - Local power storage
  - Different external connectivity

mpv_layer7_xy

mpv_layer3_xy

No problem since no beam expos

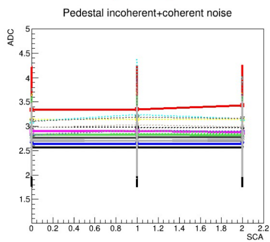
mpv_layer4_xy

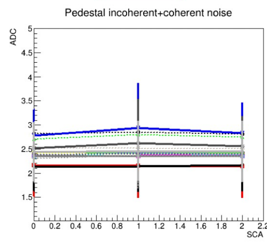
- We have good layers ...
  - Homogeneous response to MIPs over layer surface
  - Here white cells are masked cells due to PCB routing
    - Understood and will be corrected

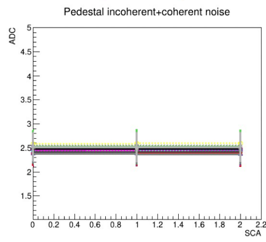
... and not so good layers

- Inhomogeneous response to MIPs
  - Partially even no response at all, in particular at the wafer boundaries
  - To be understood, may require dedicated aging studies
- Have since last week access to the different stages of the ASICs
  - => major debugging tool
- In any case less good layers will be replaced in coming months

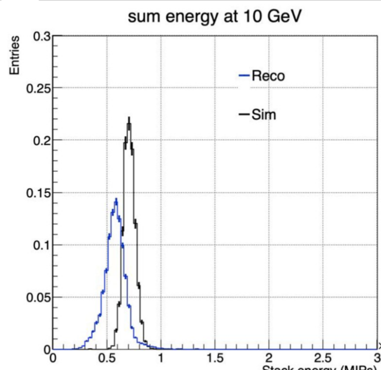
Pedestal widths, 1st memory cells, per asic



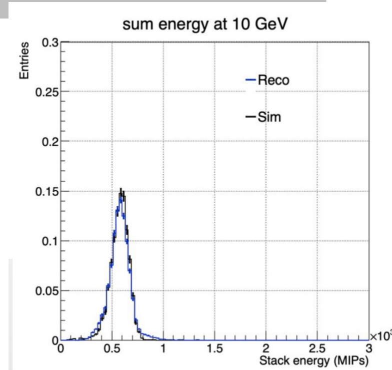




- (Average ± Standard Deviation) of Sigmas for all 64 channels in the same chip
- Latest PCBs, with optimized routing of power distribution shows better behavior
- Slightly larger spread on COB due to a near lack of decoupling capacitors



Masking Beam profiling



Yuichi Okugawa (PhD in Feb.

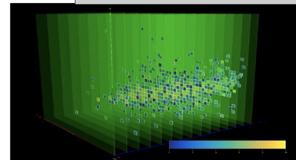


Fig. Simulation e- 100 GeV

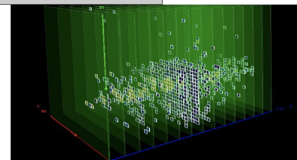
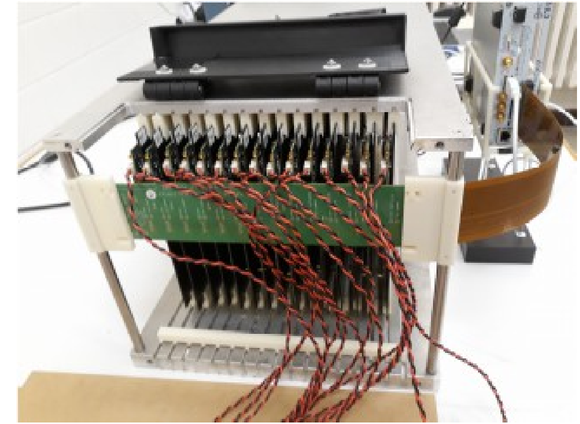


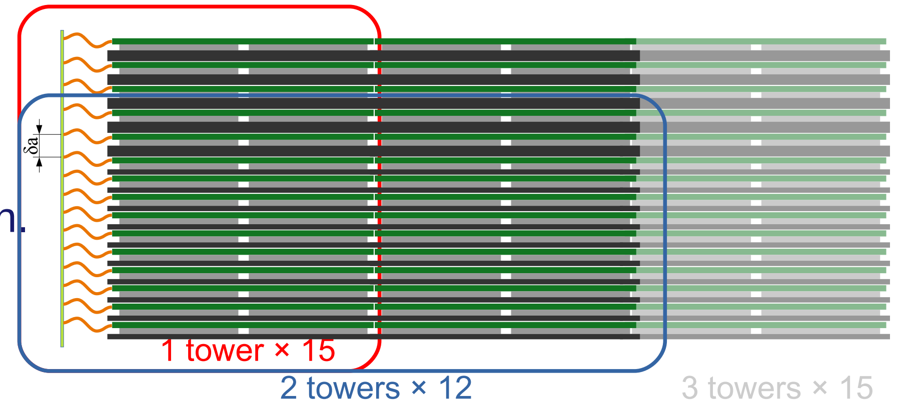
Fig. Reconstructed e- 100 GeV

Building of a uniform SiW-ECAL prototype

Rationale:

- Current prototype
  - 4(5) types of PCBs №3 sensor thicknesses (320, 500, 625 μm)
  - (un)gluing issues
- Material for 15 ASUs available → full single tower
  - FEV2.1 boards, wafers, components
- Application cases : LUXE@XFEL, EBES@KEK, Lohengrin@ELSA
  - Extreme QED & Dark *γ* searches
  - low energy, rates, …
  - LUXE: FCAL prototypes → common DAQ Application.
  - Could be built from *same cards* in 2×12
    - Needs: sensors (€), (Mech. structure), W





→ Homogenous prototype

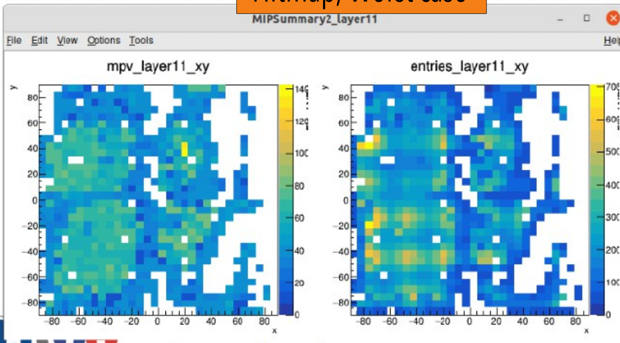
Goal:

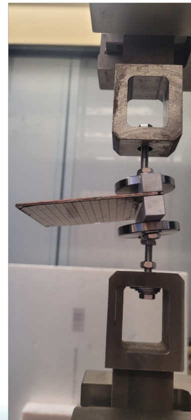
- **15 layers of FEV2.1 with 500µm wafers**
  - Uniform and more performant electronics
  - Could be used for LUXE and Dark Photons exp's.
- **All material available**

Main issue: contact PCB–Sensor

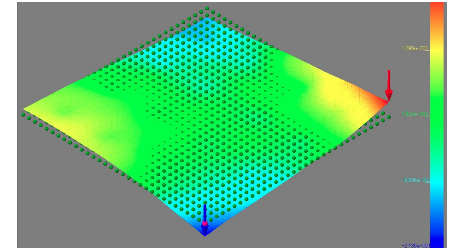
- **Conductive glue dots of A2–3mm**
- **Aging, mechanical stress, manipulations. ..**

Hitmap, Worst case

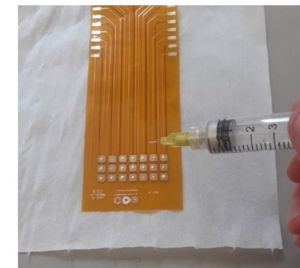


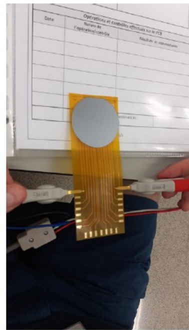


Revisiting gluing (IFIC, IJClab, LPNHE)

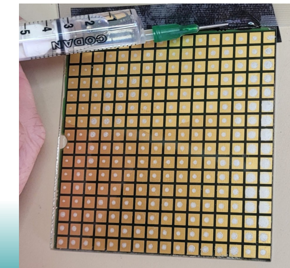


- **PCB metrology**
  - Bef. & After curing & soldering
- **Glue formula & preparation**





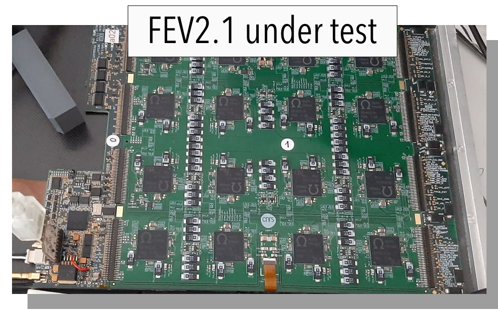
- **Gluing methods**
  - Robot
  - Stencil
- **Reenforcement**
  - Filling glue
  - Adhesive films

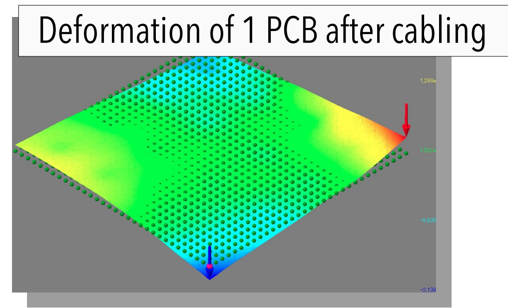


New hardware for the SiW-ECAL

30 PCB of new type (FEV2.1) have been produced

- **1st batch of 4 cabled for tests**
- **1 equipped with 4 baby-wafers for HV test**
  - Test on-going
- **Mechanical test made at IFIC Valencia**
  - Not all satisfactory (flatness ±200µm in the corners after the cabling involving heating at 300°C); further investigation on the cabling process foreseen

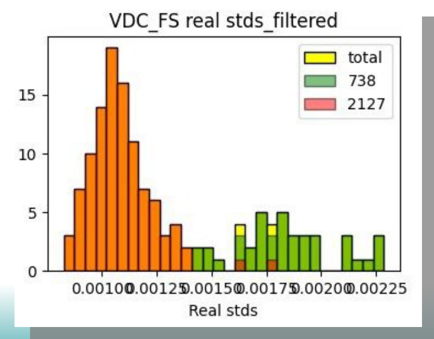




Testing of Skiroc2 ASICs:

- **~ 1/3 of ASICs tested thoughroughly on dedicated bench at Ωmega lab prior to soldering on PCB's**
  - Statistical analysis completed; testing of the rest will resume soon.
- **64 (4×16) mounted on the FEV2.1**
  - Performances (noises, thresholds, …) will be compared with bench results.

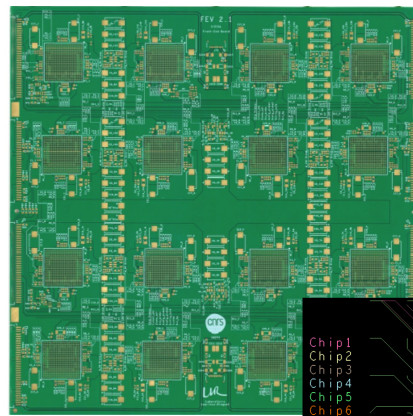
RMS of Fast Shaper for 2 type of packaging

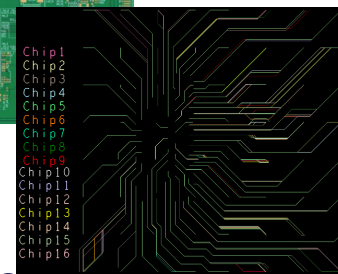


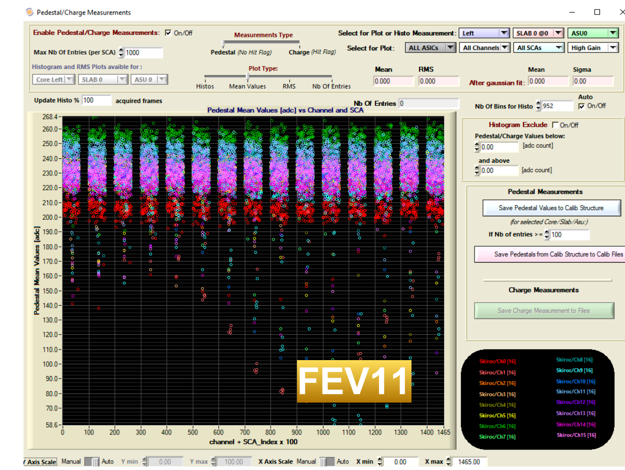
New FE boards

Improvements:

- Power distributions
  - Local power regulation: LDO's
  - Local High Voltage filtering & Supply
- Signal distribution (buffering), data paths
- Monitoring (single ID, temp, probe analogue line)
- ASIC shielding/routing



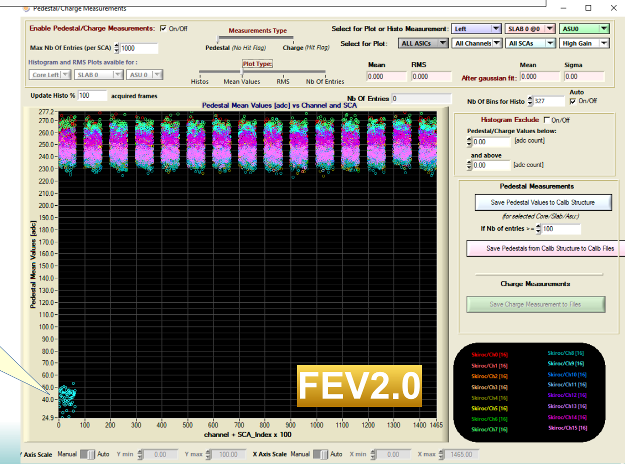




Pedestal measurements vs. Ch# + Mem# × 100)

Status:

- pre-version 2.0 tested, minor corrections needed
  - Noise uniformity dramatically improved (ex: outliers in thr. / 20 !)
- version 2.1 produced
  - before cabling, 2nd metrology, gluing, …
  - All material available : ASICs being tested

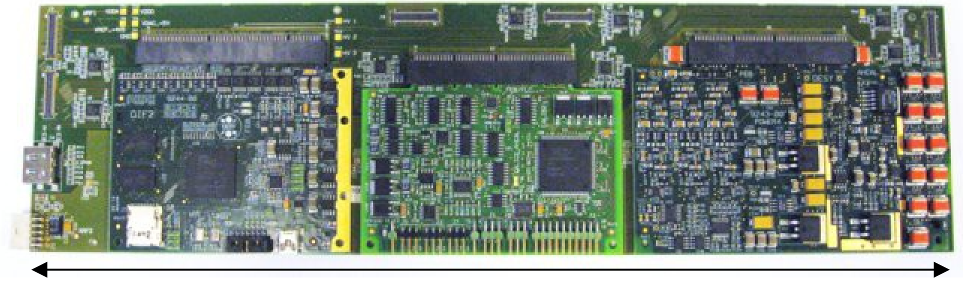


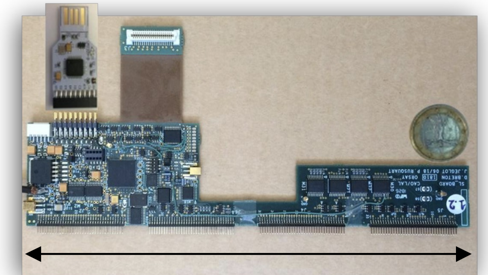
SIngle channel Ã the fault on the ASIC/packaging

AHCAL Plans: Hardware Developments

Common Readout

- Harmonize readout between CALICE SiW ECAL and AHCAL
- Reduce size of AHCAL interface boards
  - Current design is from 2007
  - Focus was on modularity
  - New SiW ECAL interface board (SL board) optimized for compactness
  - Plan to follow SiW design as much as possible
    - Some differences in powering concept
    - Additional LED calibration system in AHCAL
- Status: just started





Delay in D8.1

D8.1 :

- “Demonstrator of a combined read-out system of highly granular electromagnetic and hadronic calorimeters” **is due M36 (March, 2024)**
  - The development of common DAQ interfaces imply a knowledge/technological transfer from the SiW ECAL to the AHCAL
  - The process is started, but the board design, testing and operation are delayed
- **External events prevents delivery in due time:**
  - The SiW-ECAL wafer-PCB delamination problem needs to be solved before any further test can be made; it was raised as the highest priority on the path to the production of new ASUs.
  - The DESY AHCAL team is responsible for the production of the board for the CMS HGCAL HCAL part;
the unexpected observation of the freezing of radiation damage annealing at -35°C in scintillators forced an urgent change of design, especially of the electronics boards, which has the priority.
- **A delay of the deliverable by six months** to M42 (September, 2024) would allow to produce a few boards for a proof-of-principle test of the SiW-ECAL, which would then form the basis of the transfer to the AHCAL. A combined test of a couple of layers at DESY SiW-ECAL+AHCAL is foreseen for June 2024.

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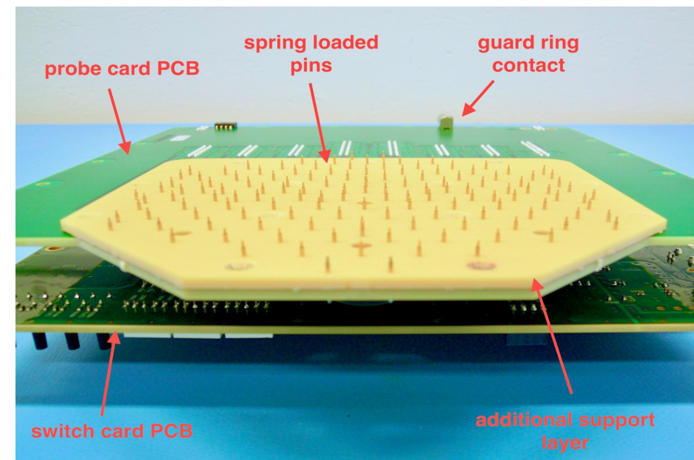
Wafers testing with CERN test bench

- **Probe board adapted to CALICE wafers (90×90 mm², 256 pads) has been designed and produced**
  - 2 for LUXE @ TAU (Tel Aviv),
  - 1 for CALICE/LUXE @ IFIC Valencia
- **A test bench is being mounted at IFIC**

System needed for electrical sensor characterisation in prototyping phase and for quality control in mass production (IV, CV, V_{BD}, V_{FD}, C_{FD})



Calice TAU sensors for LUXE

90 CALICE sensors received mid November

A probe card was designed and received in November from CERN (paid by TAU and IFIC).

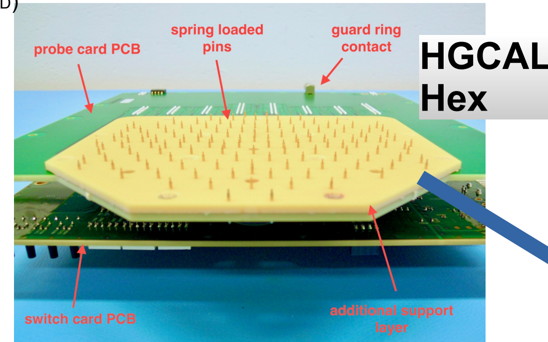
December :

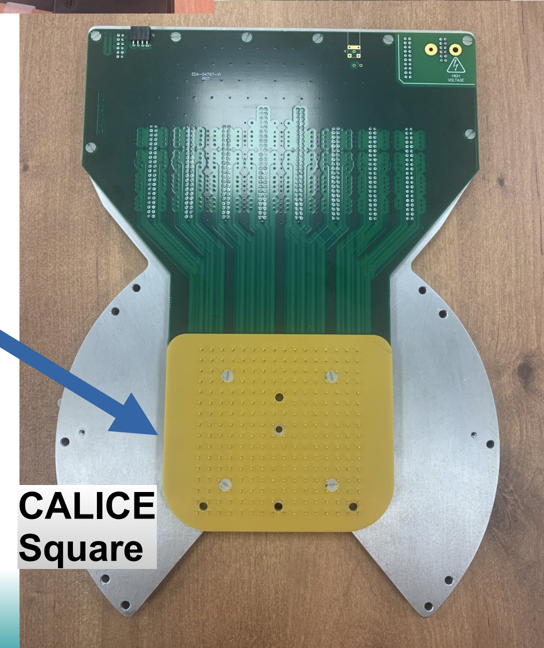
- **modification of the probe station mechanics and installation of the probe card**

January :

- **we checked the LUT of the pins (pins number ↔ DAQ channel)**
- **Started to test first sensors.**
- **Taking time to define the test procedure**

System needed for electrical sensor characterisation in prototyping phase and for quality control in mass production (IV, CV, V_{BD}, V_{FD}, C_{FD})





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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16