The Silicon Electron Multiplier, report

19th March 2024

AIDA Innova 3rd annual meeting

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AIDA innova

EP R&D

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CNM Centro Nacional de Microelectrónica IMB

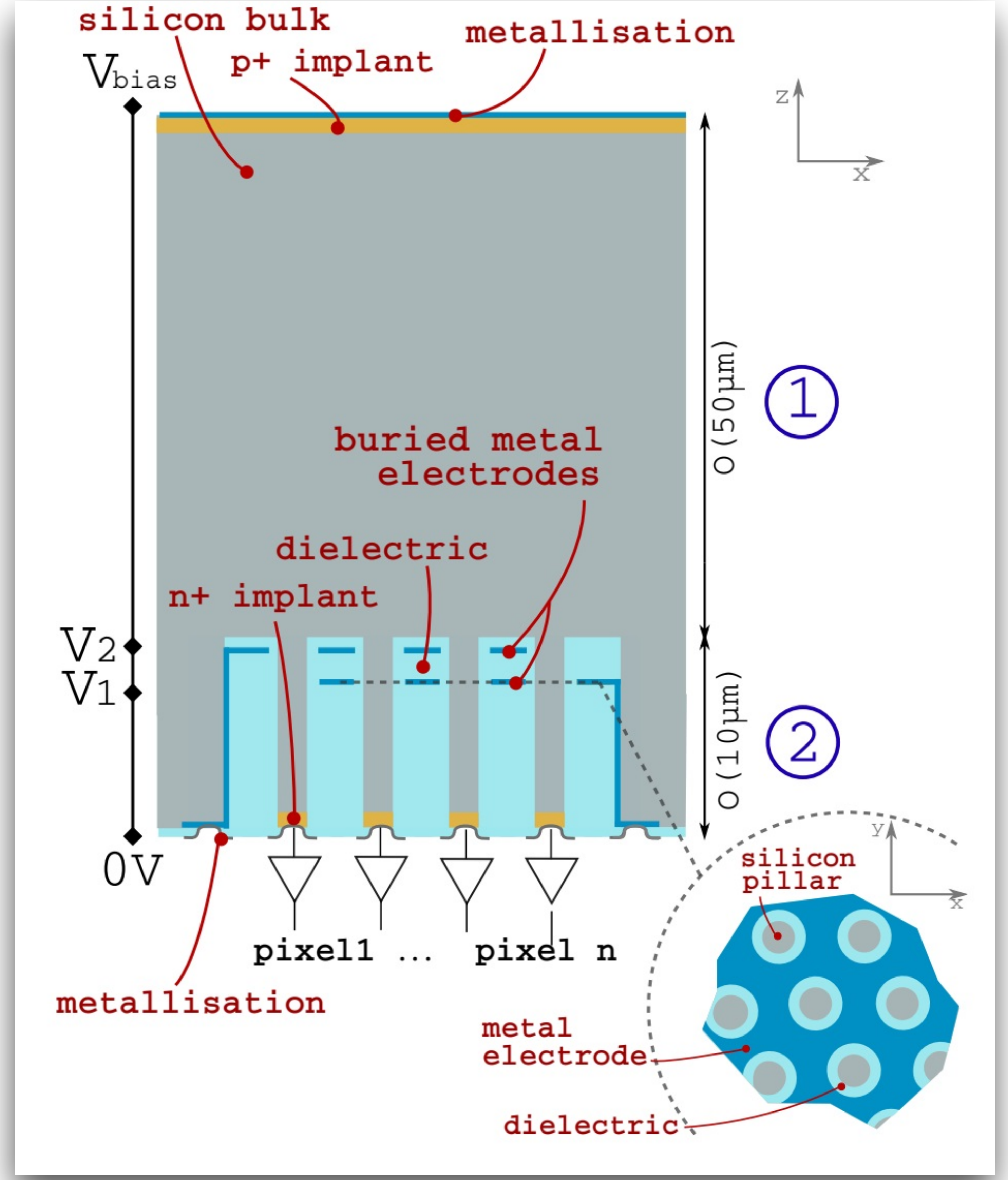
MOTIVATIONS

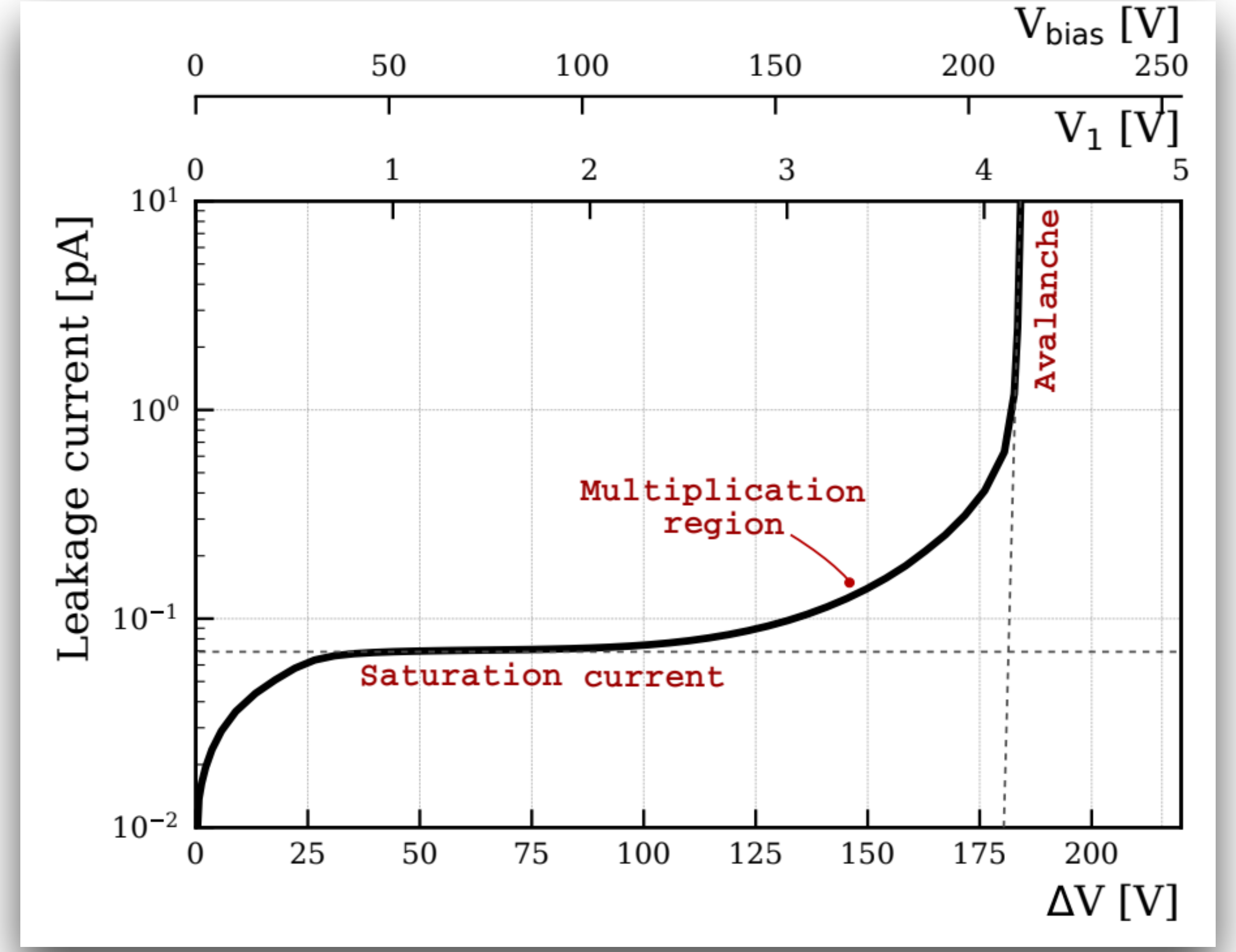
- New HEP accelerator applications require increasing radiation hardness (cumulative dose per year).
  - From $5x10^{15}$ n eq /cm^2 in ATLAS IBL lifetime to 10^{17} n eq /cm^2 in FCC hh per year.
- Inner trackers start requiring excellent time resolution.
- High pile up requires finer granularity.
- *Challenge: pixelated detector with resolutions of down to 10 ps , able to survive high fluencies.*
- Several sensor technologies available: 3D, MAPS, LGADs....
- **Is it possible to achieve internal gain without radiation damage sensitivity and 100% fill factor?**

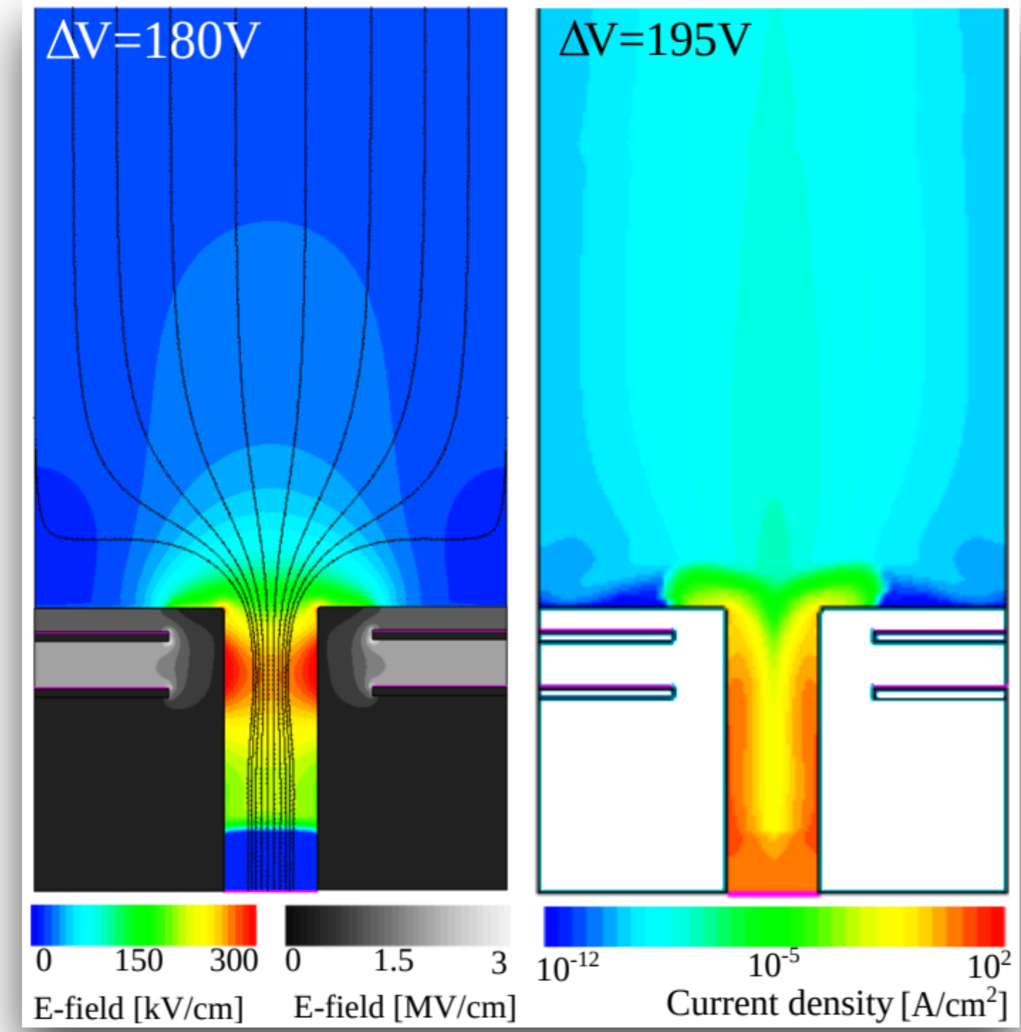
[fineprint in CERN-OPEN-2018-006]	HL-LHC	SPS	FCC-ee	FCC-hh
Fluence [$n_{eq}/cm^2/y$]	$5x10^{16}$	10^{17}	10^{10}	10^{17}
Max Hit rate [cm^{-2} s^{-1}]	2-4G	8G	20M	20G
Material budget per layer [X_0]	0.1-2%	2%	0.3%	1%
Pixel size [μm^2] inner trackers	50x50	50x50	25x25	25x25
Temporal hit resolution [ps] inner trackers	~50	~40	-	~10

SiEM PRINCIPLES

- The Silicon Electron Multiplier (SiEM) is a novel sensor concept NIM A 1041 [2022] 167325.
- Internal gain and fine pitch --> excellent time and spatial resolution.
- Divided in two regions: 1. conversion and drift layer, 2. amplification layer.
- Gain mechanism --> impact ionization applying a ΔV in embedded electrodes deposited in a trench, surrounding a Si pillar.
- No gain-layer deactivation is expected with radiation damage, expected to withstand fluencies up to 10^{16} neq/cm^2.
- **Potential for small pixel size, multiplication not affected by radiation and 100% fill factor --> promising for future colliders.**







GOALS

- **Identify a suitable production process for the demonstrators, can it be manufactured?**
  - DRIE based process is the best candidate
- **Demonstrate that it is possible to achieve high electric field in the pillar.**
- **Demonstrate that is possible to achieve charge multiplication.**

TEAM

- **CERN**
  - Victor Coco [coordination]
  - Federico De Benedetti [PhD 25% AIDAInnova], Marius Halvorsen [PhD ended Dec 2023]
  - Edgar Lemos [fellow - support]
  - Morag Williams [fellow - support]

- **CNM**
  - Giulio Pellegrini [coordination]
  - Ivan Lopez Paz [postdoc] started in July 2022 for 2 years 100% AIDAinnova
  - Gemma Rius [researcher]
  - Technical and executive support from the Clean Room staff (DRIE expert etc…)

Collaboration with PSI + Nikhef teams beyond the AIDAInnova project

Centro Nacional de Microelectrónica IMB

PLANNING TOWARDS DEMONSTRATOR

[1] Definition of design rules:

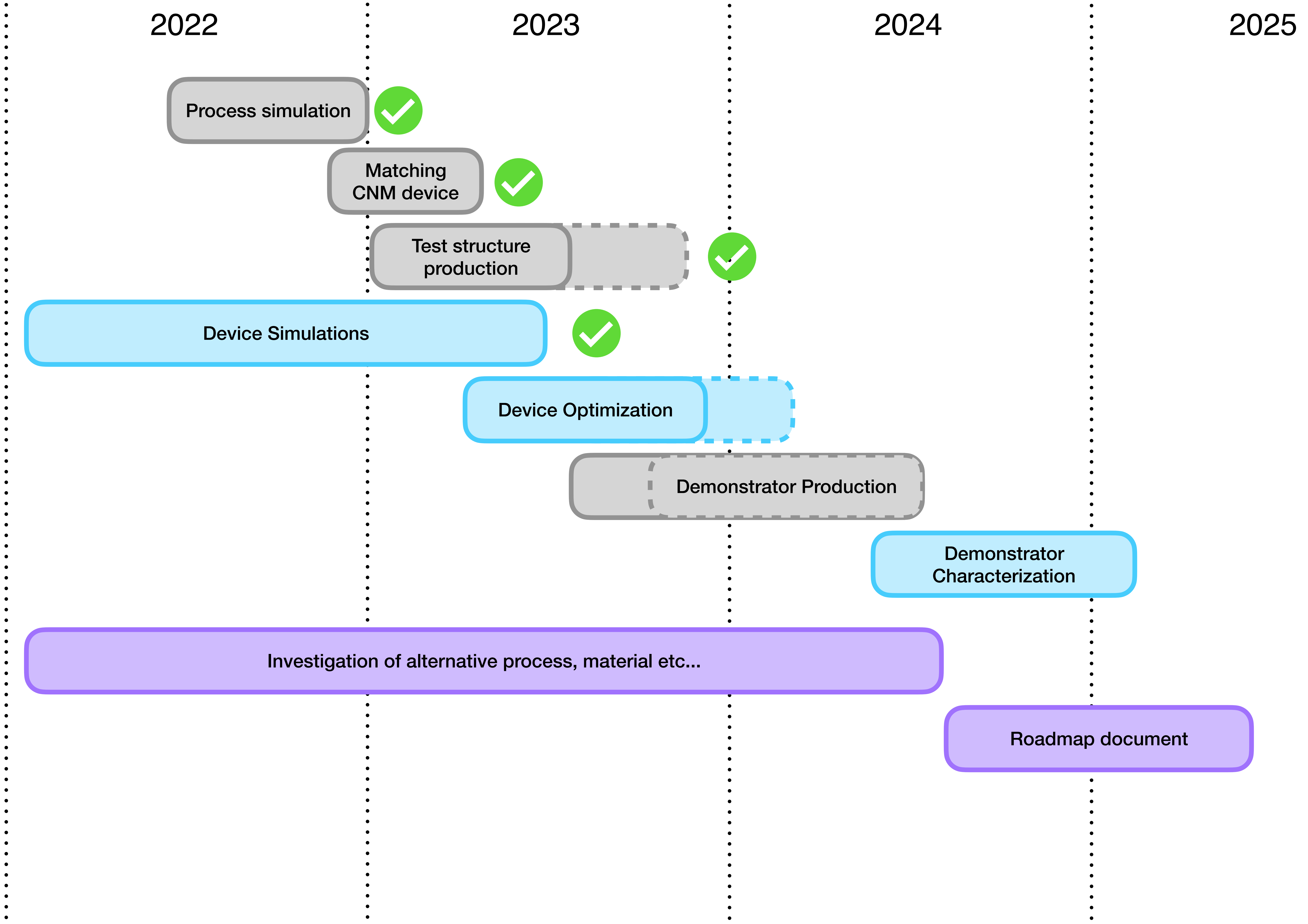
[2] Demonstrator design:

[3] Demonstrator production:

[4] Demonstrator characterization:

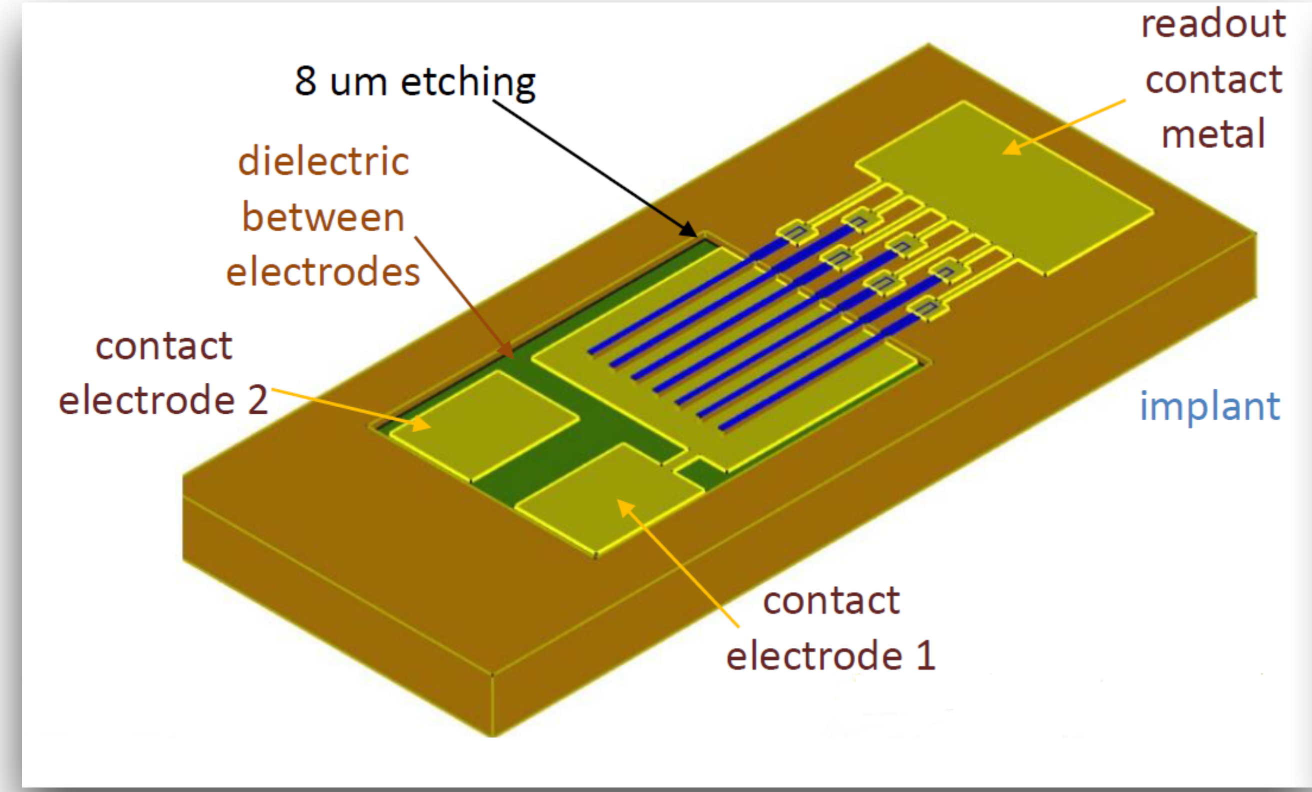
[5] Advanced technologies investigation:

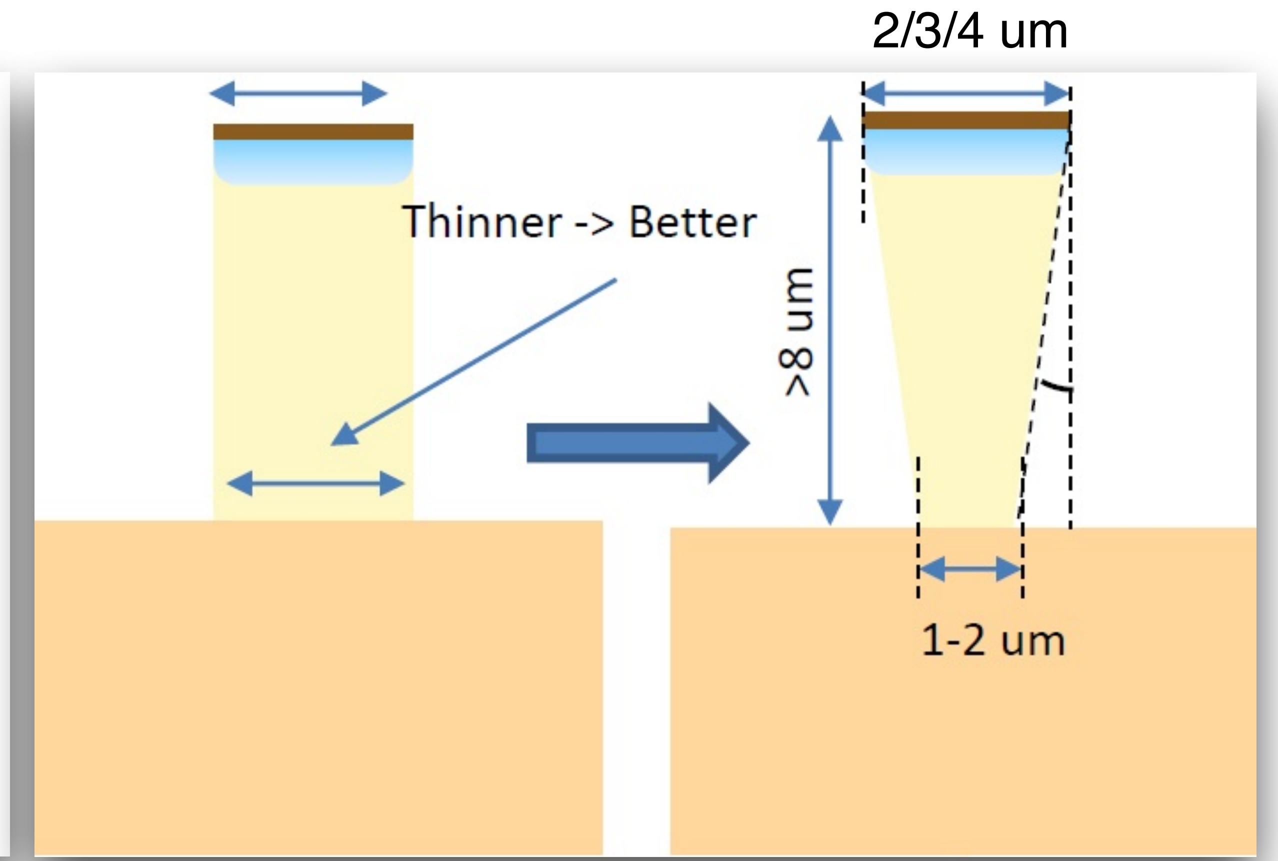
[6] Roadmap document:

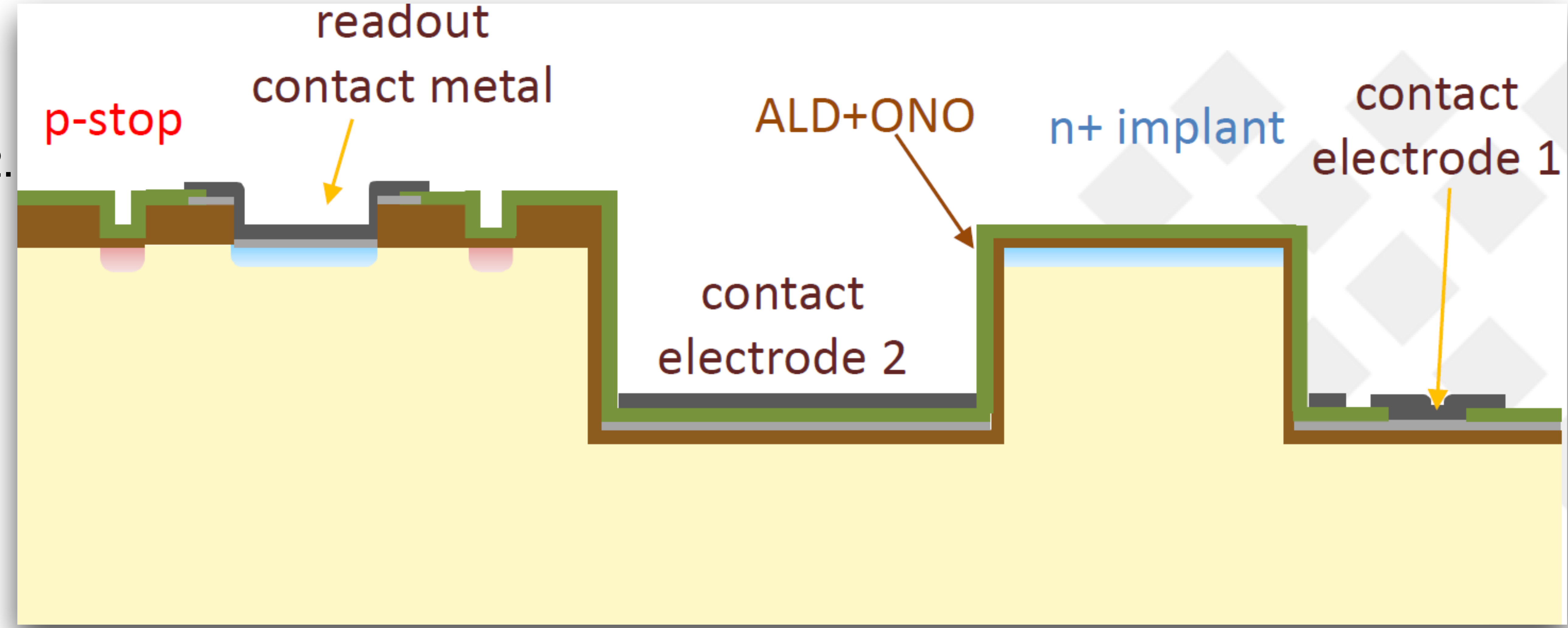


DRIE DEMONSTRATOR

- **Demonstrator as a PoC manufactured by CNM.**
  - Strip with two embedded electrodes design, wire bond pads connects strips in parallel.
- **Trenches:**
  - Si trenches etched (DRIE).
- **Electrode deposition:**
  - ALD 50 nm HfO_2, metal deposition, ALD 50 nm HfO_2, SiO_2 deposition, electrode 2.
- **Challenges:**
  - Oxide layer can induce stress, limiting the gap between electrode 1 and 2.
  - Etching limited in width depending on patterning process used:
    - Laser photolithography down to 2 um.
      - Fast prototyping and good flexibility.
      - *Require pyramidal profile to achieve best multiplication performance.*
    - Electron beam lithography (adjustment needed).

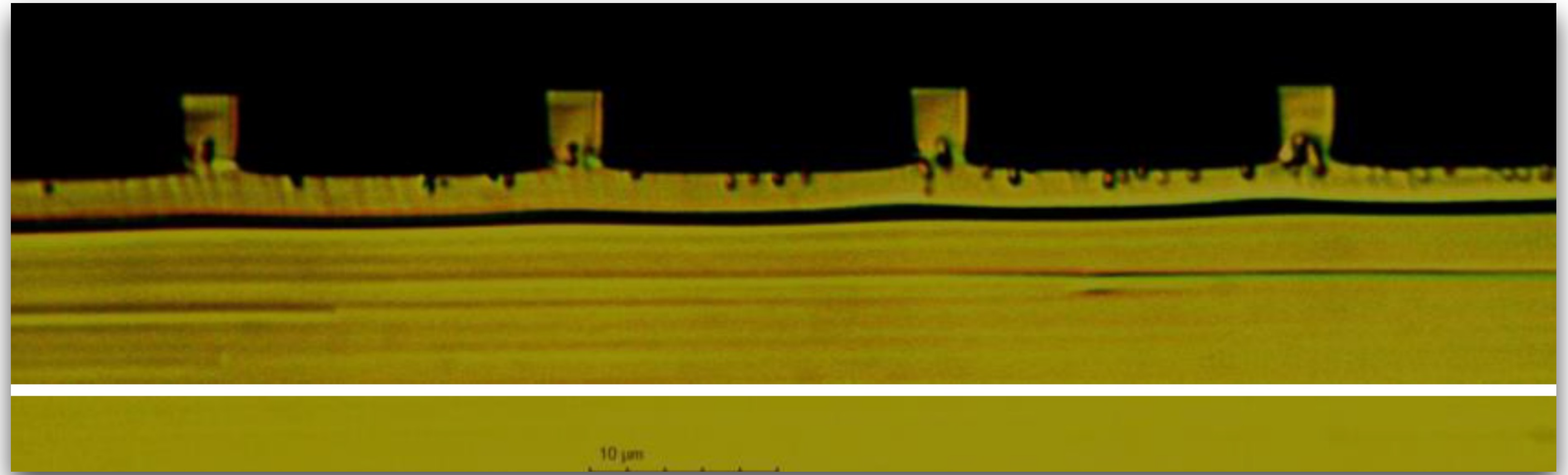


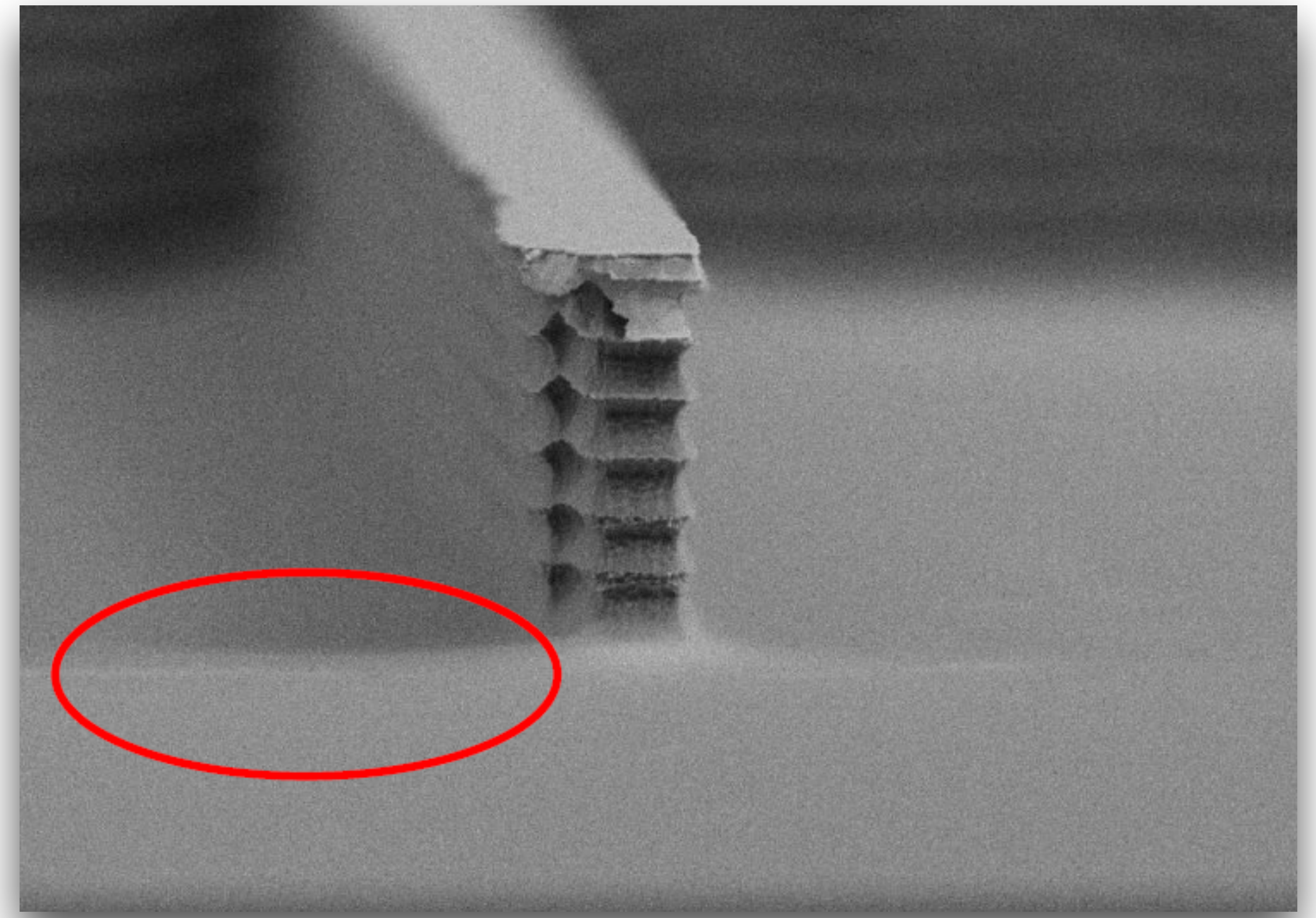


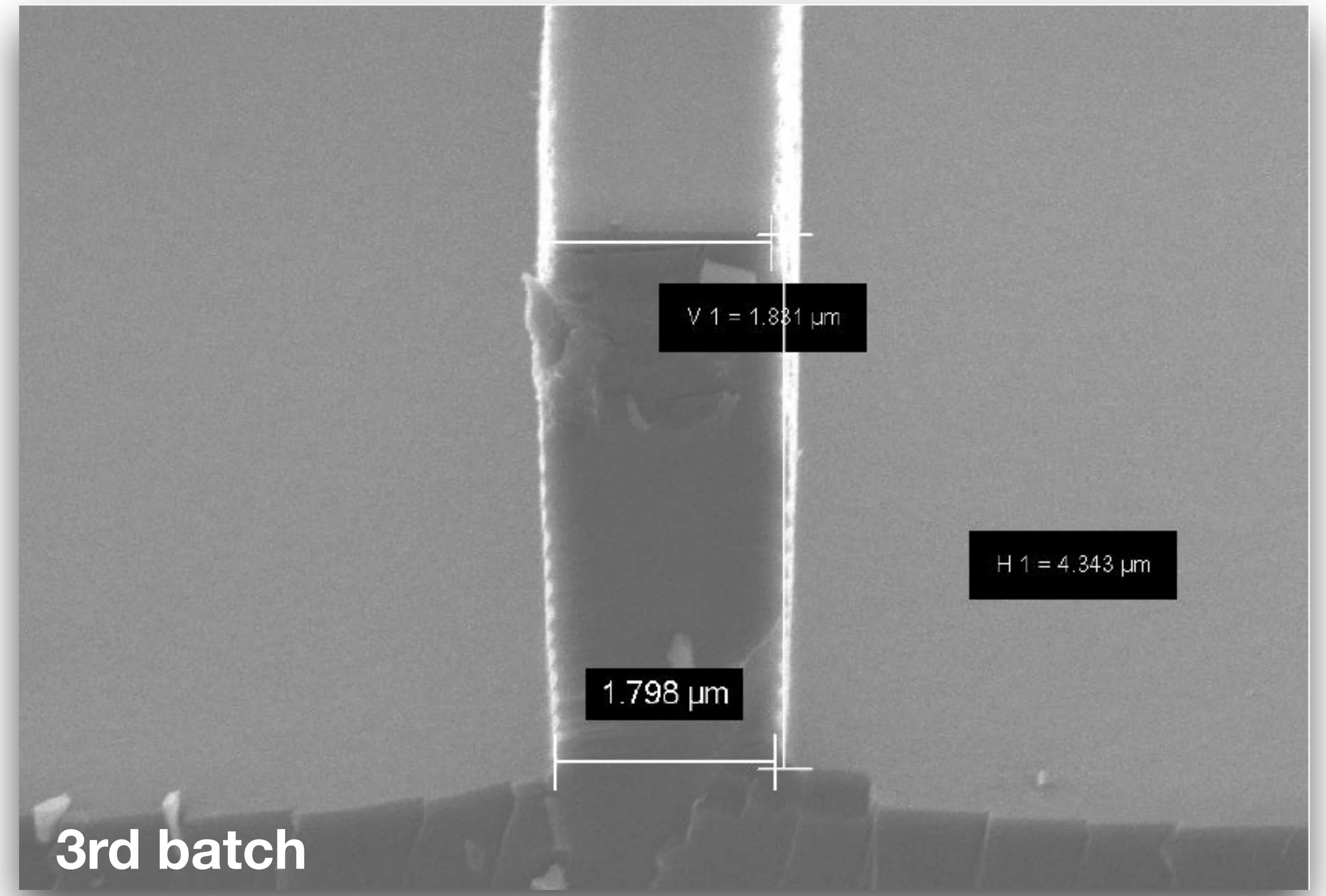


DRIE ITERATIONS

- **1st batch over etched:**
  - Trench 25 um instead of 8 um.
- **2nd batch improved etching:**
  - Two process tested:
    - With few long etching steps, walls too scalloped.
    - Smooth walls but no pyramidal shape.
  - Test B: 9 um, test C: 8.41 um.
  - Pillars thinner than nominal 1.7 um, some were broken.
- **3rd batch closer to specs:**
  - Pyramidal shape achieved but rough walls.
  - Slightly over etched due to thin photoresist (unexpected).
  - Curved profile at the pillar base due to etching.
- **Recipes closer to the goal profile:**
  - May require minor adjustments.
  - Some curved profile in the base from etching process.
  - Goal is to achieve 2/3/4um on top and 1um on bottom.



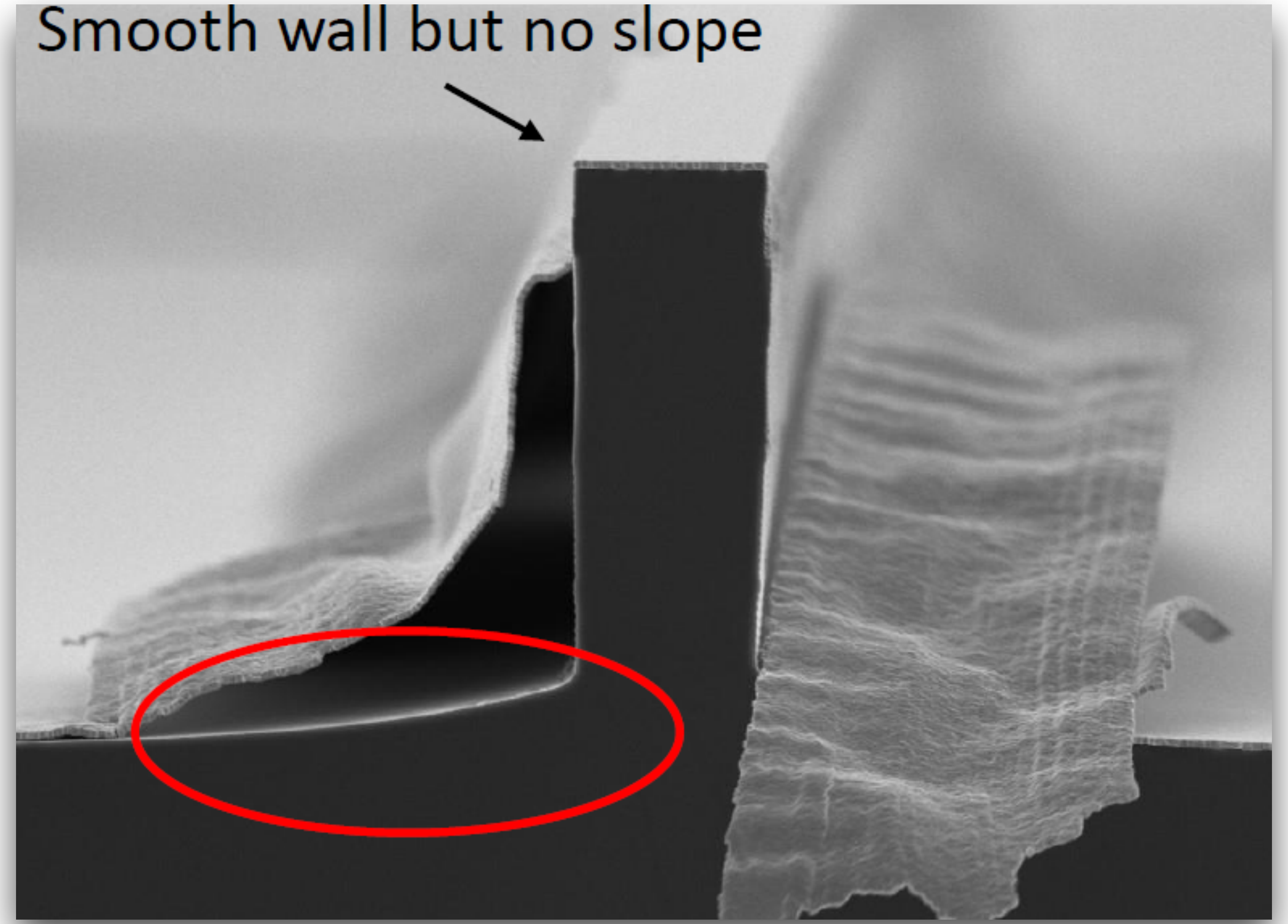


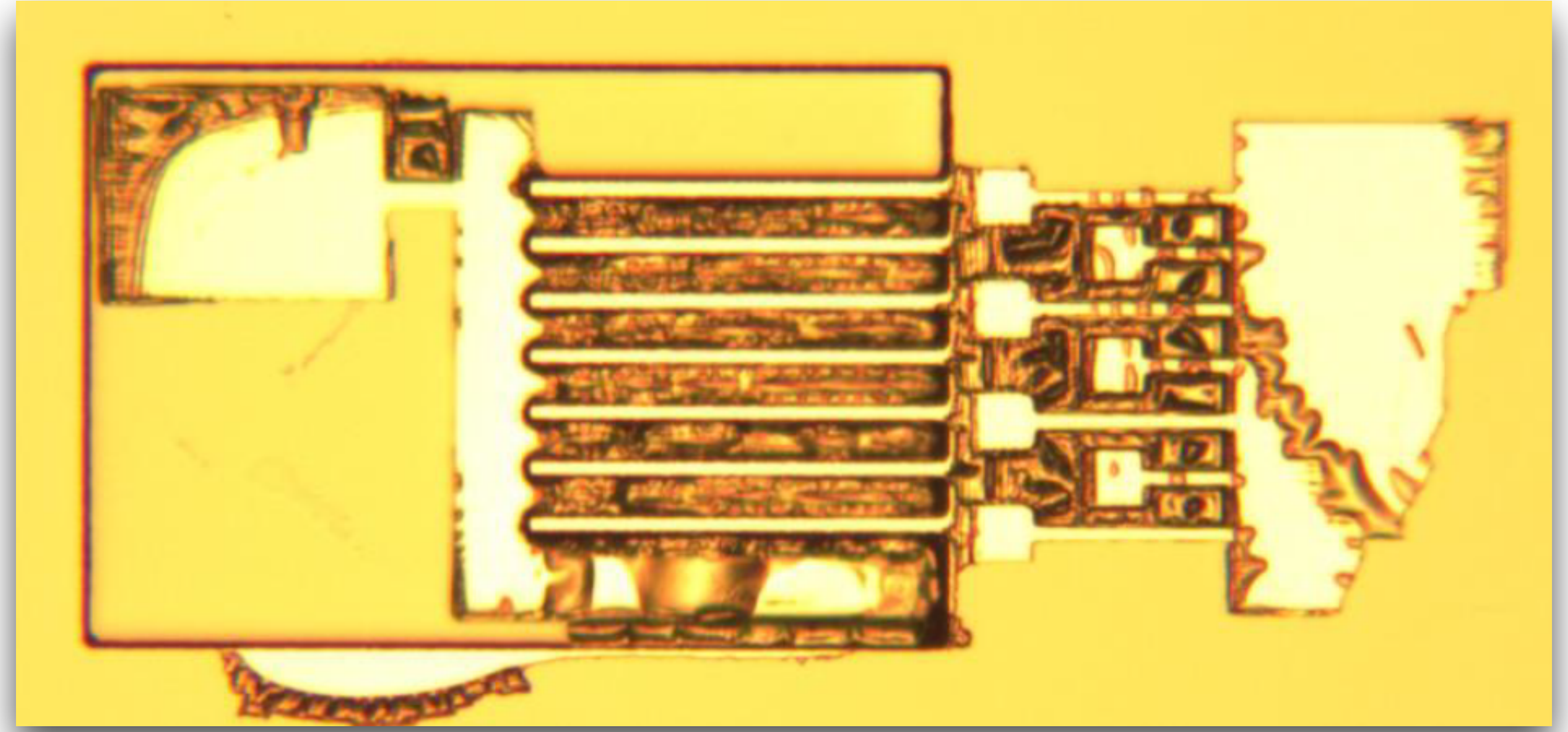


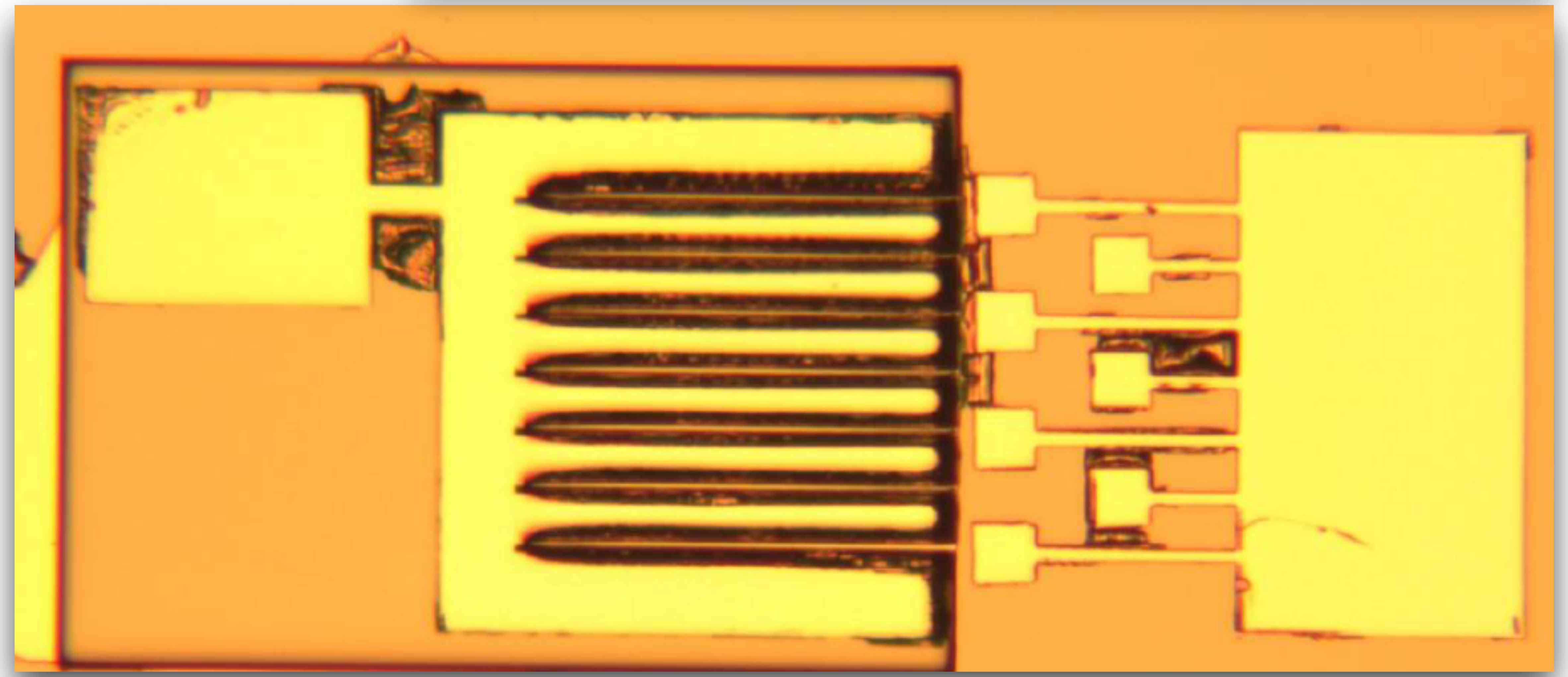
TEST OF METAL DEPOSITION

- First metal electrode planned to be W sputtered at 100 nm (W evaporation not available), then lift-off.
- Using W allow to obtain higher SiO2 thinkness between electrode 1 and 2 --> better for multiplication
- Areas of the deposited metal are “lifted", some others seem better.

- **Switching to evaporation of Al for metal contacts.**
    - Solve the metal "lift" problem but results in lower oxide thickness

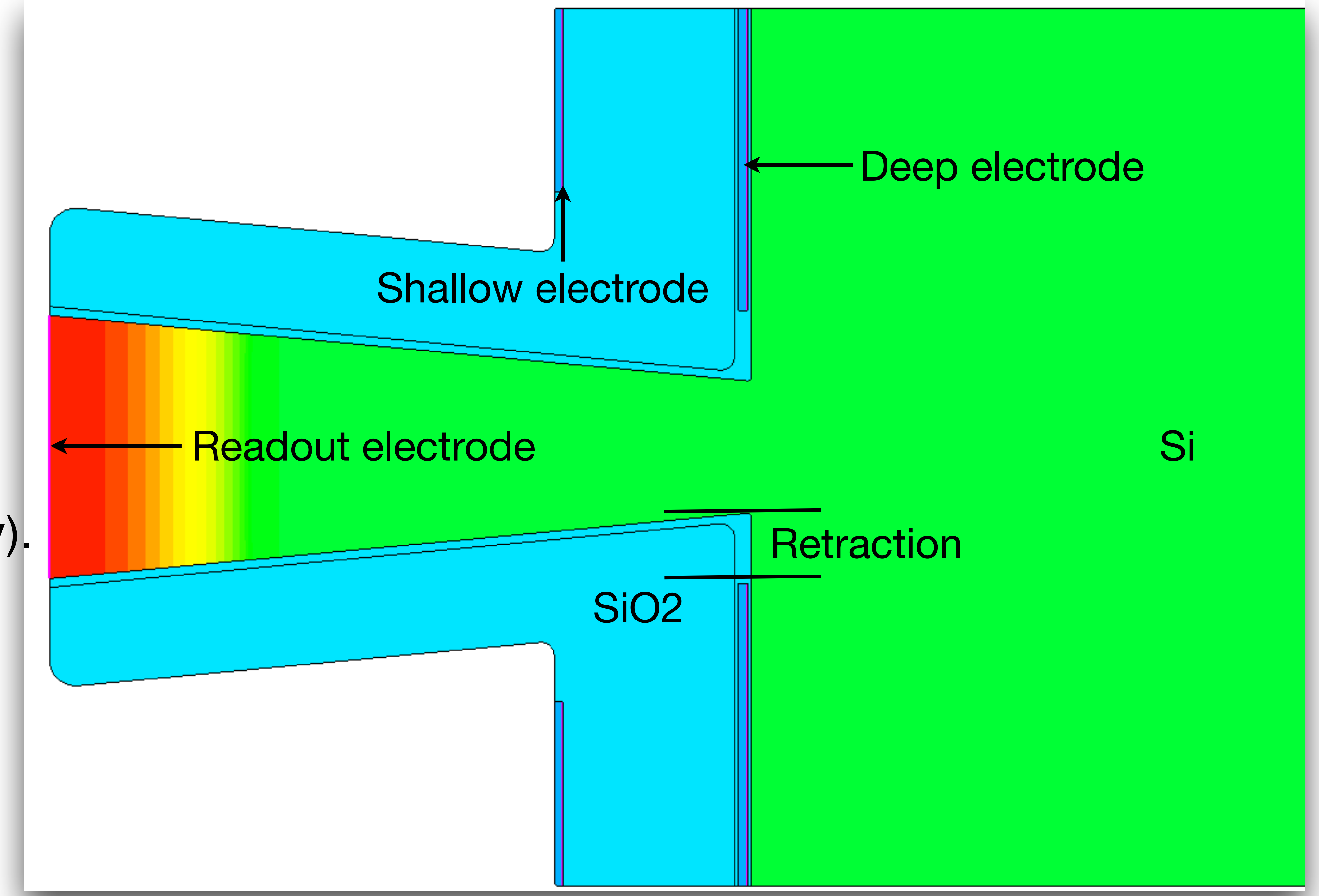


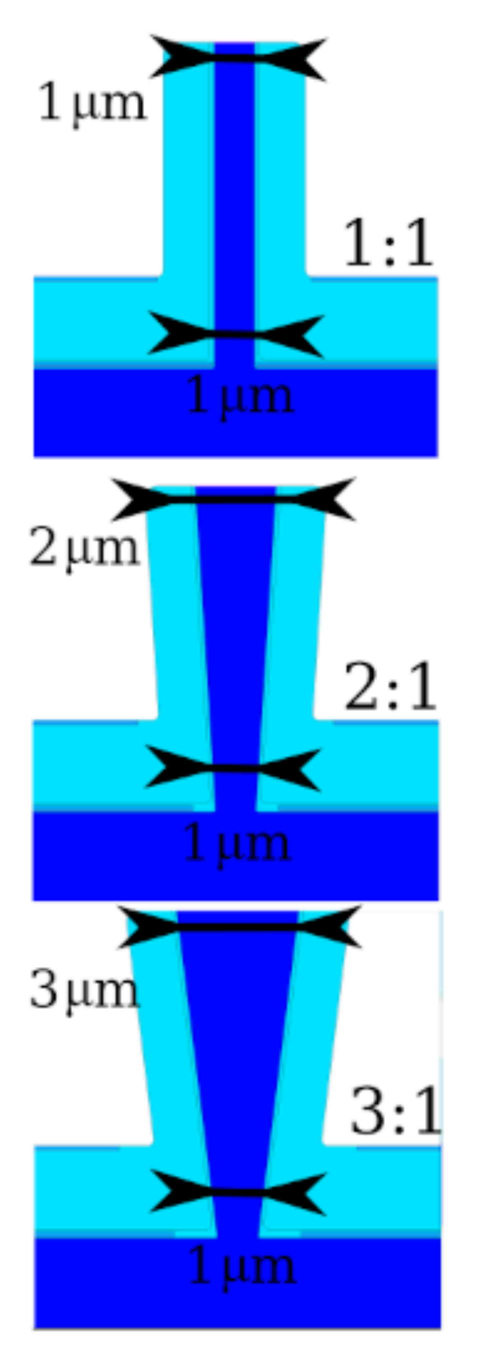




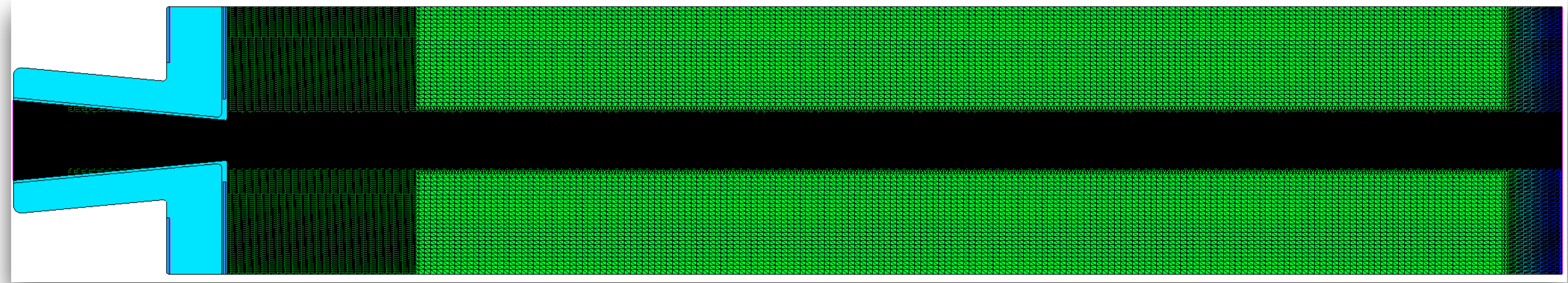
SIMULATIONS OF NEW GEOMETRIES

- **Simulations:**
  - Simulations on first 1:1 um geometry have been performed
    NIM A 1041 [2022] 167325
  - Need to adapt the geometry to the CNM process.
  - Extracted gain and IVs.
  - SiO2 thickness, ΔV between electrodes pillar width impact the gain.
- **Geometry:**
  - Pillar slant introduced to match CNM process (laser photolithography).
  - Parametrized to study different pillar walls configuration.
  - Rounded corners to mimic etching process at CNM.
- **Mesh:**
  - Moved to snmesh to have better control of interface areas.
  - Improved MIP region for transient simulations.
  - Convergence studies ongoing for HfO2 ALD layer.





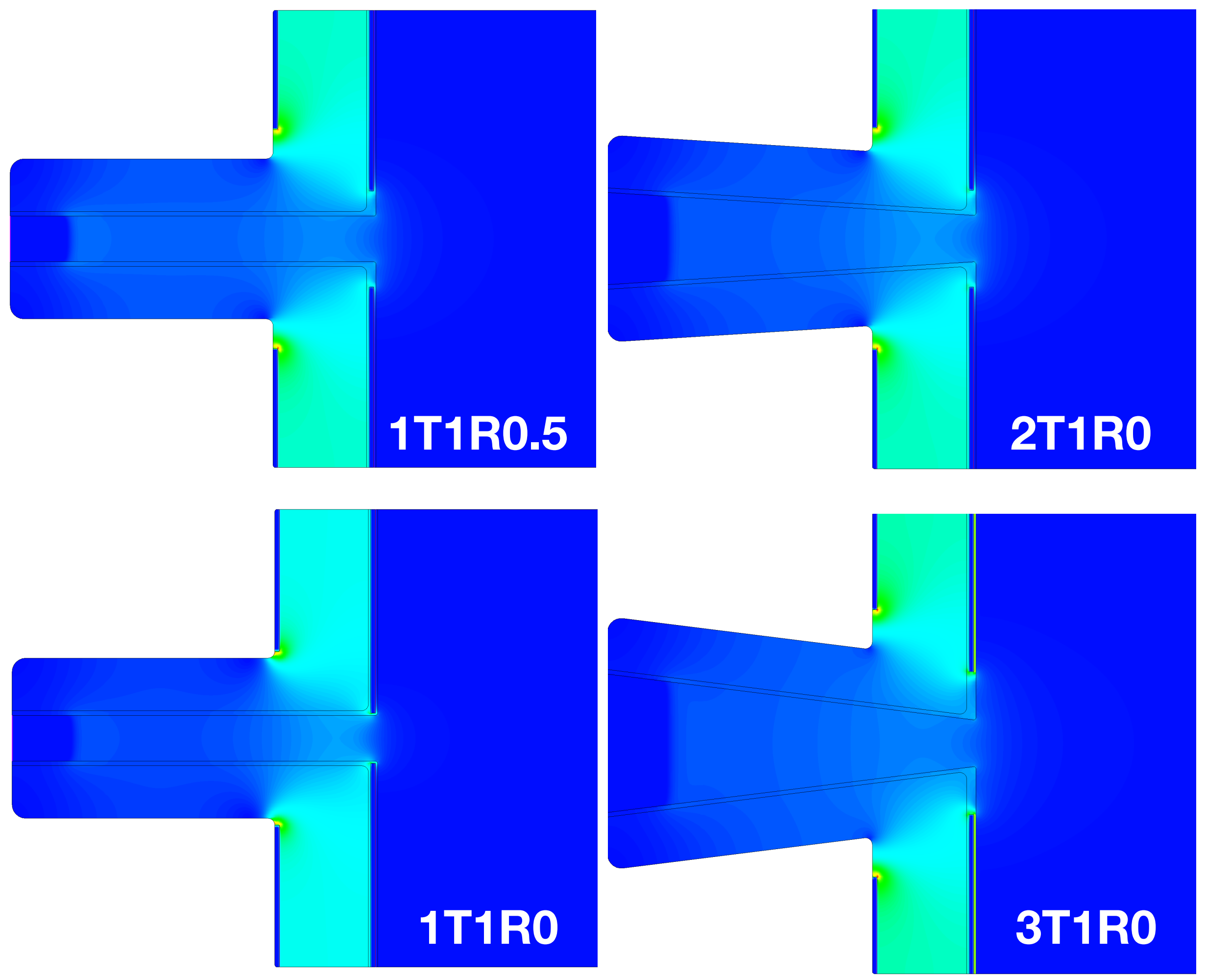
Top/Bottom	1 [um]	1.5 [um]	2 [um]	2.5 [um]	3 [um]
3 [um]					
2 [um]					
1 [um]					

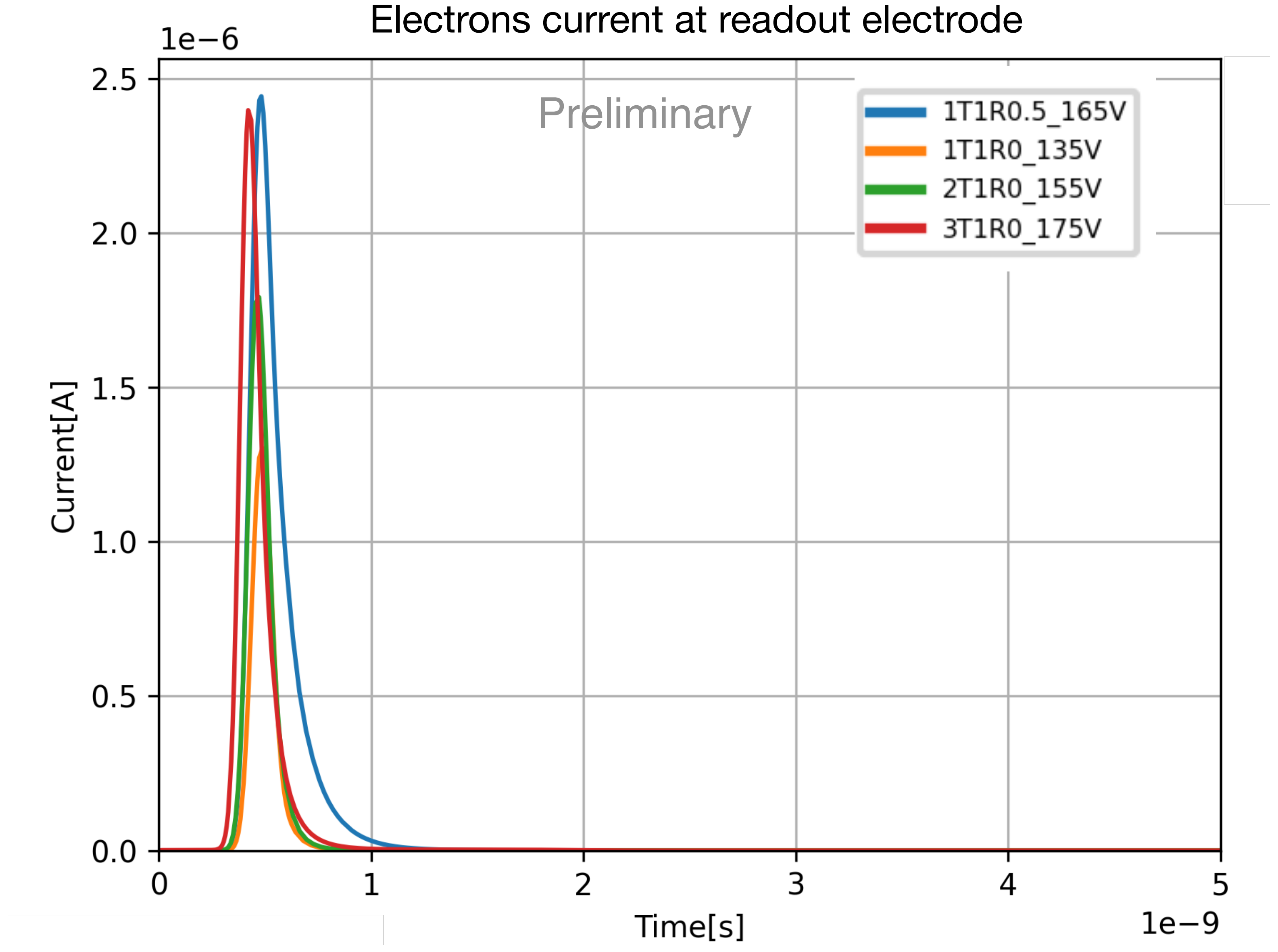


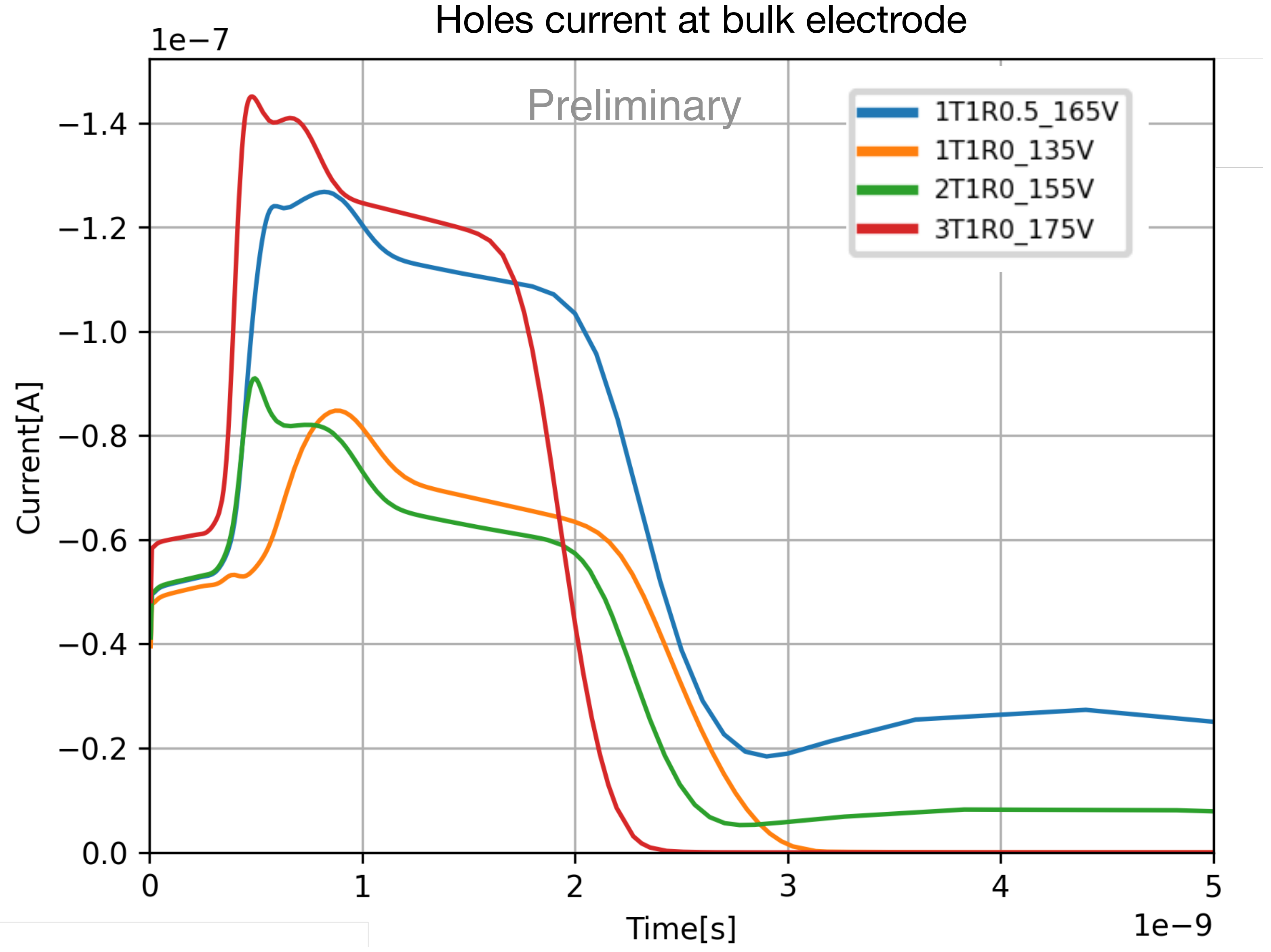
SIMULATIONS OF NEW GEOMETRIES

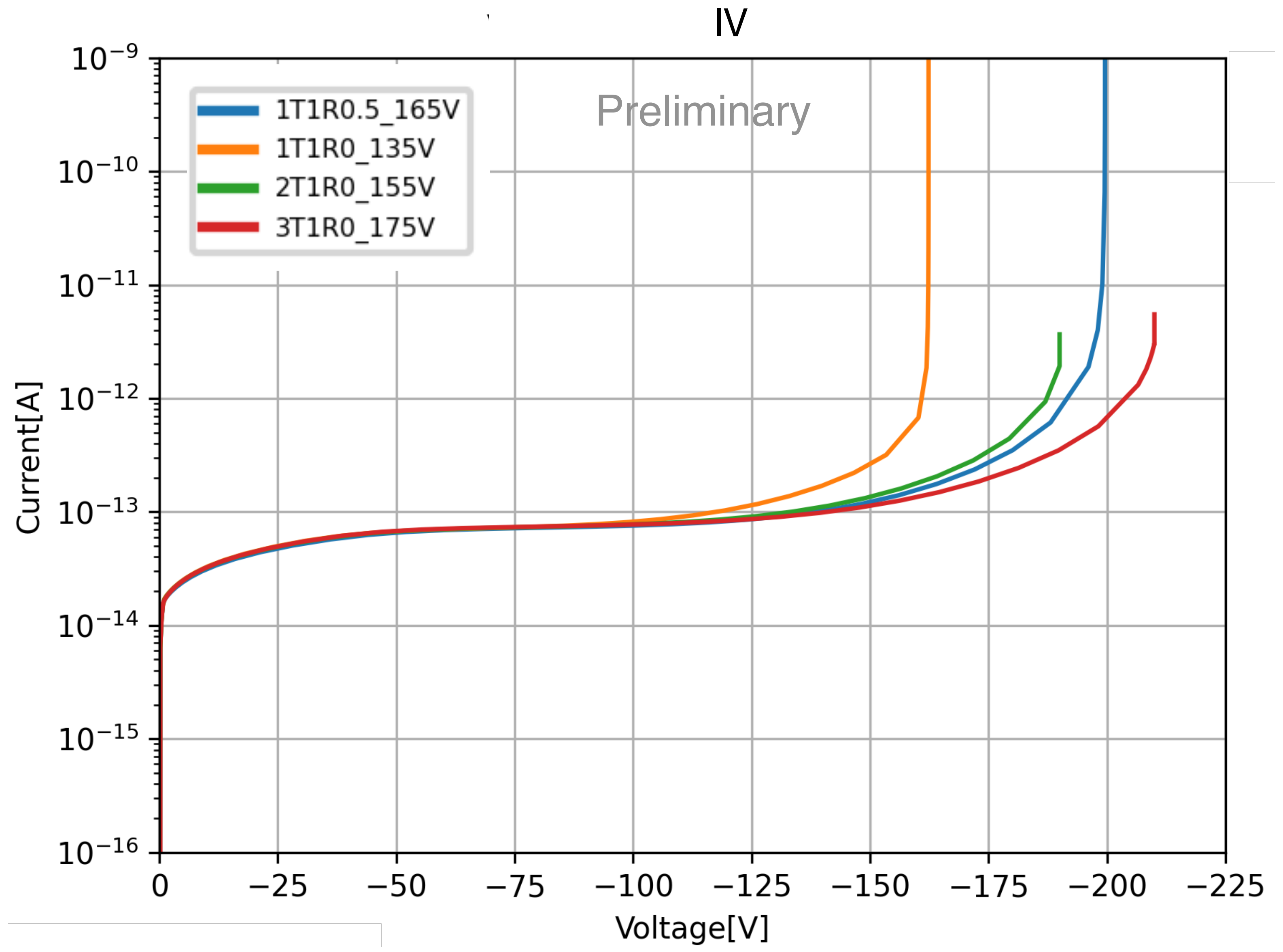
- Electrode 2 is aligned with the top of the pillar (due to fabrication process).
- High angles increase the distance of deep electrode from pillar base.
  - Higher voltages can be reached but breakdown occurs from pillar walls.
- Performance modification in slanted geometry largely due to retraction of the electrodes.
- Best configuration is where the pillar base is small and the slant angle is small.

Electric Field Map

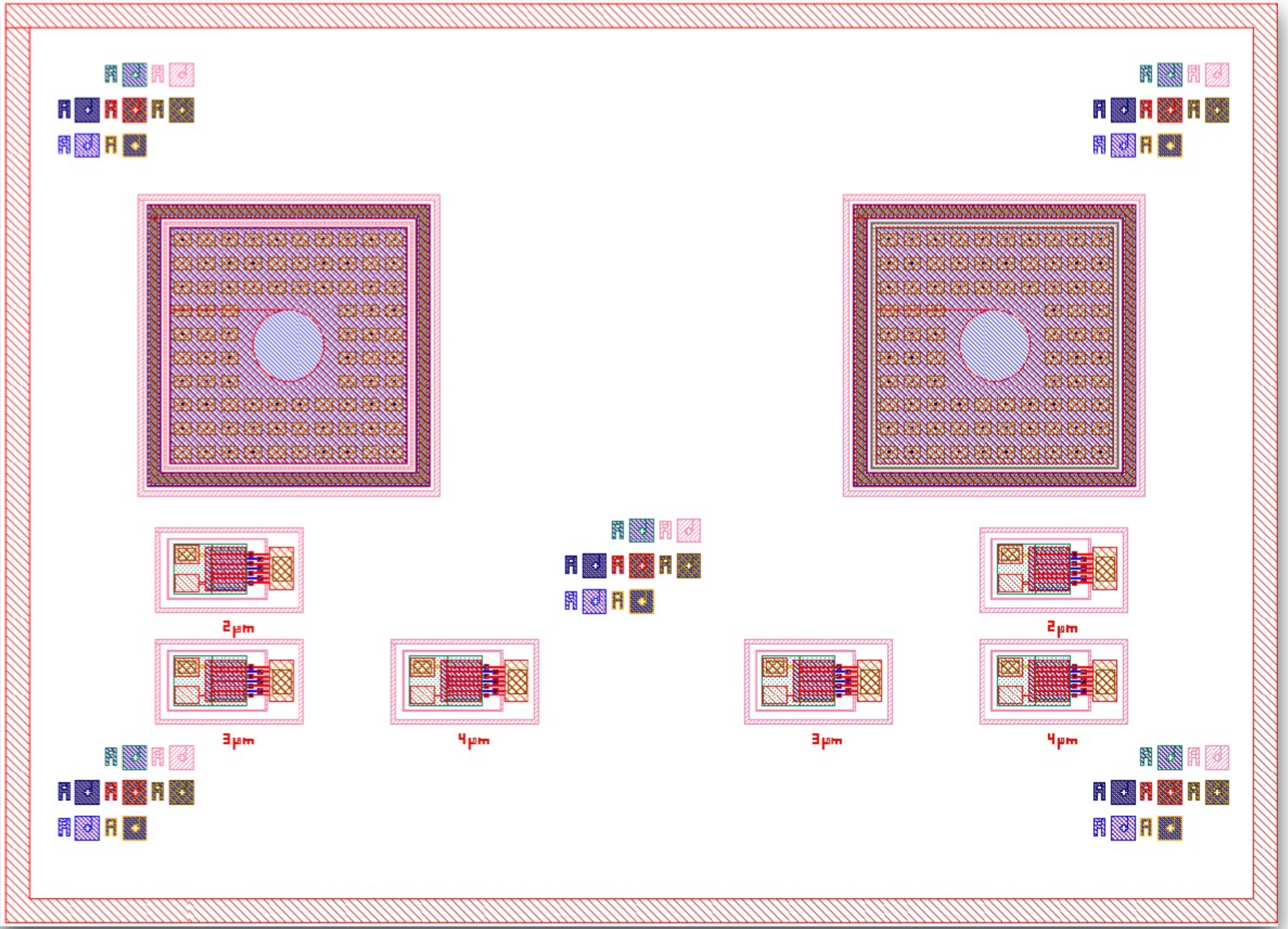








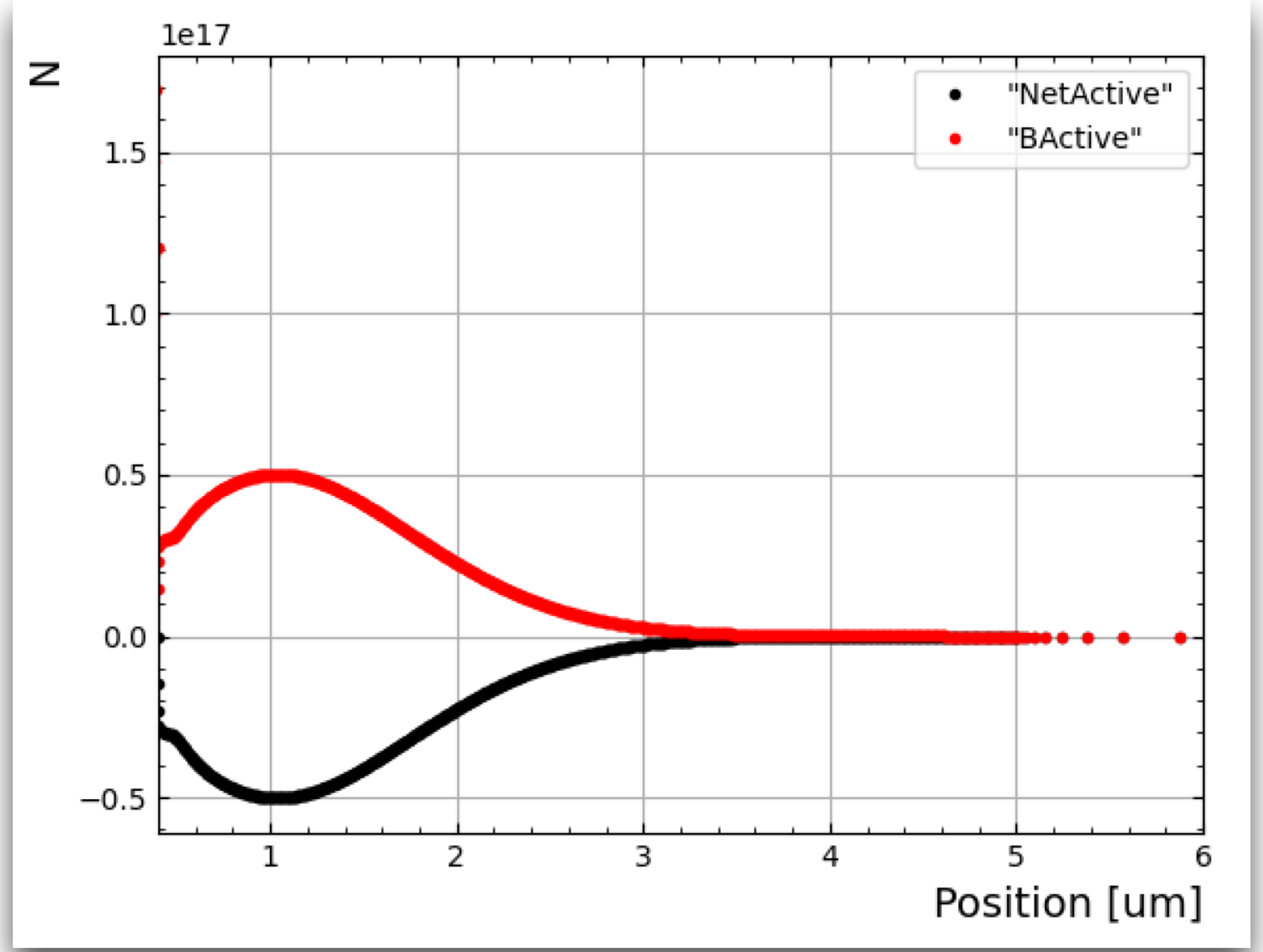
PRODUCTION WAFER LAYOUT



- 3 SiSi quarter wafers 50um p-type.
- Test structures:
  - 1x1 mm regular diode.
  - 1x1 mm diode with trench.
- SiEM inverted pyramids samples:
  - 2 um (x2).
  - 3 um (x2).
  - 4 um (x2).
- After first metallization 1 sample removed and electrically tested at CNM.

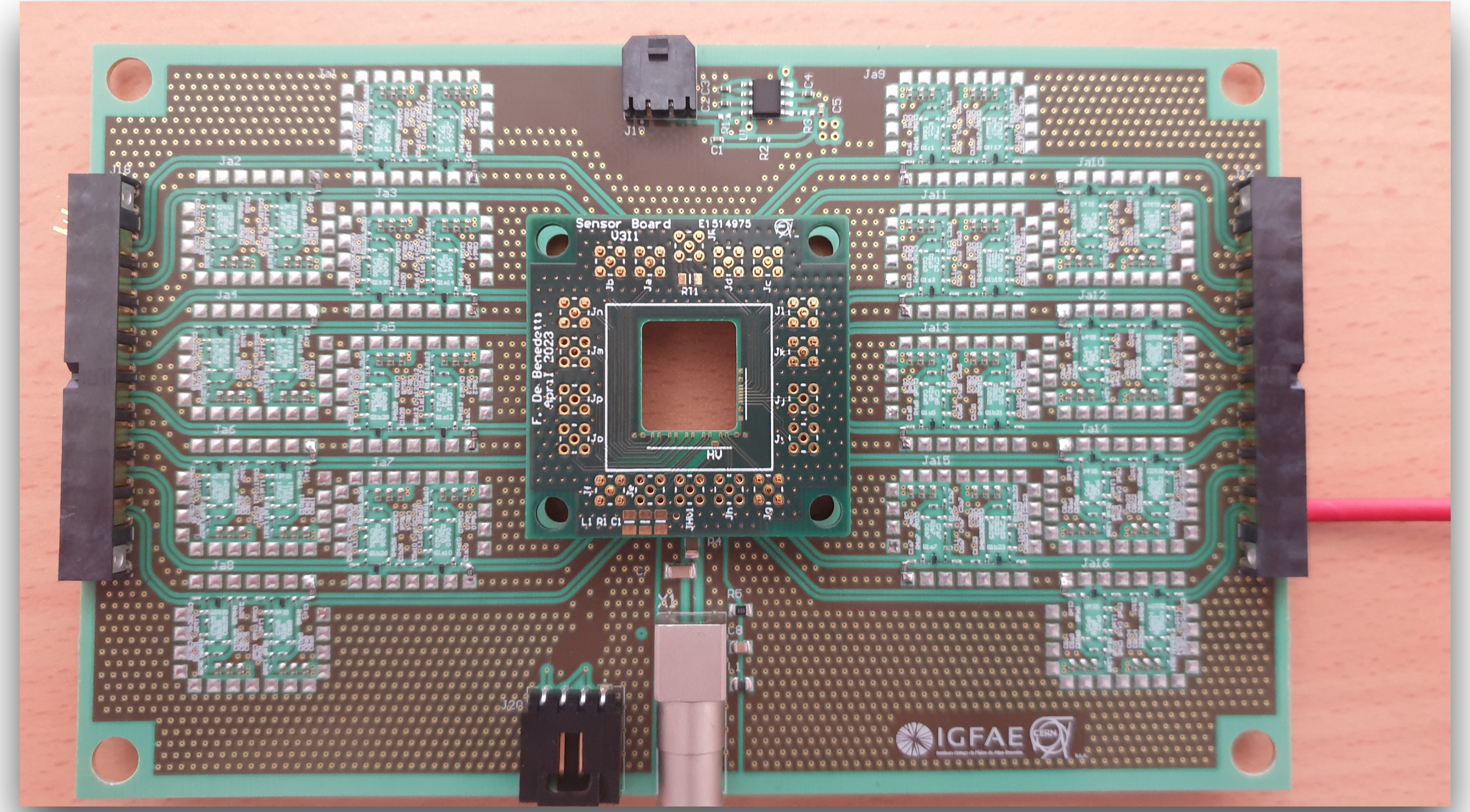
CNM PRODUCTION CRITICAL STEPS

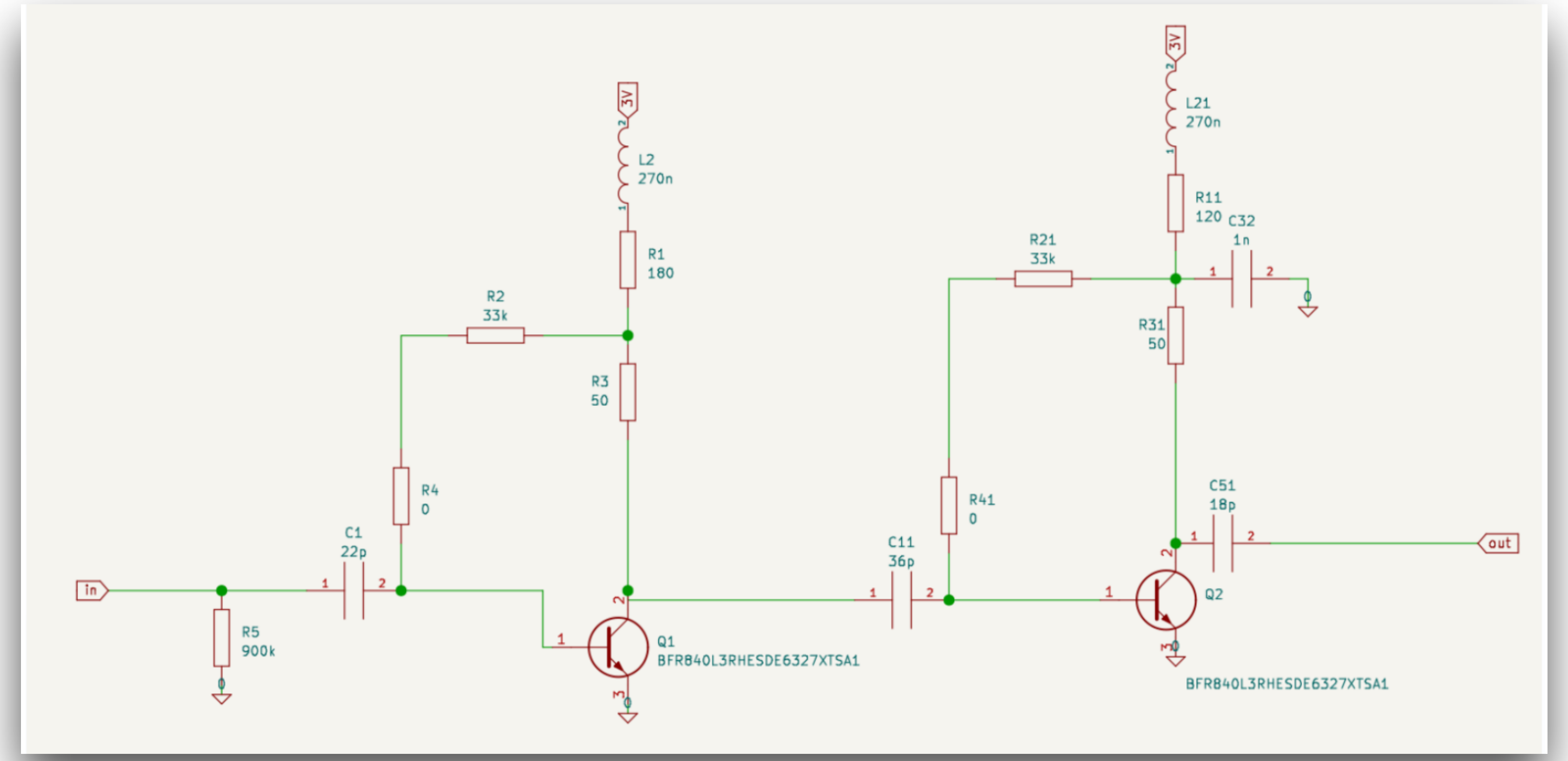
- **P stop/N+ implants:**
  - Simulation of fabrication process to control p stop => **Done, looks good.**
  - Asses electrical characteristics of p stop and pn junction after first metallization with 1x1mm2 diode in chip.
- **Trenches:**
  - Final etching test, before RIE in production run => **Done.**
- **Photolithographies post RIE:**
  - Contact with clean room photolithography experts to ease the lithographies.
- **Metallizations:**
  - Evaporation of Al instead of W sputtering (no W evaporation available).
  - Changes dielectric to $HfO_2 + SiO_2$ (no need for high T processes).



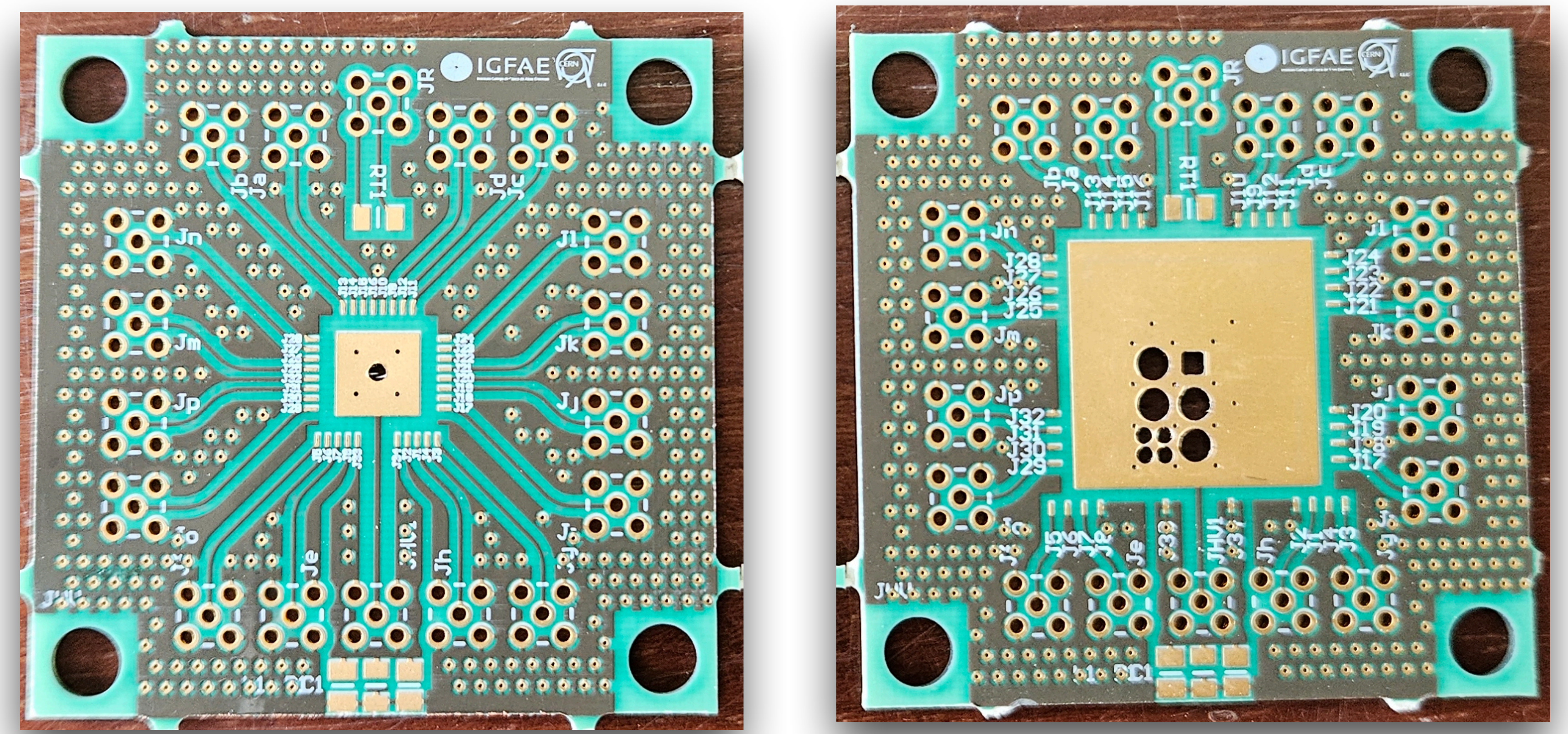
- **16 Channel Readout board:**
  - Designed to be a common platform to test different sensor typologies.
  - Trans-impedance amplifier (gain ~37db) based on two stages RF BJT SiGe.
  - High frequency design up to 12 GHz with Rogers 4350B stack up.
  - Carrier board allow easily to change the DUT.
  - Multiple designs of the carrier board to install different sensor shapes.
  - First tests on V1 performed, V2 manufactured and under test.
- **Laser setup and test beams:**
  - Integration with the TimePix4 telescope mechanics for test beam characterization.
  - Improvements on laser setup are foreseen (optics, X/Y stage, pulser, oscilloscope...).

16 Channel Board V1

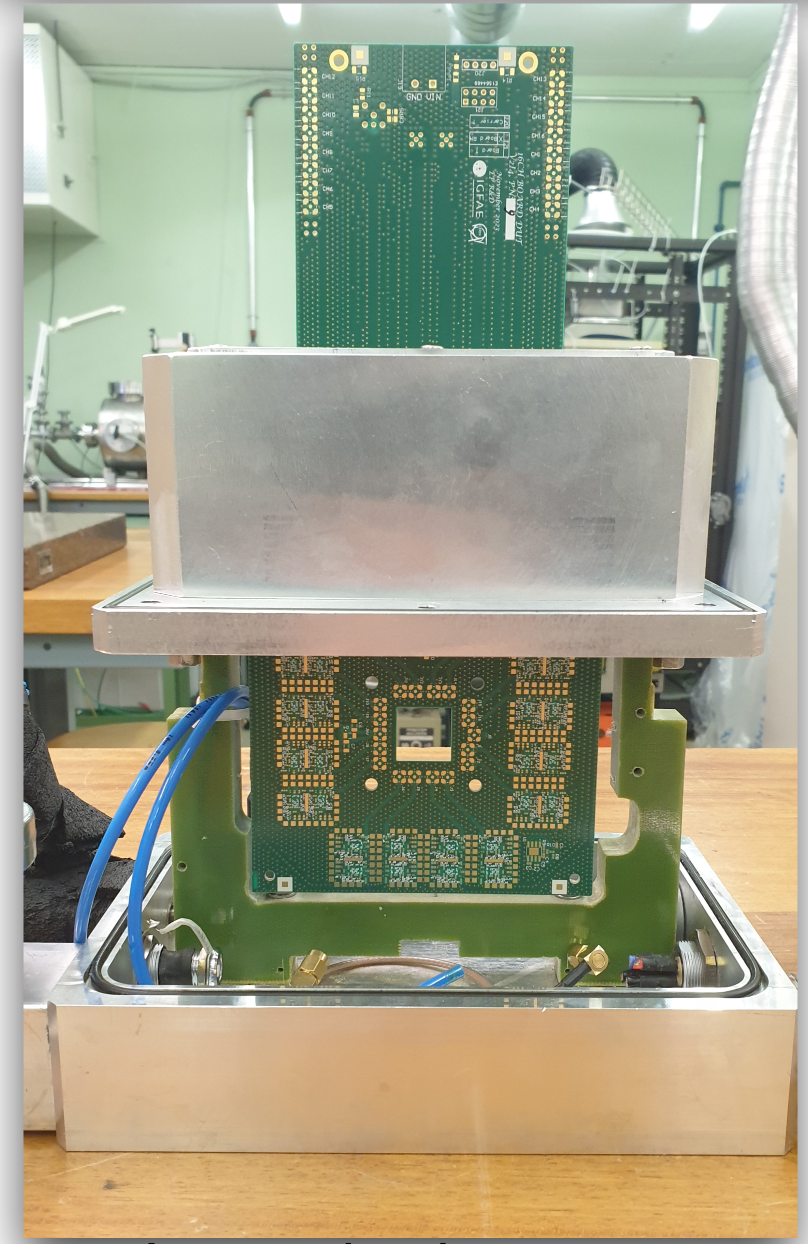




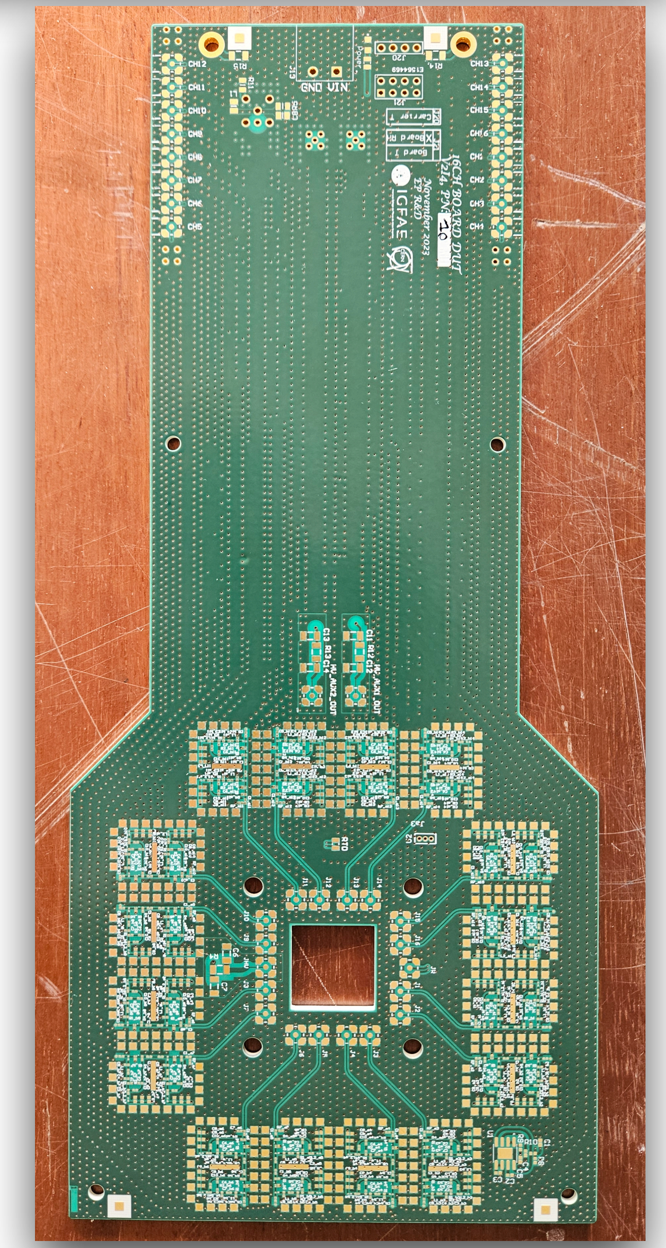
16 Channel board schematic



Two designs of the carrier board



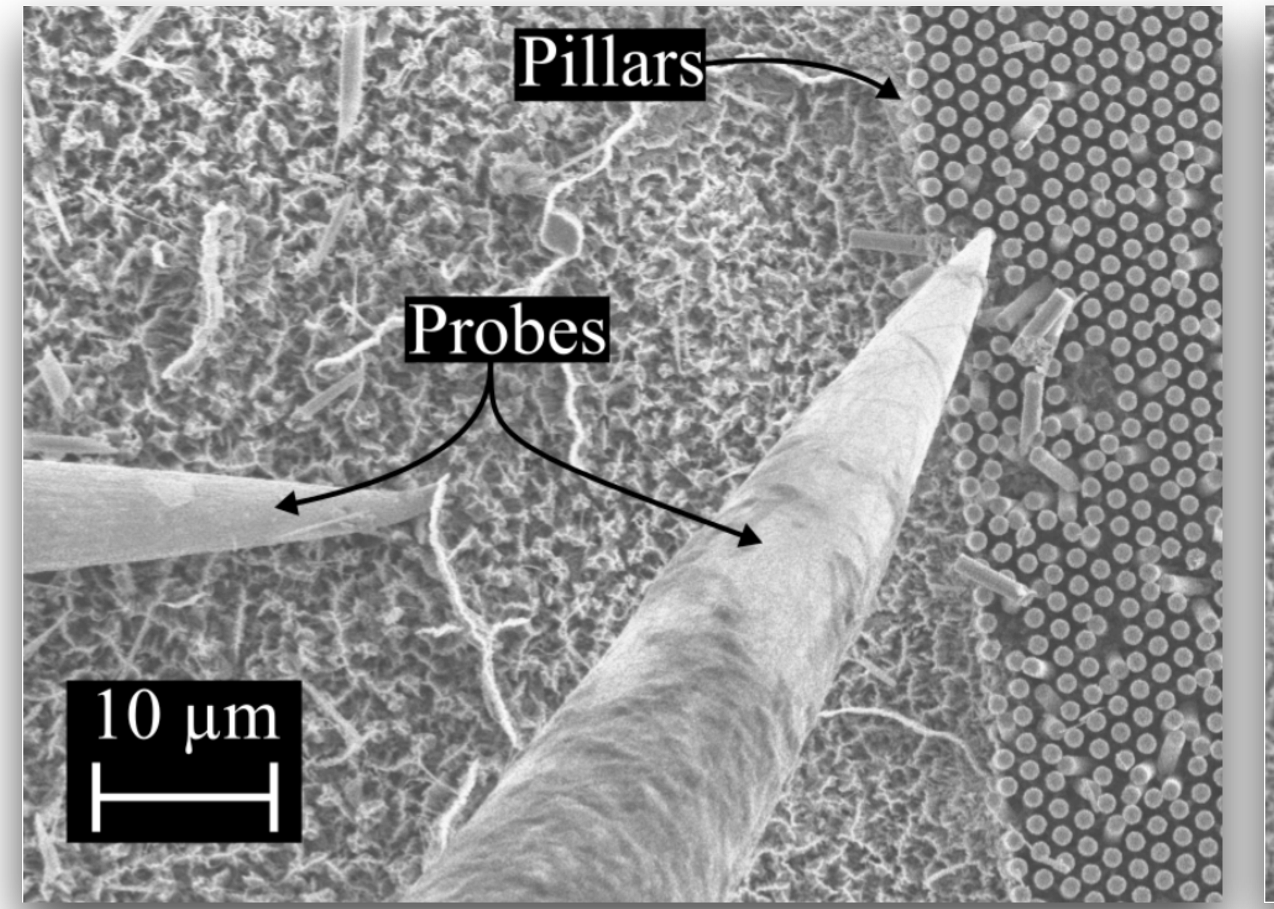
Integration in TimePix4 DUT box

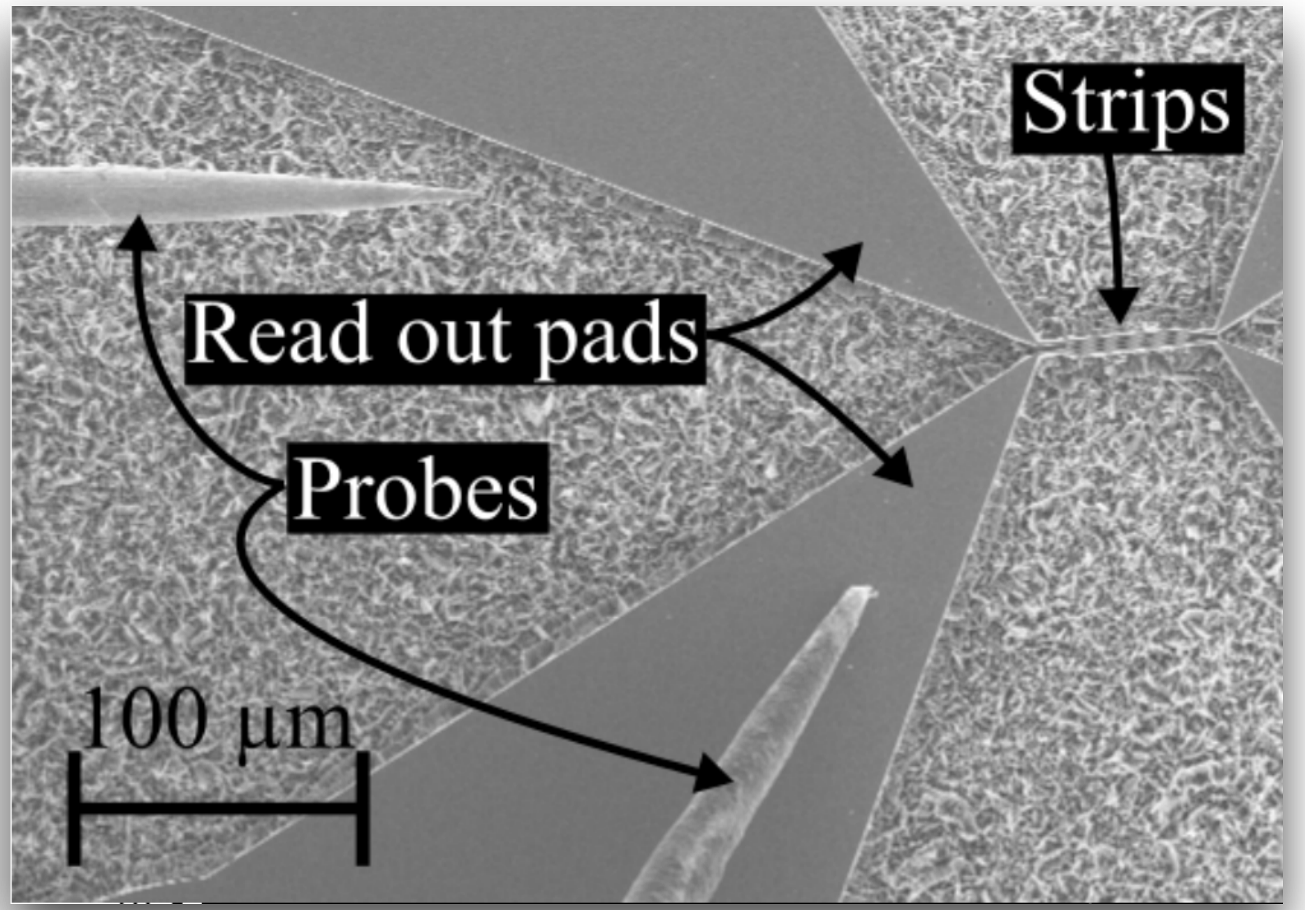


16 Channel Board V2

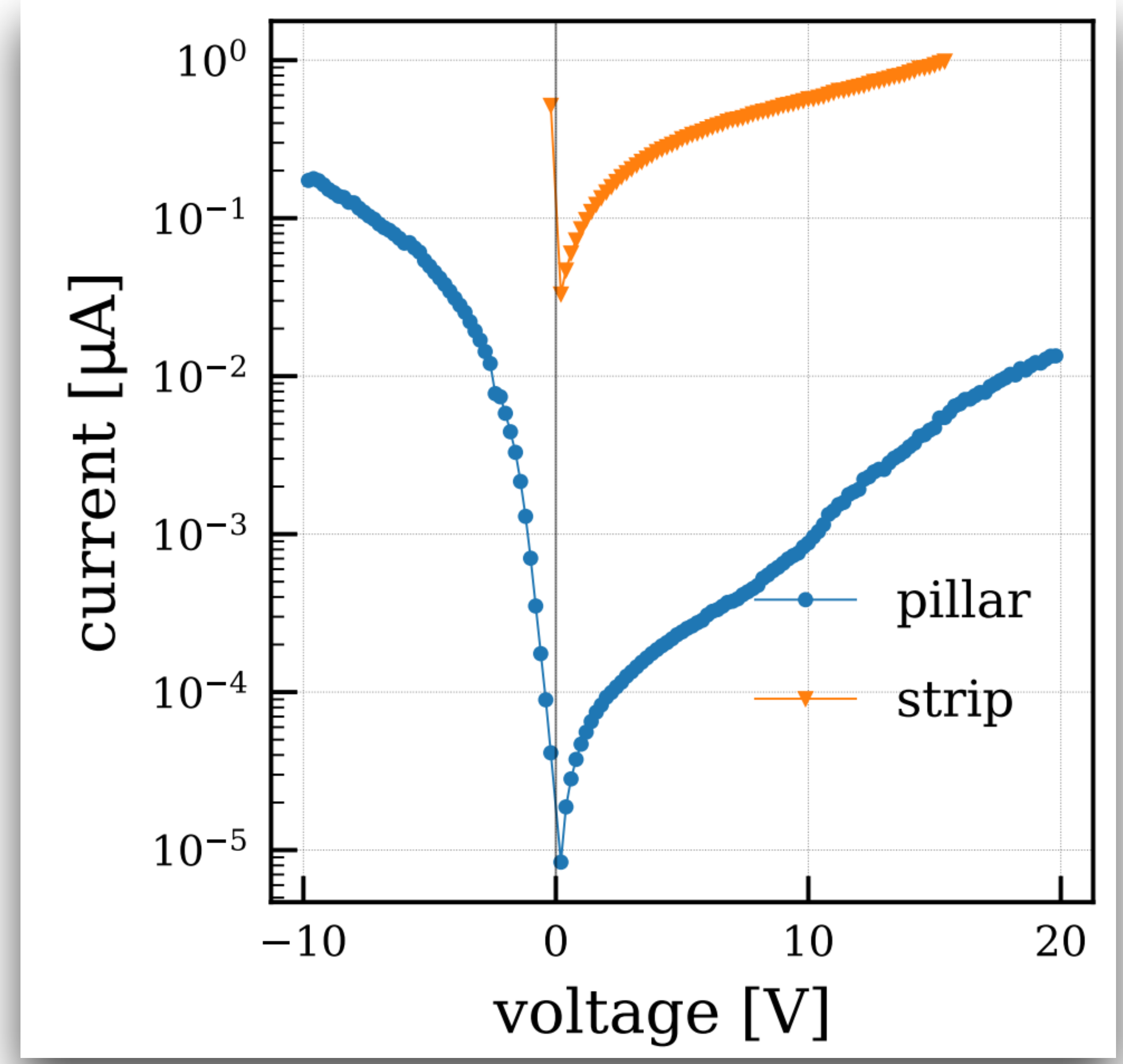
ADVANCED TECHNOLOGIES INVESTIGATION - MACETCH

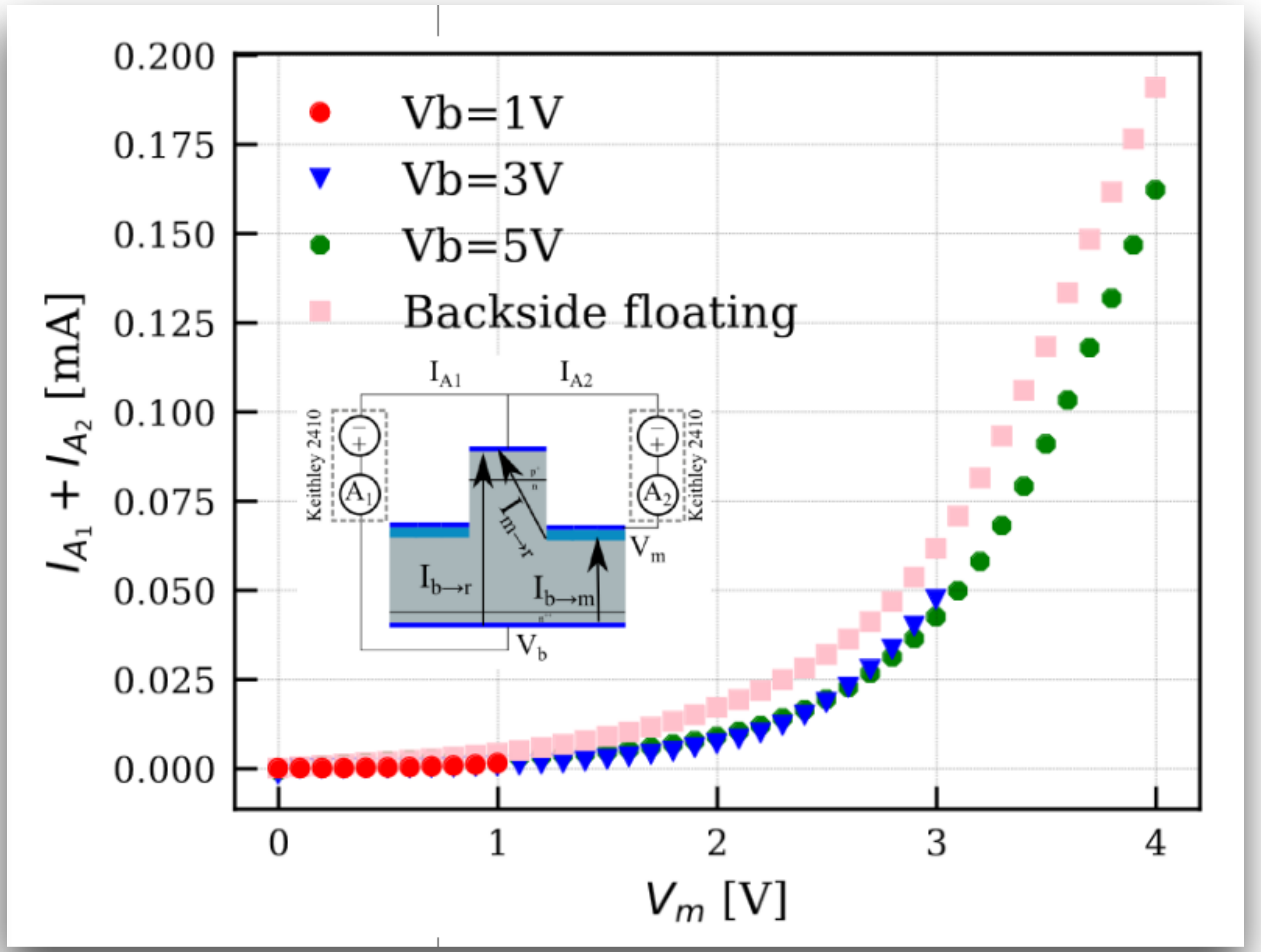
- **Study possible use of Metal assisted etching:**
  - Parallel project between CERN and PSI, based on AdEM 22 (2020) 2000258.
  - Very different process constraints (cheap, high aspect ratio, first electrode deposited while etching).
  - Fast development.
  - Samples manufactured on n on p wafers
  - One gain electrode structure with metal in contact with Si (no SiO2).
  - Strips and pillar geometries.
  - Published NIM A 1060 [2024] 169046





- **Testing the structures:**
  - IV just after production with probe station pn junction conserved.
  - Bonding of test structures to a carrier board.
  - IV done in the lab using 16 Channel board V1 from backside electrode and multiplication electrode.
  - Preparing setup for laser/test beam.

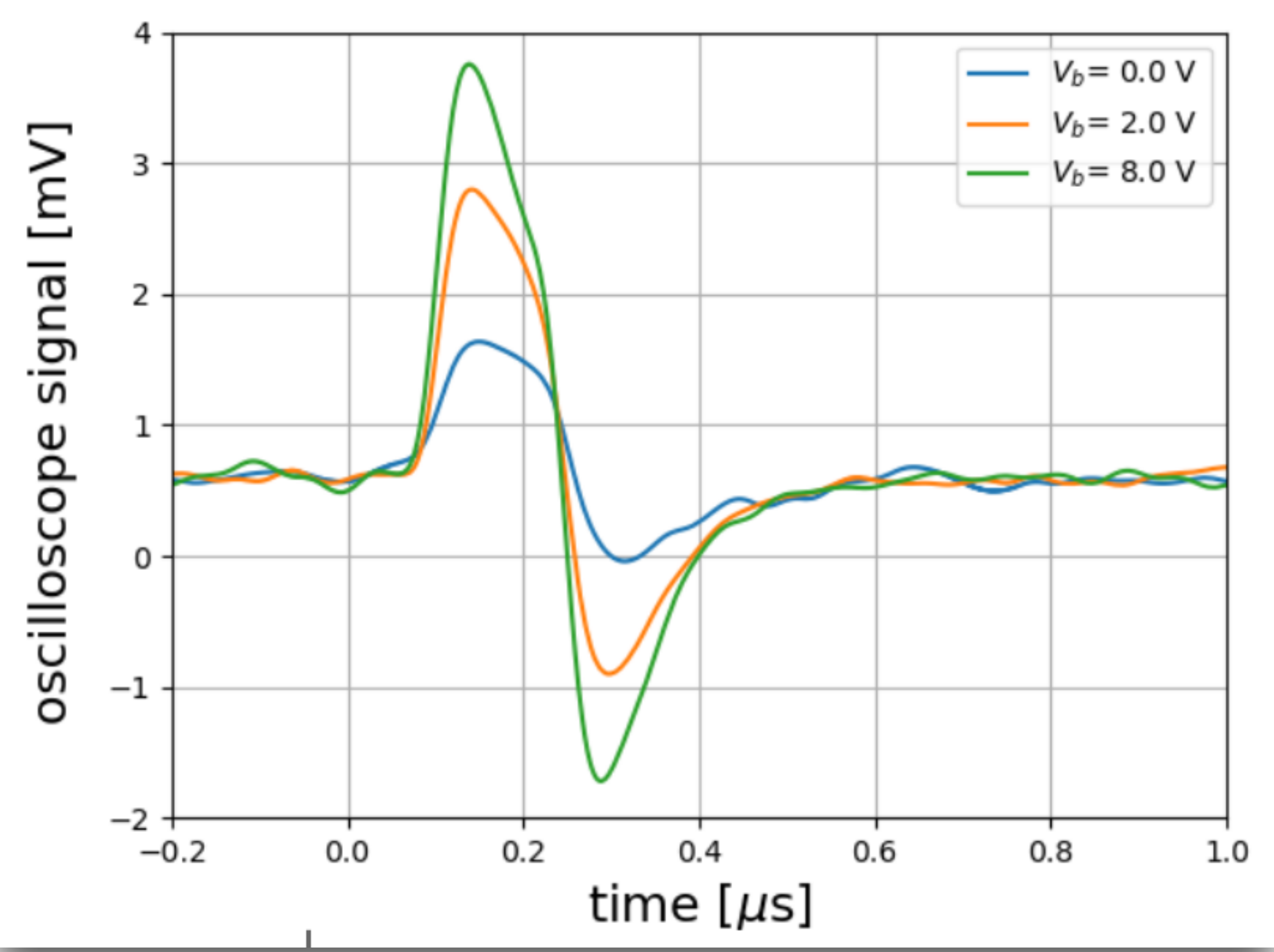


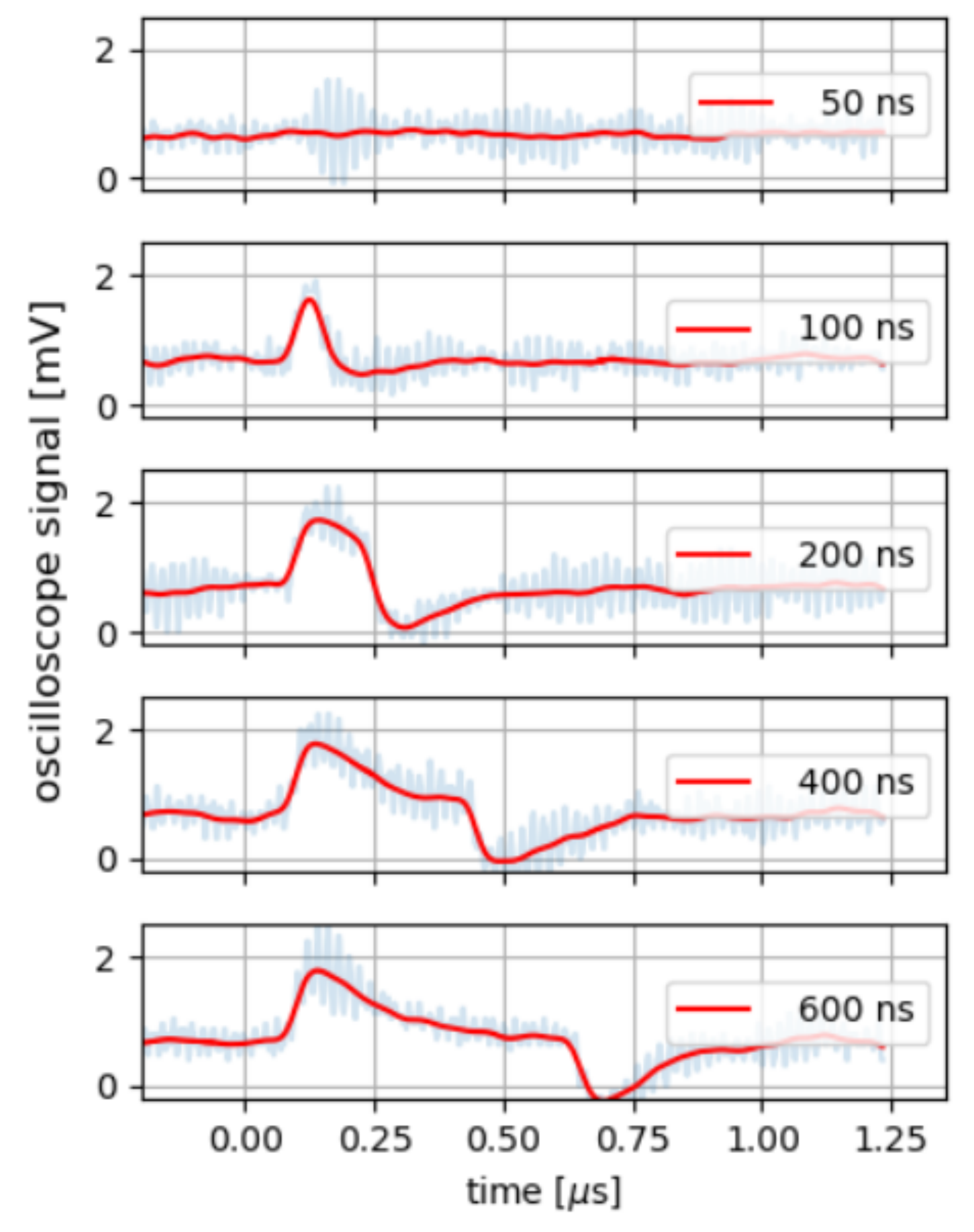


ADVANCED TECHNOLOGIES INVESTIGATION - MACETCH TEST

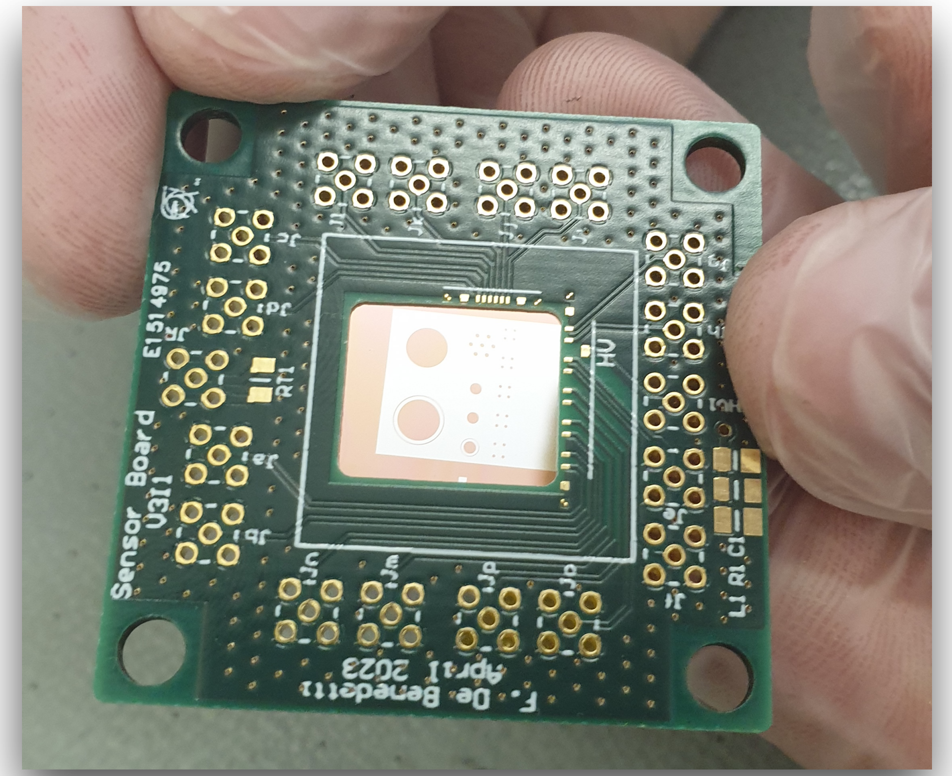
- **Setup:**
  - MacEtch sample from PSI p on n wafer.
  - Sample wire bonded to carrier a board.
  - Signal amplification using the 16 channel readout board V1.
  - Injected signal with pulsed infrared laser.

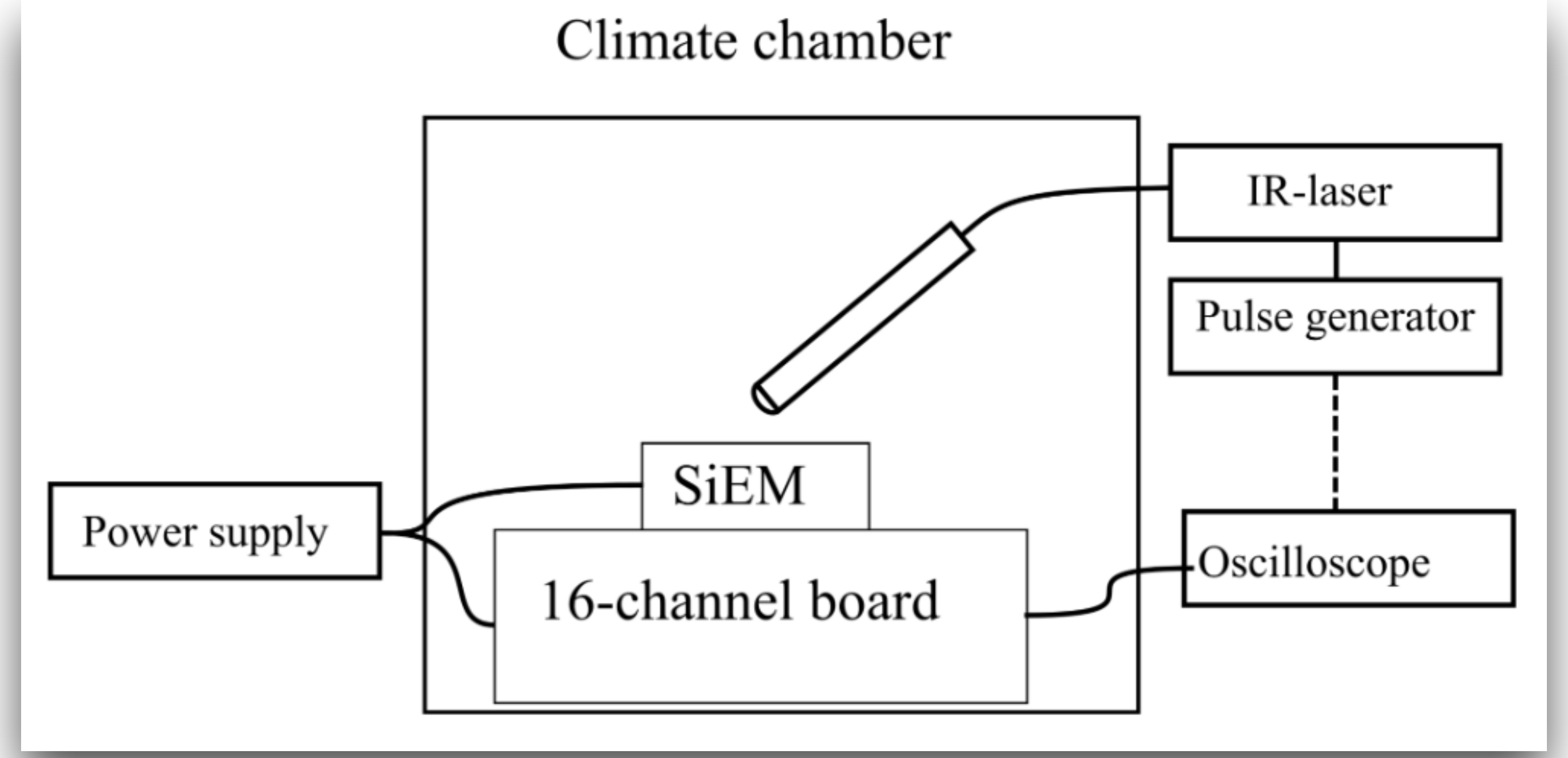
- **Preliminary results:**
  - Dependence with bias voltage observed.
    - Larger depletion region with increasing HV give larger signal.
  - High leakage current and non optimal wafer limit the gain analysis.





- **Next steps:**
  - Improvements in the setup are needed for future tests:
    - Laser setup commissioning, focusing beam on specific strip/pillar to isolate gain.
    - Full characterization of the 16 channels board V2 (gain and transfer function).
    - Cooling of the sensor.
  - Pillar VS strips comparison.





SUMMARY AND OUTLOOK

- Silicon Electron multiplier concept should allow to achieve charge multiplication with metal electrode embedded in the Si bulk.
- Gain mechanism should be intrinsically radiation hard.
- CNM DRIE demonstrator production is ongoing, first samples expected in few months.
- Simulation are being adapted to the produced geometry.
- MacEtch process investigated as a possible alternative approach to the DRIE process.
- Characterization setup used for the MactEtch structure is being extended to test the DRIE demonstrator.

Thank you!

Backup

PILLAR DETAILS