AIDA innova

Advancement and Innovation for Detectors at Accelerators

# WP10 – CSIC report

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3rd AIDAinnova annual meeting, Catania, March 2024

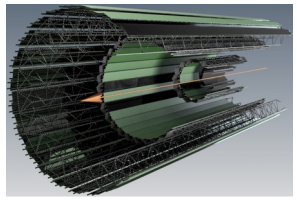
This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004761.

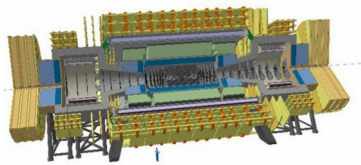
# Global R&D landscape

- detector R&D embedded in the global R&D landscape

## Future Projects Timeline

Agreed Working Hypothesis





Belle II upgrade (circa 2027):
https://arxiv.org/pdf/2203.11349.pdf

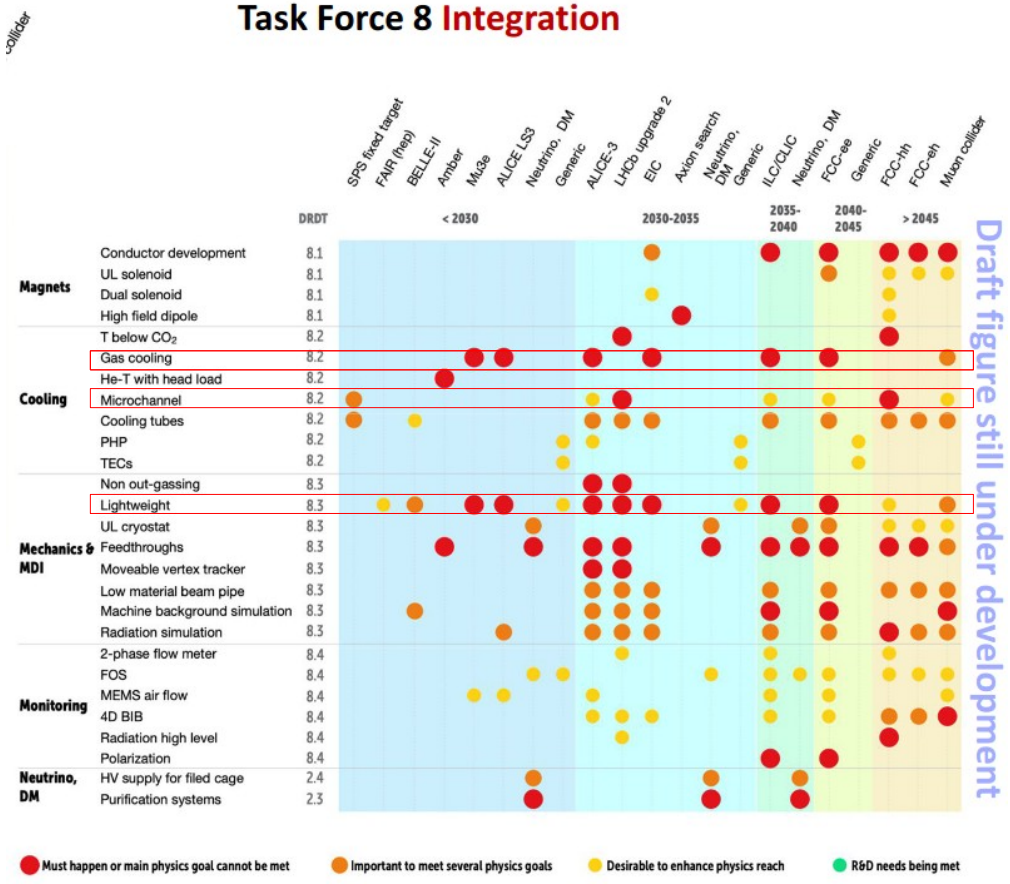



- Funding for “future” projects and “blue sky” R&D is scarce
- Try to use intermediate-timescale projects as stepping stones

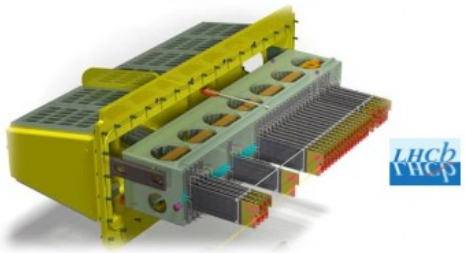
# ECFA R&D strategy

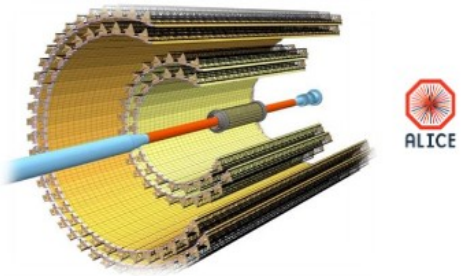
Important efforts in Europe and US to define detector R&D programs for upcoming experiments in particle physics

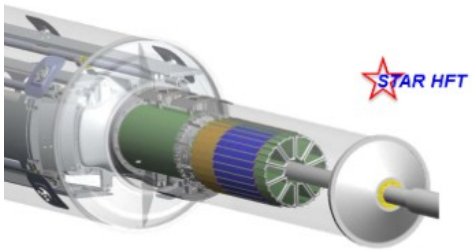
Cooling and low-mass structures are prominent
In many projects



# Ultra-light cooling



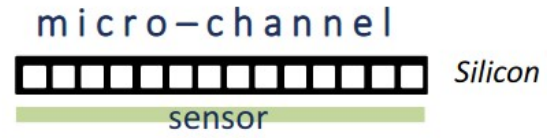
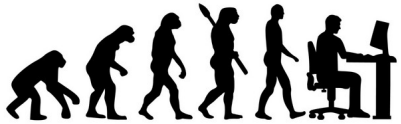
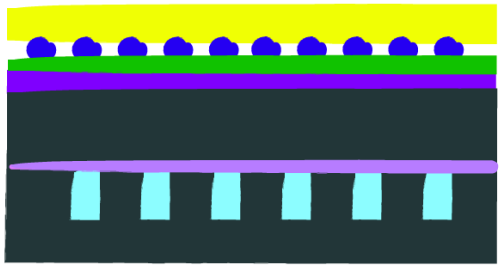






*Image from Corrado Gargiulo*

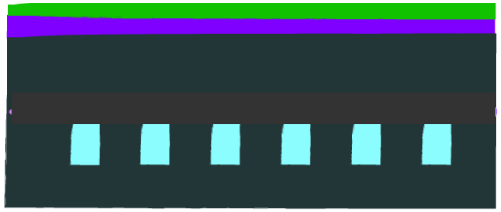
# MCC evolution: integrated cooling





Hybrid pixel detector &
micro-channel cooling plate

Monolithic CMOS detector



Monolithic CMOS detector
with integrated micro-channels

# WP10 CSIC activity

## Integrated detector design with support and cooling

- AIDA2020: production and characterization of several Silicon structures with/without micro-channels

- IFIC: Design of Belle 2 PXD upgrade, with U. Bonn, IJCLab, QM
  proto-typing self-supporting ladders with IZM
  FE simulation and setup to characterize cooling performance
- CNM: Development of in-house “post-processing” capacity
  anodic and eutectic bonding compatible with metal
  wafer-level integration of micro-channels in CMOS sensors

# WP10 CSIC personpower

Staff scientists at IFIC and CNM are guaranteed (but busy)
Difficulties finding/keeping clean room staff and mechanical engineers

- IFIC: Carlos Orero Canet starts in April 2024
- continuity beyond AIDAinnova ensured with regional funding

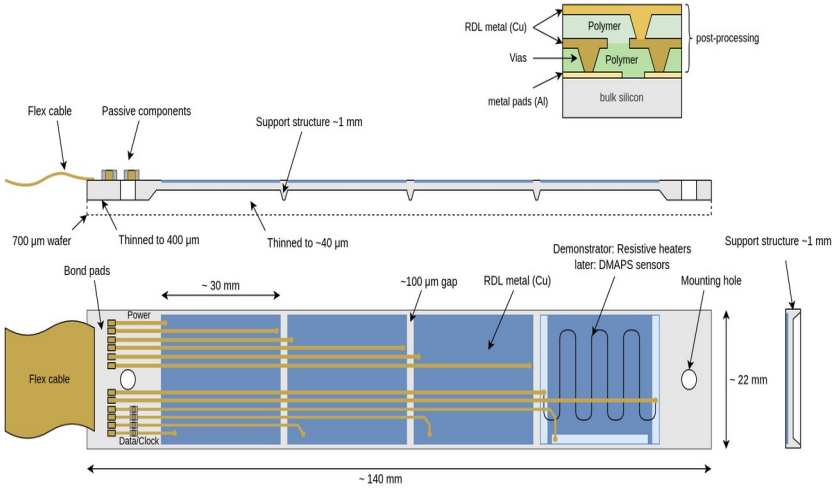
- IFIC: possible master project student from Oregon this summer

- CNM: lost clean-room technician, hiring replacement

# iVTX Inner Layer Concept

## All-silicon module < 0.15 % $X_0$

4 contiguous sensors diced as a block from the wafer
Redistribution layer for interconnection
Heterogeneous thinning for thinness & stiffness

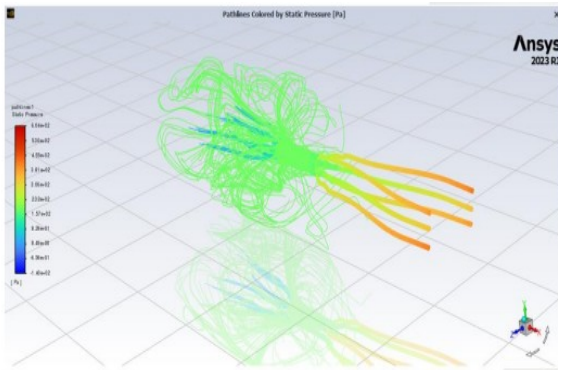


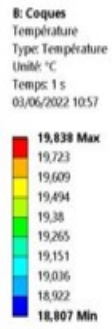

## Prototyping

First real-size ladders at IZM-Berlin with dummy Si
True iVTX geometry available

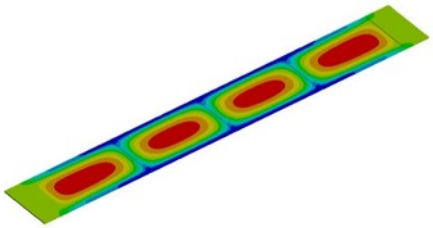
## Simulation on cooling

Dry air cooling 15°C
Assume 200 mW/cm$^2$

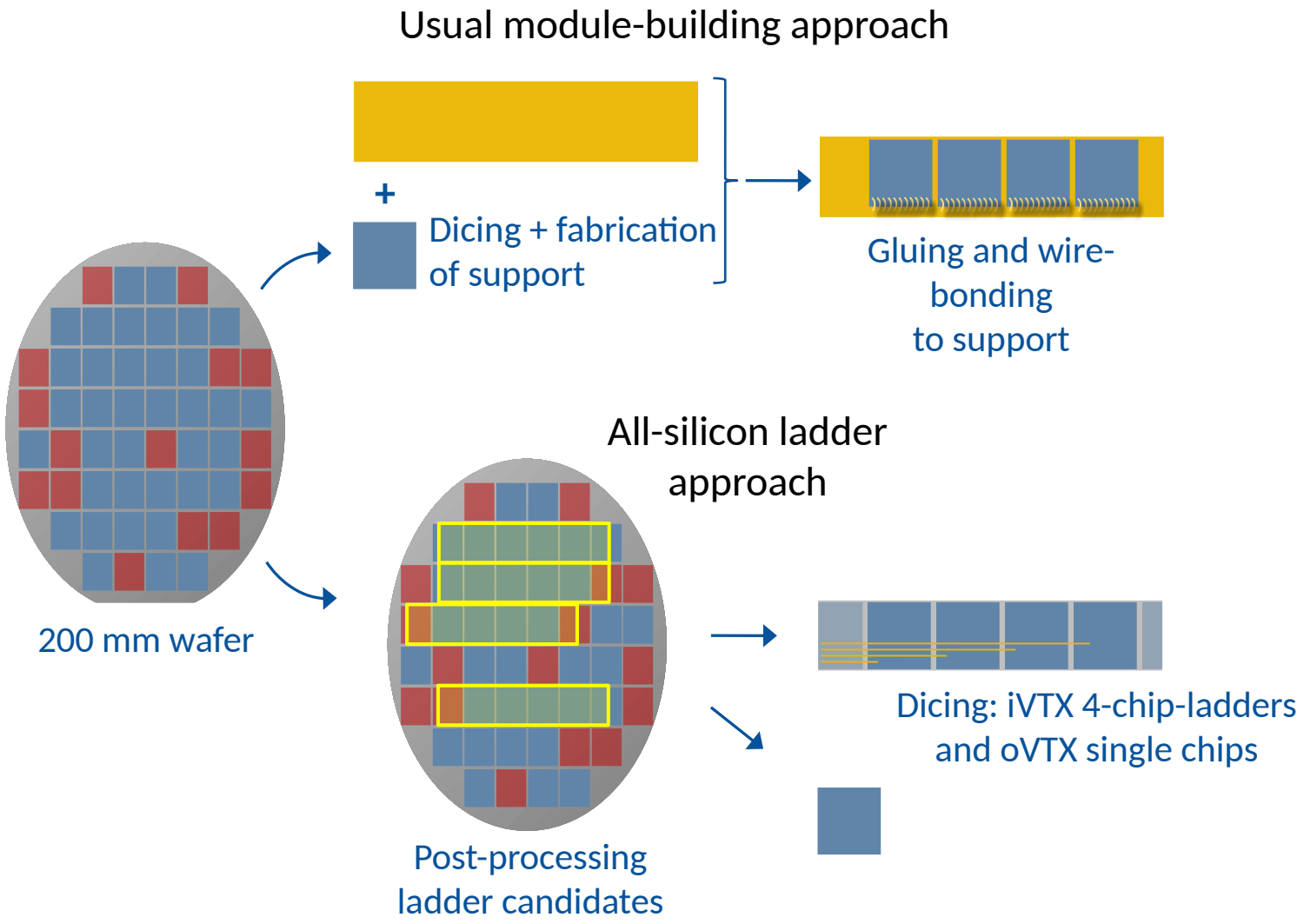


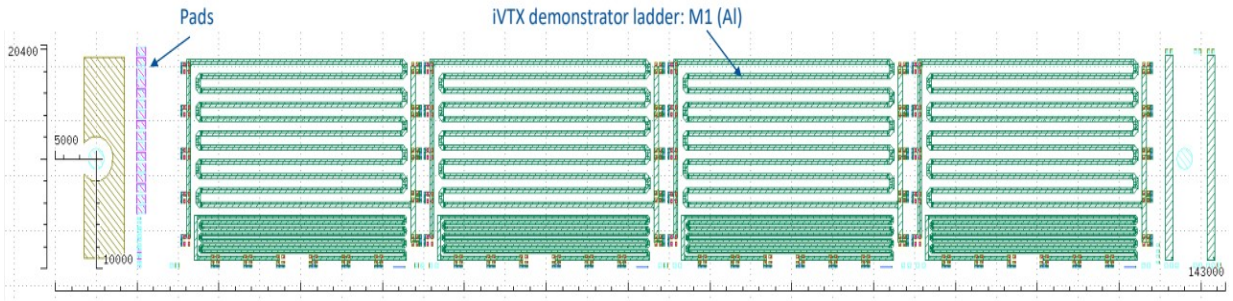

$T_{MAX}$ ~ 20°C
$\Delta T$ < 5°C

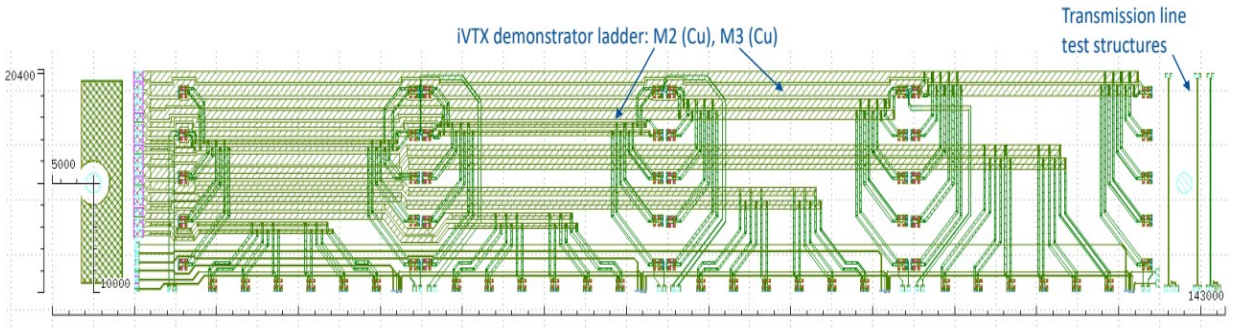


# All Silicon CMOS Ladders



# iVTX Ladder Demonstrator



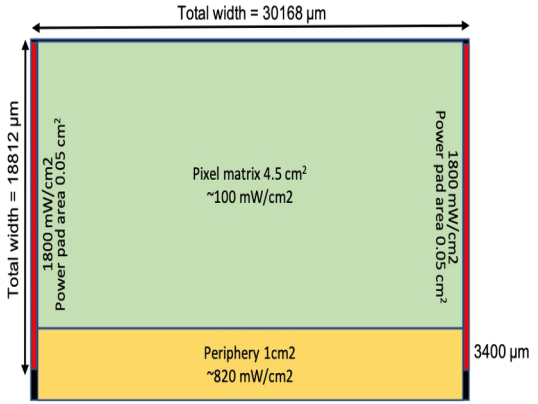

Metal system:

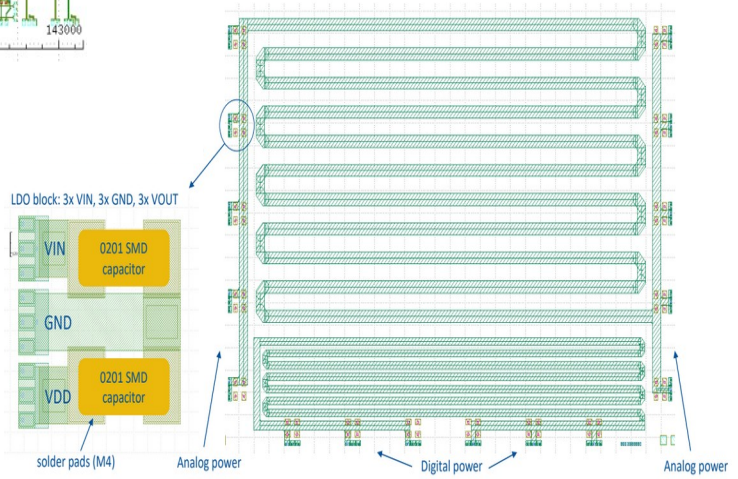
- Resistive heaters: 1.5 um Al (M1)
- 2 RDL metal layers: 3 um Cu (M2, M3)
- Top metal finish: NiAu (M4)

Wirebonding, SMD soldering

Final ladder dimension: 143 x 20.4 mm$^2$
Dummy heaters: 30 x 20 mm$^2$
Prepared for 1.7 mm mounting hole

Characterization of electrical, mechanical and thermal performance of iVTX ladders



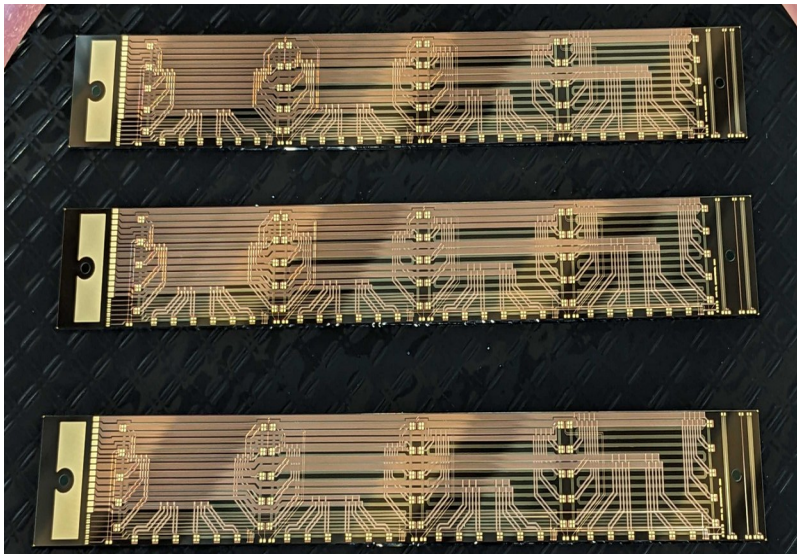



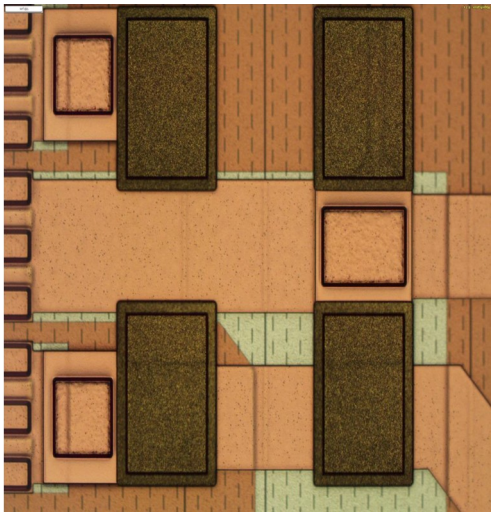
# iVTX Ladder Demonstrator

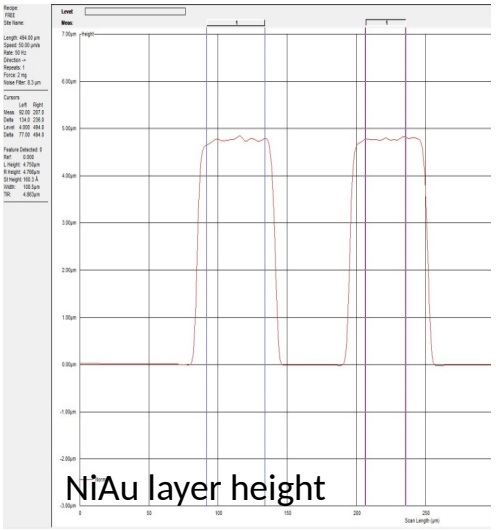
First demonstrators arrived at IFIC:
8 Wafers (725 µm, 400 µm, 300 µm)

Production at IZM finished smoothly

Characterization starting

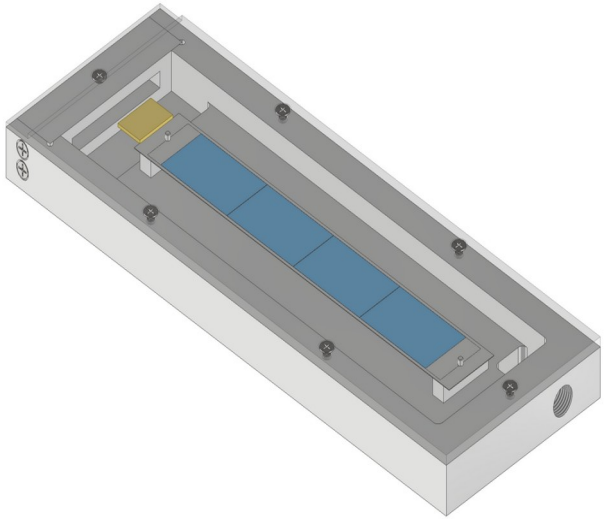


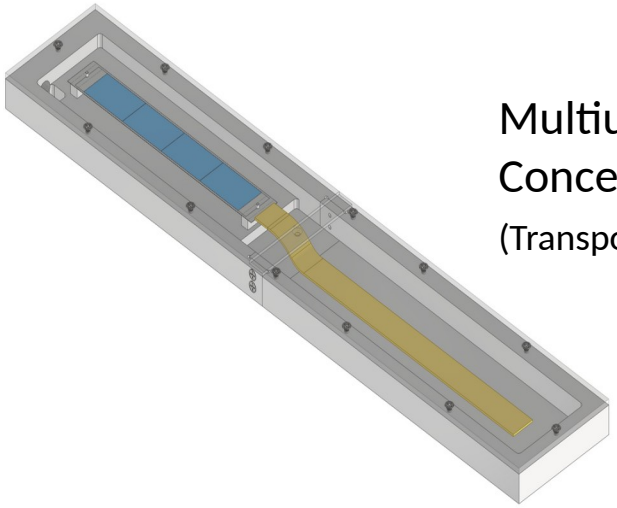




NiAu layer height

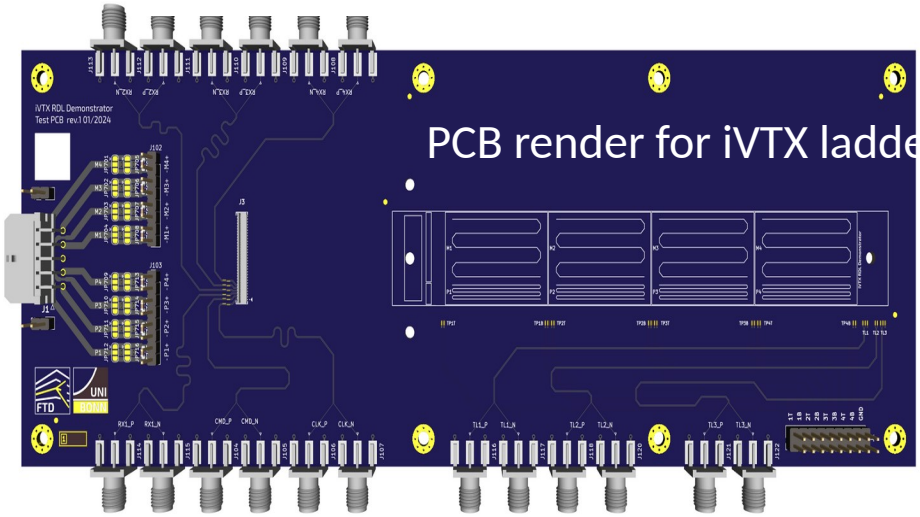
# iVTX Ladder Tests





Multiuse Ladder Box Concepts

(Transportation, bonding, tests)

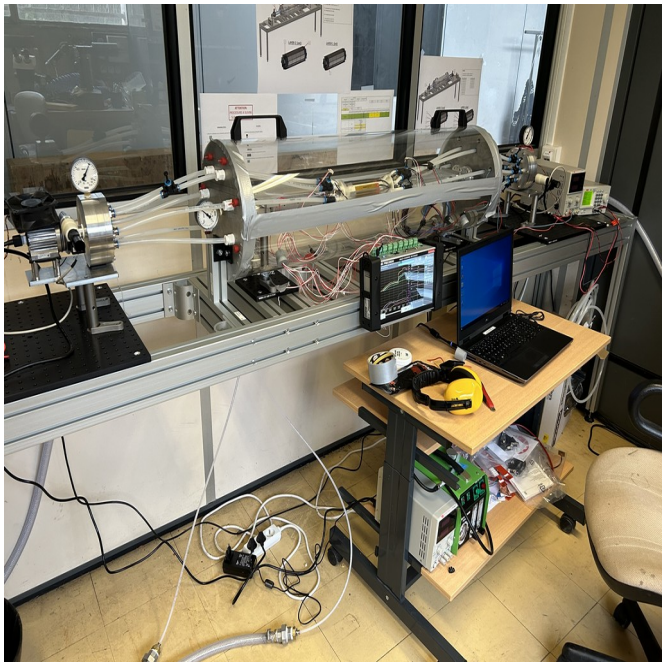


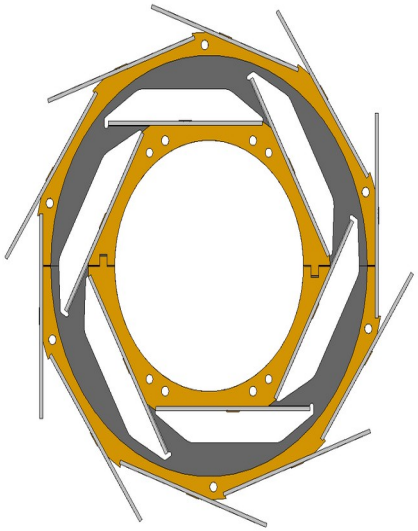

Configurable power routing and test points for I*R drop measurements

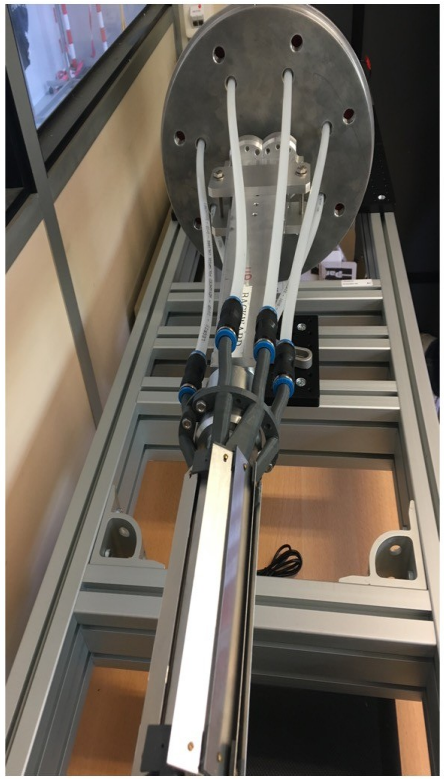
SMA connection for data lanes and and TDR measurements

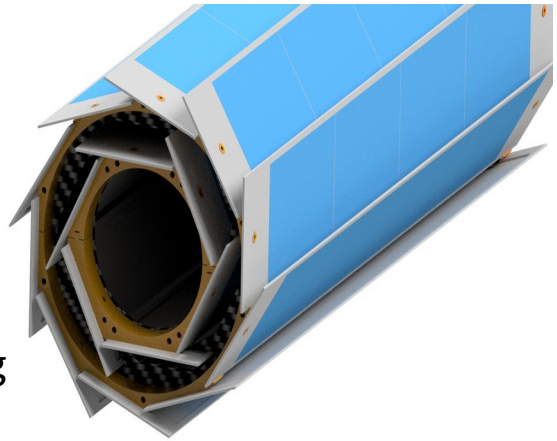
Also preparing a PCB mockup of the ladder to practice soldering etc

# iVTX Integration and Cooling









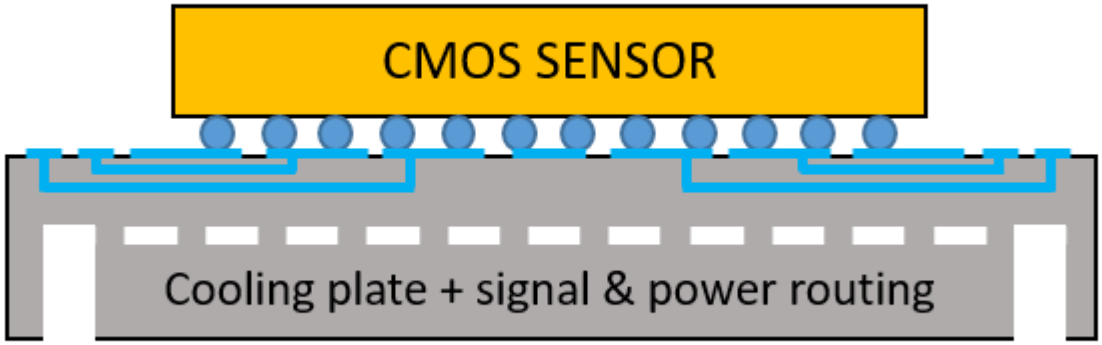
iVTX wind tunnel to study flow

Air cooling feasibility under study

Next: ladder mounting/service routing

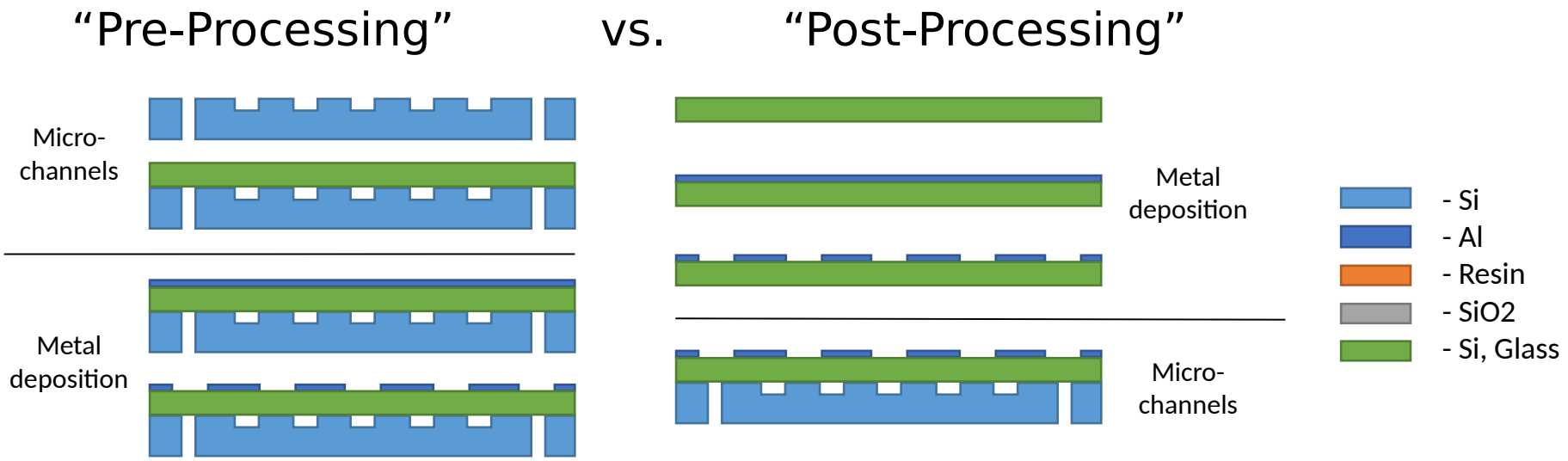
# CNM results

First objective: integration of micro-channels in silicon plates with integrated signal and power routing. **Achieved!!**



# Technological process

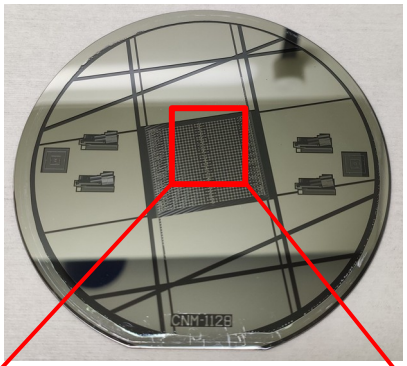
- Technological options
  - **Pre-processing**: The microchannels are created first, sealed, and only then the metal is deposited on the assembly and structured with a photolithographic process
  - **Post-processing**: The metal is deposited and structured first on a single wafer, then the buried microchannels are created by wafer bonding (at low temperature)

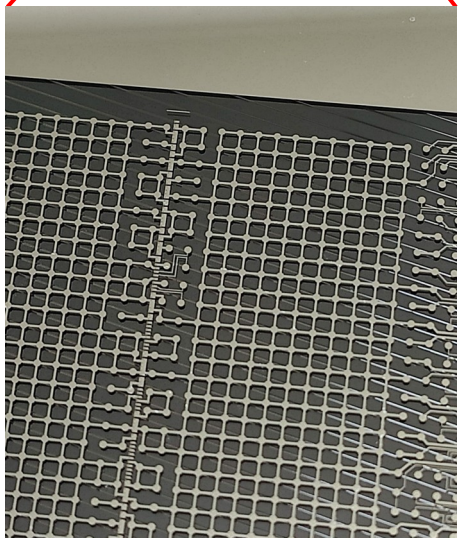


# Silicon plates – Results

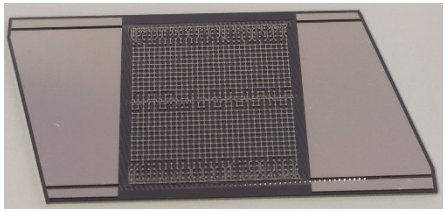
## Pre-processing:

- Successful integration of microchannels in silicon plates with integrated signal and power routing



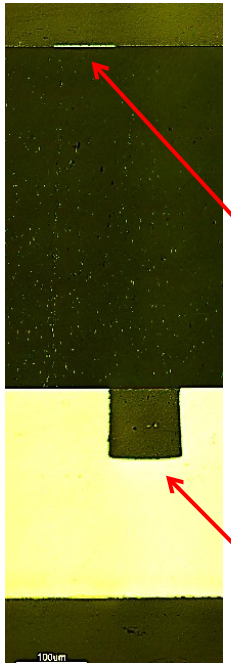



**Silicon plate**



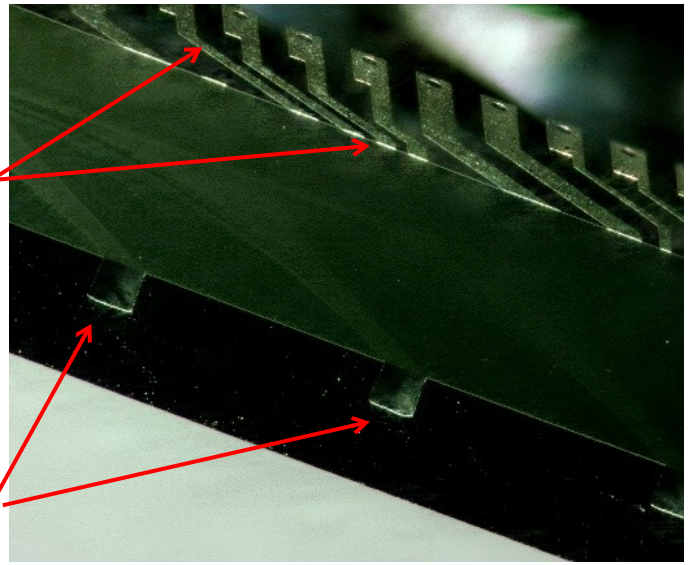
Front

Back



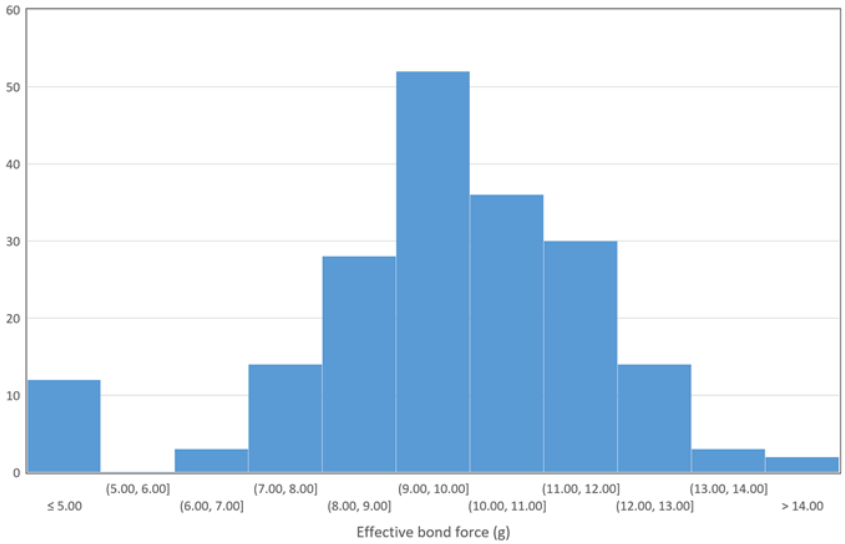

Metal tracks

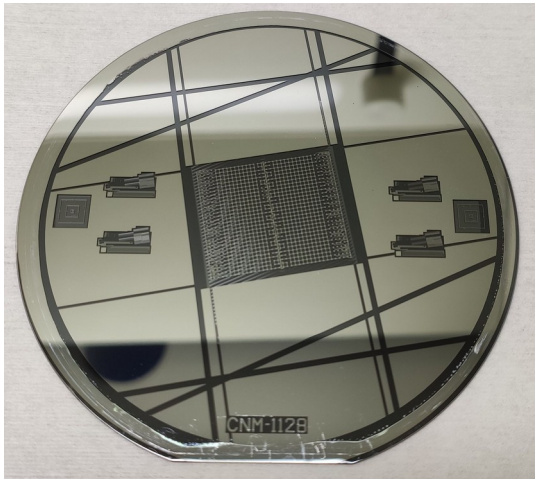
Microchannels



# Quality of metal

- Tests of the metal system: bondability
  - Hundreds of wire-bonds made and pulled on full assemblies
    - 25 µm Aluminum wire.
  - Test performed on **Pre-processing** sample
    - Average bond force obtained: 9.5 ± 1.3 g



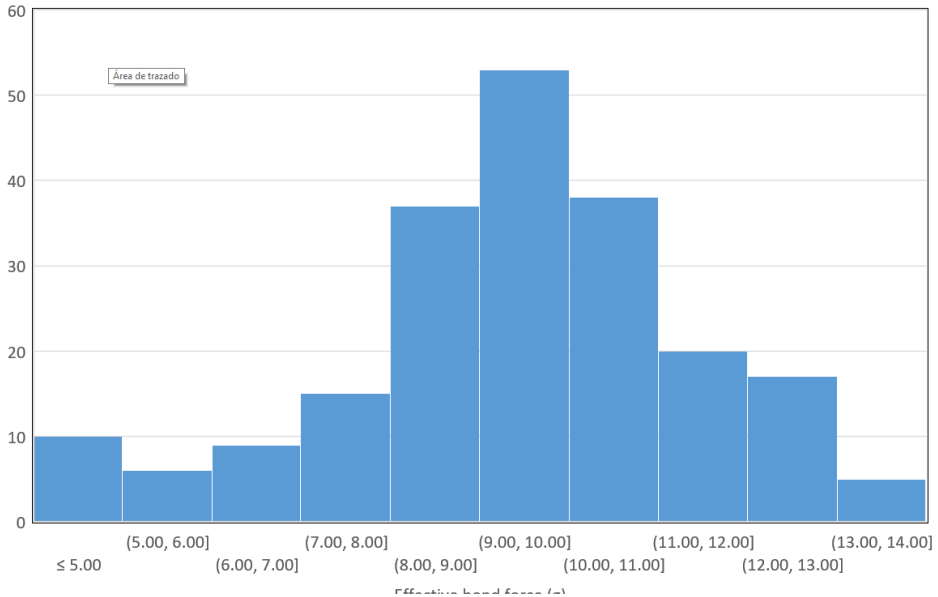
# Post-processing

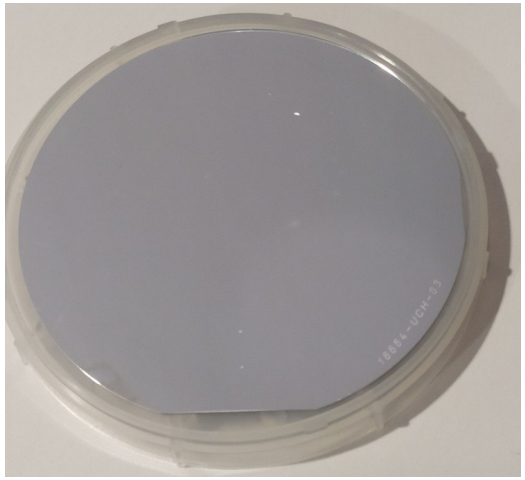
**Post-processing:**

- Optimization of metal deposition process
  - Sputtering deposition of the metal at high temperature (350 ºC) so the metal is not degraded during the bonding process at high temperature
    - Better metal test results on blanket wafers
  - Still some localized problems observed in the metal layer
    - Could be derived from the ion displacement within the glass wafer, inherent to the anodic bonding process
- Process modification to deposit the metal on the Silicon side.
  - Good metal results in blanket wafers, with anodic bonding
  - Final full assemblies with structured metal (signal and power tracks) on-going
  - Good step forward for CMOS integration process !

# Quality of metal

- Tests of the metal system: bondability
  - Test performed on **Post-processing** blanket assembled sample
    - Metal on the silicon wafer
    - Average bond force obtained: 9.6 ± 1.8 g



No degradation of the metal system: technology for integration of embedded microchannels and metal routing demonstrated (pre-processing and post-processing)

# CSIC summary

**Aim: integrate support structures and micro-channel cooling in “large” CMOS ladders for Belle 2 upgrade and Higgs factories**

**Development of low-temperature bonding compatible with CMOS post-processing ongoing at CNM (M. Ullan), see also L. Andricek for HLL**

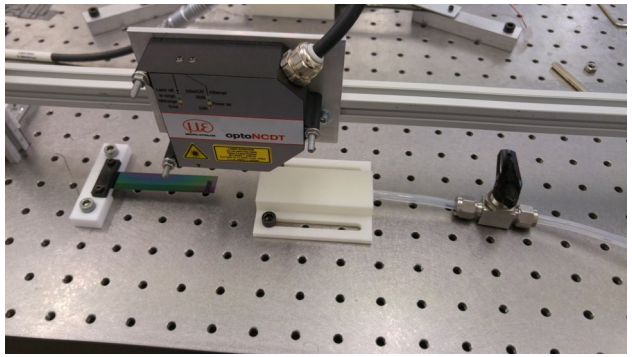
**Integrated micro-channel and metal systems on Silicon: pre-processing and anodic bonding successfully demonstrated. Eutectic bonding soon!**

**Belle 2 upgrade: extensive FE simulation and prototype measurements to demonstrate gas cooling for very thin ladders. Use simulation to compare to micro-channels.**

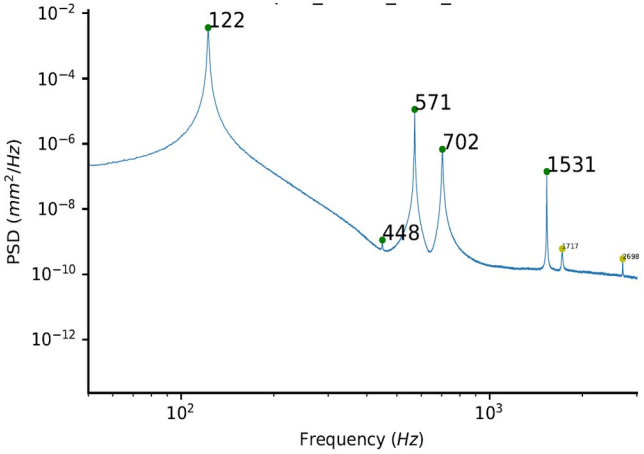
**Small steps: mechanical prototypes, simulations & dummy CMOS wafers within AIDAinnova, full demonstrator beyond the timeline of the project.**

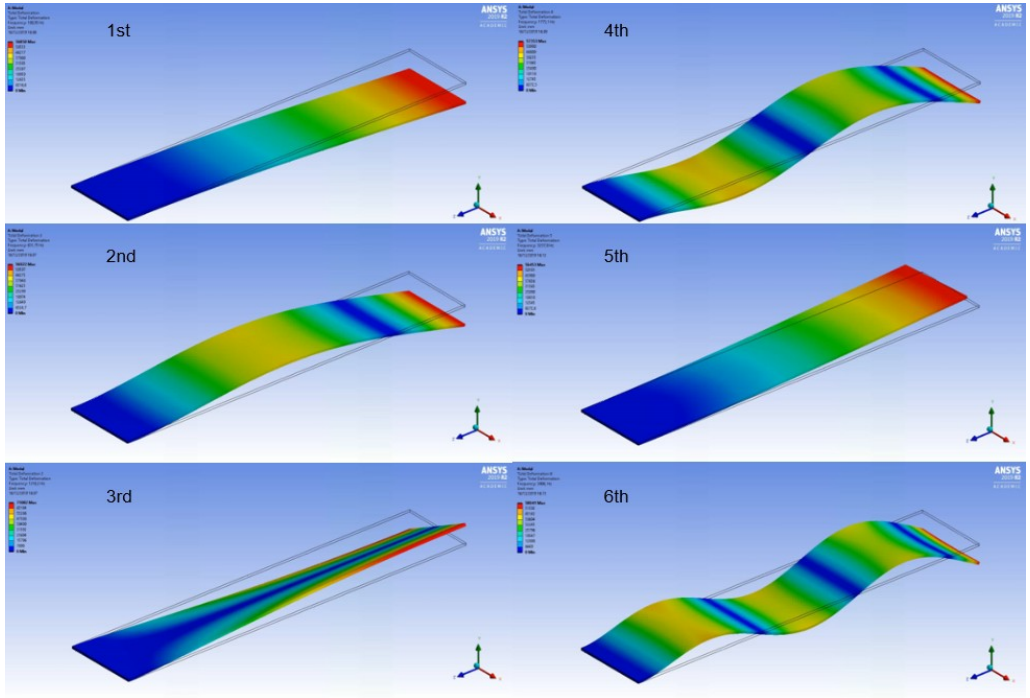
# Measurements

Multiple silicon structures measured in Oxford and Valencia

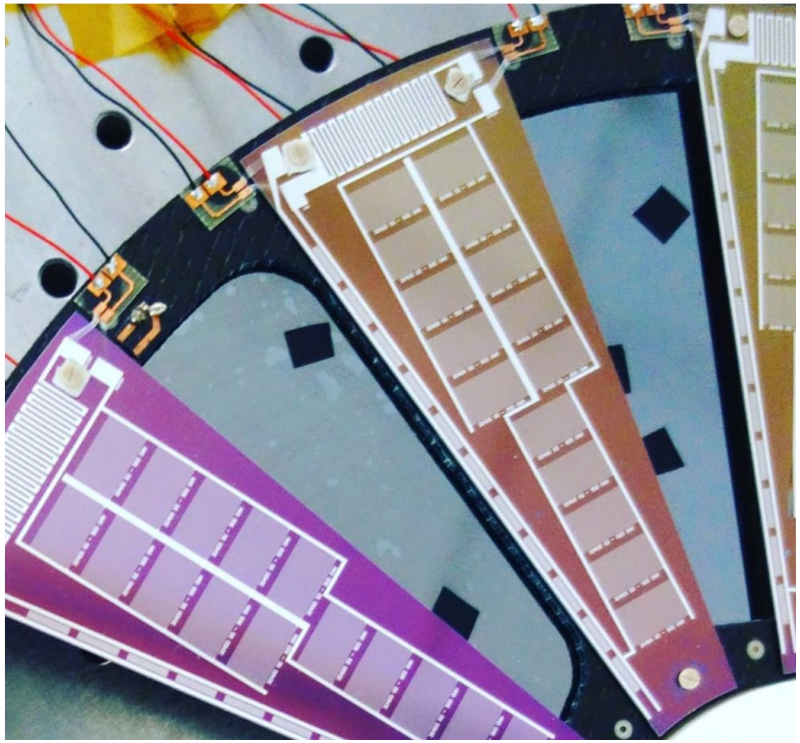



Vibration Setup – IFIC Valencia



# Vibration analysis



Master's thesis Yamal Naser Requena

Analytical expressions

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ANSYS FEA

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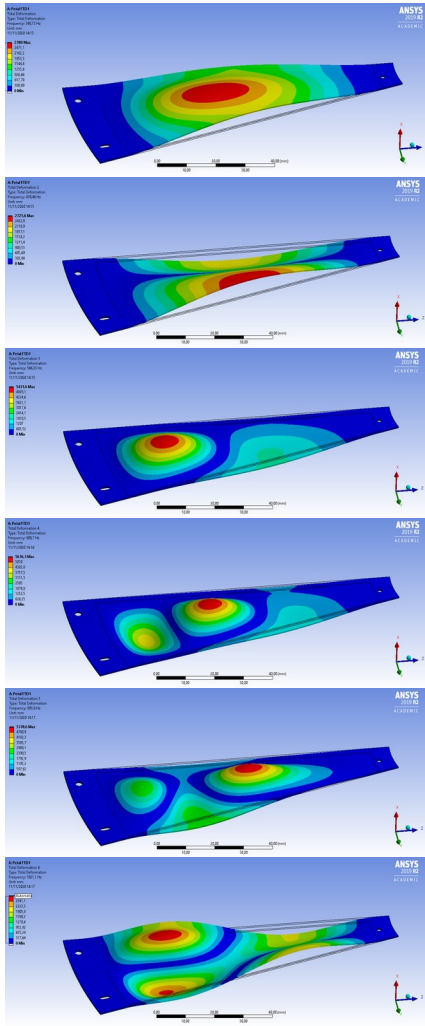
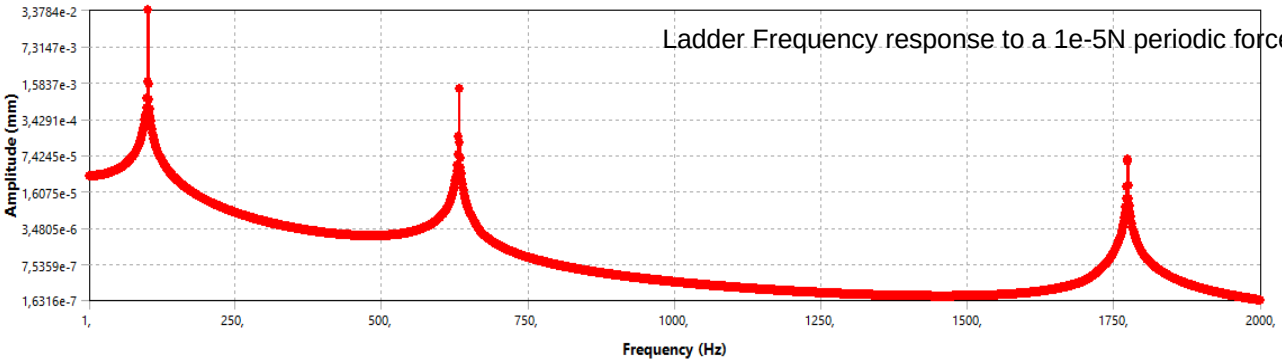
Measurements

Extend to more realistic vibration loads (air flow, cavern floor, earthquake)





# WP10 – CSIC - NEWS

**Milestone MS41 with minor delay**

**Executive summary:**

- CNM anodic/eutectic bonding (see M. Ullan)
- HLL direct bonding (see L. Andricek)
- INFN effort on CoolFPGA (see L. Bosi)
- buried channels currently uncovered

Grant Agreement No: 101004761

**AIDAinnova**

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

## MILESTONE REPORT

## COMBINED WORKPLAN WITH OBJECTIVES AND TEST DEFINITION FOR ALL TECHNOLOGIES

### MILESTONE: MS41

| | |
|---|---|
| **Document identifier:** | AIDAinnova_MS41.docx |
| **Due date of milestone:** | End of Month 11 (February 2022) |
| **Justification for delay:** | [if delays occurred] |
| **Report release date:** | 07/03/2022 |
| **Work package:** | WP10: Advanced mechanics for tracking and vertex detectors |
| **Lead beneficiary:** | CERN |
| **Document status:** | Draft |

# Summary

- Technology for integration of embedded microchannels and metal routing demonstrated (pre-processing and post-processing)
- Successful fabrication of pre-processing silicon plates with microchannel cooling and integrated signal and power routing
- Good bondability tests results of the metal on the silicon plates with pre- and post-processing

Next steps:

- ❖ Full silicon plates to be finally fabricated with post-processing (on-going)
- ❖ Improve eutectic bonding
- ❖ Thermal and fluidic tests with fabricated silicon plates
- ❖ Working on further integration of microchannel cooling for a full system
  - ➢ Full monolithic integration with CMOS sensors
  - ➢ Exploring other technological options (microchannels on glass, TSV, …)