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SI LAB
Silizium Labor Bonn

STATUS UPDATE ON WAFER-TO-WAFER INTERCONNECTION

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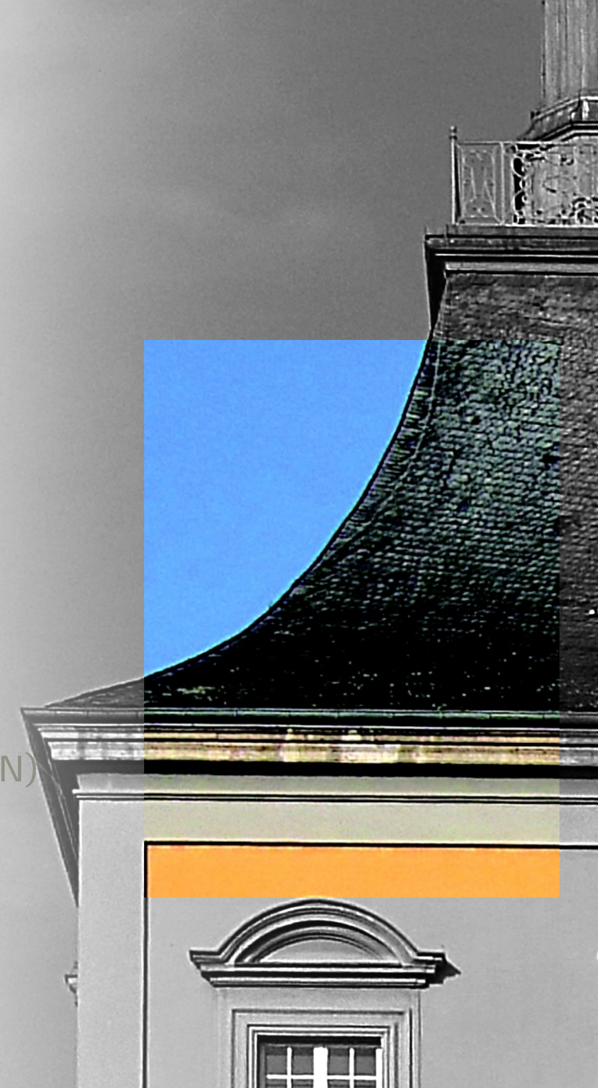
AIDAINNOVA WP 6 MEETING,
CATANIA, 19 MARCH 2024



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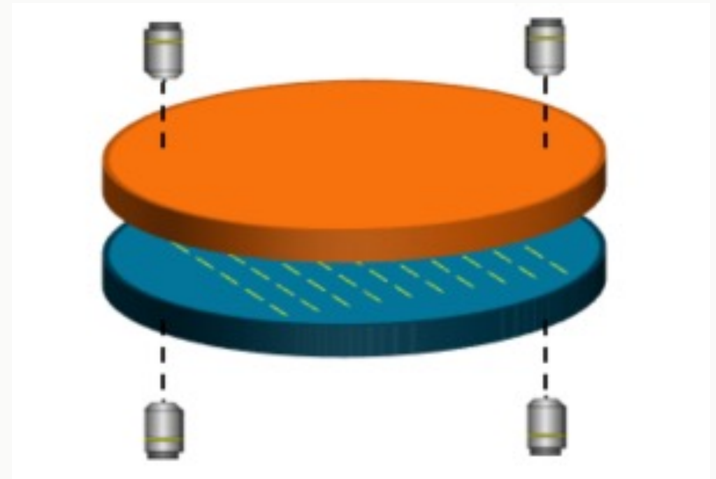
PROOF OF CONCEPT PROJECT FOR AIDAINNOVA

- Develop dedicated CMOS Sensor wafer compatible with a pixel FE chip wafer:
  - Starting point: passive CMOS sensor development on 200 mm wafer with 110/150 nm process node from LFoundry
  - Use TimePix3 chip wafers (GF 130 nm on 200 mm wafers)
  - Keep own FE development on the same wafer as the sensor as backup option
- Developing and optimization of hybridization process including thinning and interconnection from chip's backside at IZM.
- Longer Term: Transfer process to more modern feature size pixel chips (65nm or 28 nm on 300 mm wafers) for smaller pixel pitches and faster electronics



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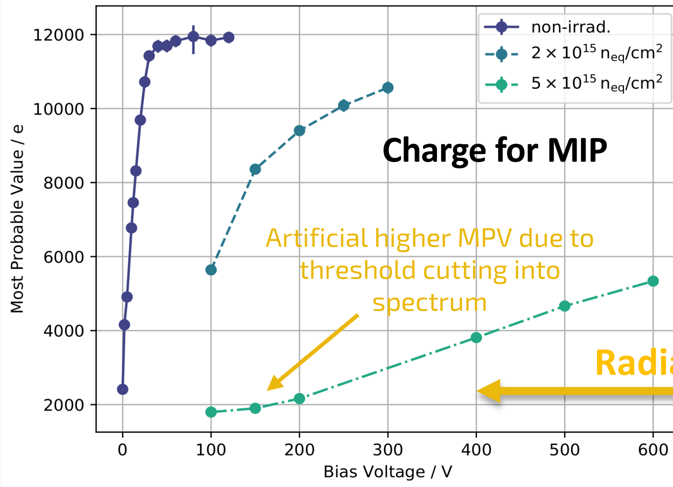
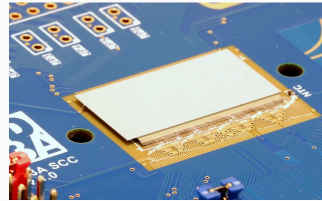
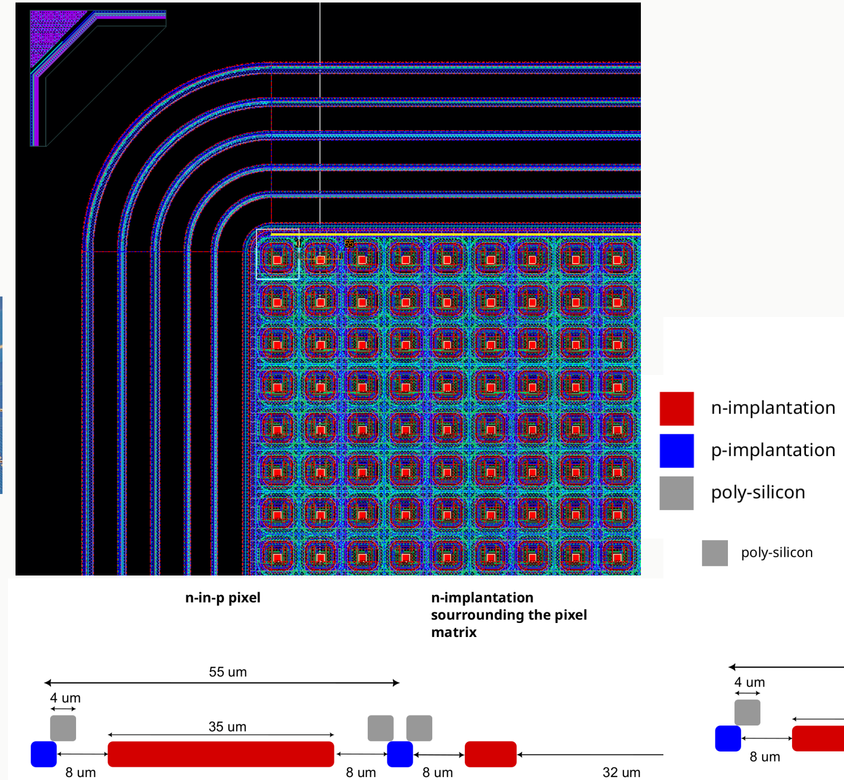
SENSOR WAFER DESIGN

- Layout is derived from former passive CMOS sensor submissions
  - Increased n-implant width from 30 um to 35 um in order to match 55 x 55 pixel
  - 5 x n-p guard ring structure
  - Bias grid + DC-coupling with bias resistor (4 – 5 MΩ)



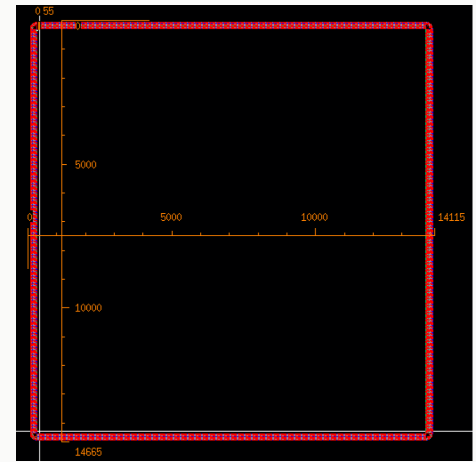


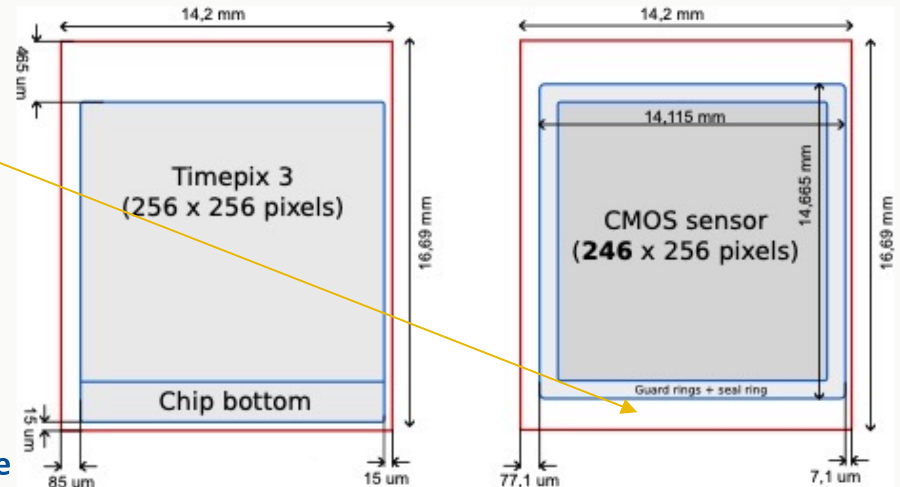


SENSOR WAFER DESIGN

- CMOS sensor has to fit into same reticule as TimePix3 chip
  - use only 246 pixels in horizontal axis, instead of 256

    → All chips can be used after dicing
- Smaller sensor pixel matrix is not a problem for sensor or TimePix chip
- Few things still to be defined:
  - TSV etching through TimePix3 chip such that chip pads are accessible from chip backside
  - sensor backside HV contact requires the usage of fully processed sensors incl. thinning, backside implantation and metallization for the W2W bonding process
- Status:
  - Design ready only a few clarifications with foundry are still pending
  - **Quote from LFoundry available, tape-out could be done within the next weeks/months → wafers could be available by end of summer**





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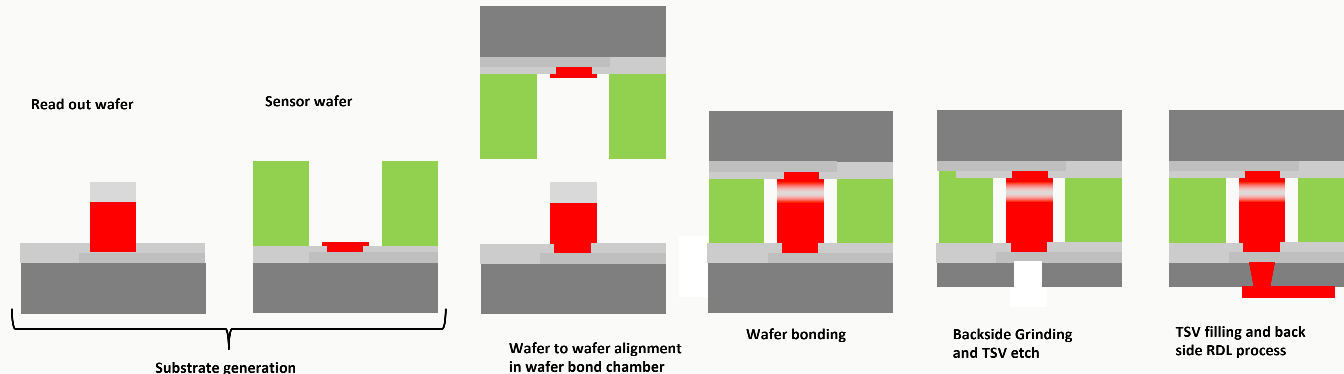
W2W BONDING PROCESS DEVELOPMENT AT IZM

- **WP1: Design development and manufacturing of process qualification wafer, design preparation of functional TIMEPIX3 and DMAPS sensor wafer**
  - 1.1 Definition of technological approach for ultra-thin low-mass hybrid pixel detectors
  - 1.2 Process qualification design including test structures
  - 1.3 Fabrication of process development wafer
  - 1.4 Design and mask preparation for TIMEPIX3 readout electronics and DMAPS active sensor wafer
- **WP2: Wafer bonding and thinning process**
  - **Bonding material evaluation and process setup** → new material identified and process setup is done now
- **WP3: Wafer bonding with capacitive coupled IOs and conductive IOs**
- **WP4: Backside wafer process with TSV-etching and backside metallisation process**

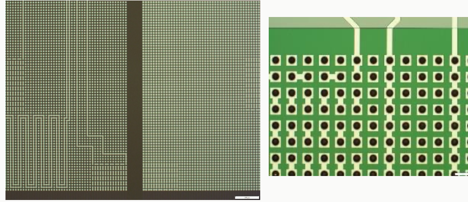
W2W BONDING - GENERAL PROCESS FLOW

- The Cu/Sn wafer bonding is a well established process
- The Cu/Sn bond will be supported by spin coated, photo-structured polymer layer which is joined simultaneously (polymer hybrid wafer bonding)
- Depending on total wafer stack thickness a mechanical support during TSV formation and backside RDL process will be required

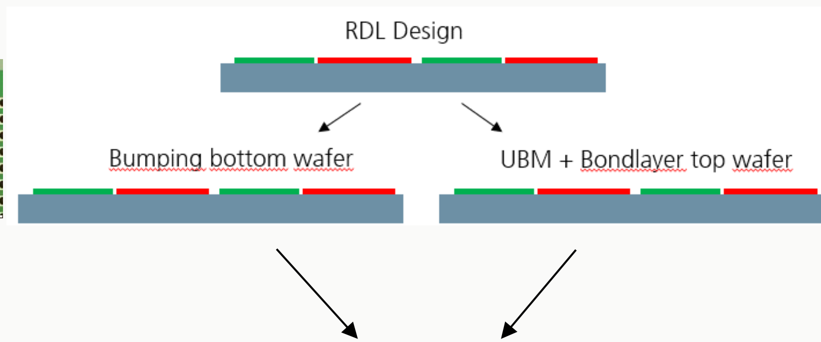


PROCESS SETUP USING DAISY CHAIN WAFER

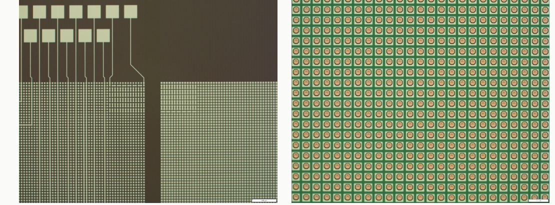
W2W bonding setup bottom wafer:



Bottom wafer with Cu-SnAg pillar



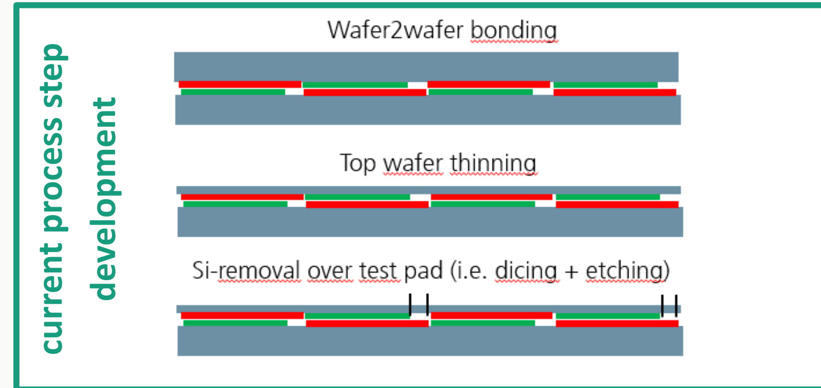
W2W bonding setup top wafer:



Top wafer with Cu-Pad and polymer layer

Process Development Goal:

Evaluation of a bonding material that enables the combination of a polymer glue bonding process with the Cu-SnAg pillar bonding process



Process evaluation with different wafer stacks:

I. Planar Glass-Si wafer: optical bonding interface characterization (fast track)

II. Planar Si-wafer with UBM: polymer bonding with topography wafer

III. Daisy-chain-test wafer (silicon to silicon): bonding process evaluation with focus on polymer layer thickness – Pillar/UBM height tolerances

Details of different wafer stack types see next slides

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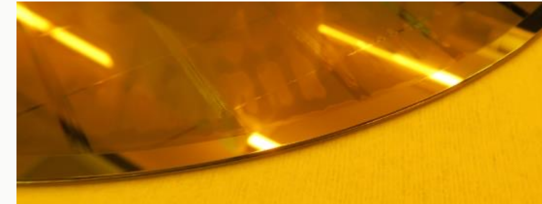
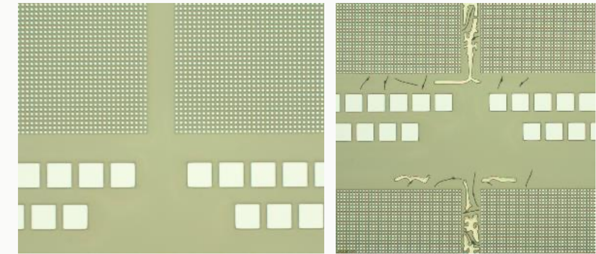
W2W BONDING – PROCESS EVALUATION I

TOP wafer: planar Si-wafer with patterned polymer layer
BOTTOM wafer: planar glass-wafer

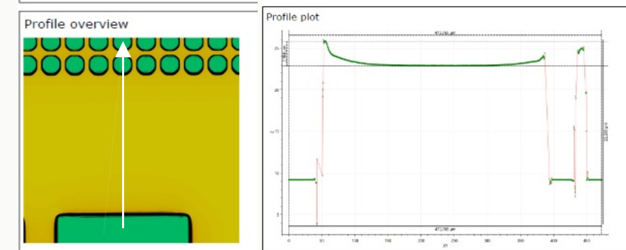
- **Wafer to wafer polymeric bonding material evaluation:**
  - Development of process chain for metal - polymer hybrid bonding
  - Silicon-glass wafer bond for visual inspection
  - (Evaluation of different bonding materials – to be continued)
- **Processing of setup bond wafer:**
  - Bond layer thickness adjustment
  - Bond layer planarity optimization
  - pre-conditioning of polymer
  - Influence of curing temperature
  - Bond parameter setting (pressure, temperature, time)
- **Evaluation target:**
  - Polymer layer height and planarity
  - Void-free bonding
  - No outgassing during bonding process
  - Lateral structure size stability



Si-Glass wafer stack (glass wafer on top)



Left: good bond; right: voids in bondlayer



Bond-layer thickness and planarity measurement (measurement before bonding)

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W2W BONDING – PROCESS EVALUATION II

TOP wafer: planar Si-wafer with polymer

BOTTOM wafer: pillar/UBM pad test wafer without solder

Polymer layer height and planarity

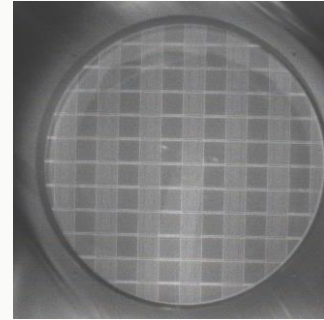
- Polymer process on planar Si-wafer
- Planarization process developed and evaluated
- Evaluation of bonding layer thickness along the process chain, calculation of pillar and UBM height

Bonding test and characterization

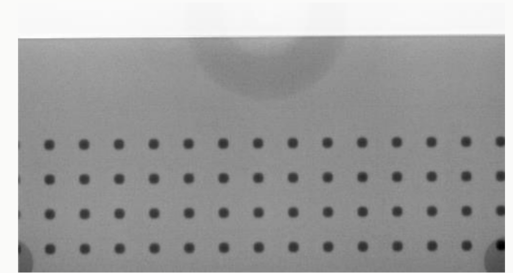
- Bonding test using pillar/UBM pad test wafer without solder for layer height analysis in combination with topography
- Check of characterization methods (IR, X-ray, cross section)

Preliminary Process Results

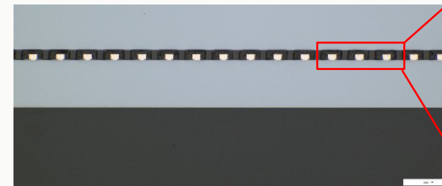
- Process evaluated for 20µm polymer layer thickness
- Bonding parameter profile setup tested (temperature, pressure, time, ramping)
- Bonding test successful: no delamination, stable pattern structure

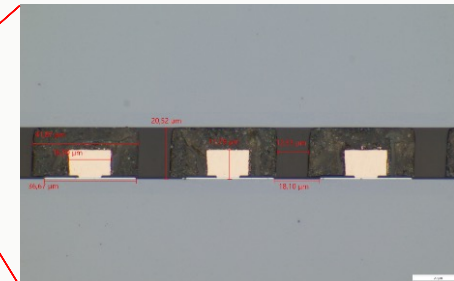


Full wafer IR image, details are to small for bond layer characterization



X-ray inspection of bonded chips, poor contrast of bond layer details and aluminium lines, only Cu pads visible





Bond layer evaluation and feature height measurement using Cu pillar + RDL test wafer
Recalculation of the required pillar + UBM height based on bond layer thickness results

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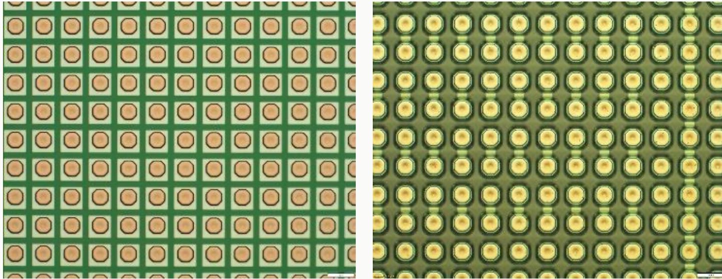
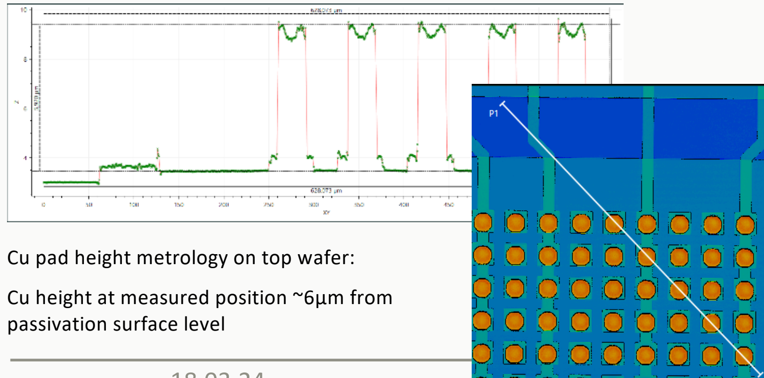
W2W BONDING – PROCESS EVALUATION III: DAISY-CHAIN-TEST WAFER

TOP wafer: Cu UBM pad and patterned polymer layer



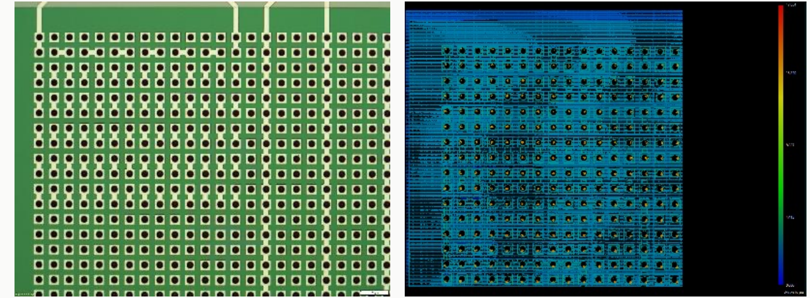
Cu-UBM pad wafer without (left) and with polymer bond layer (right)

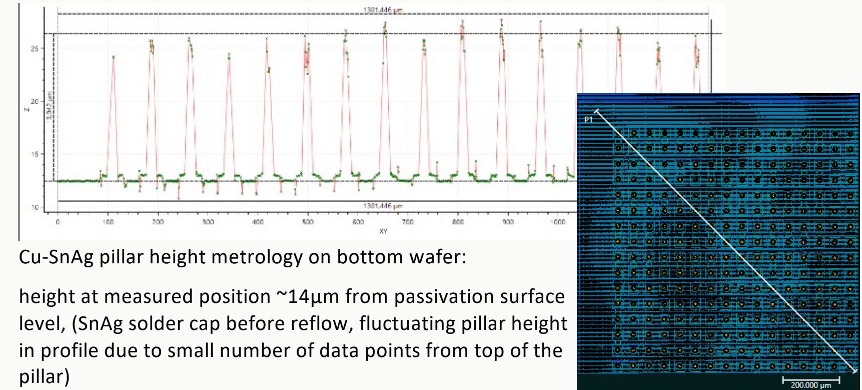


Cu pad height metrology on top wafer:

Cu height at measured position ~6µm from passivation surface level

BOTTOM wafer: Cu-SnAg pillar





Cu-SnAg pillar height metrology on bottom wafer:

height at measured position ~14µm from passivation surface level, (SnAg solder cap before reflow, fluctuating pillar height in profile due to small number of data points from top of the pillar)

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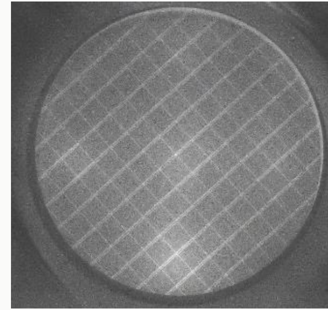
W2W BONDING – PROCESS EVALUATION III: WAFER TO WAFER BONDING

Bonding process evaluation using daisy-chain-test wafer:

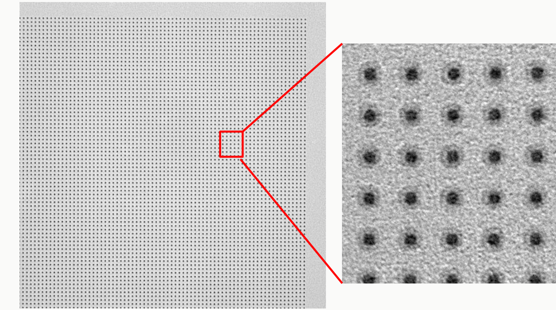
TOP wafer: UBM pad and patterned polymer layer
BOTTOM wafer: Cu-SnAg pillar

Preliminary Process Results:

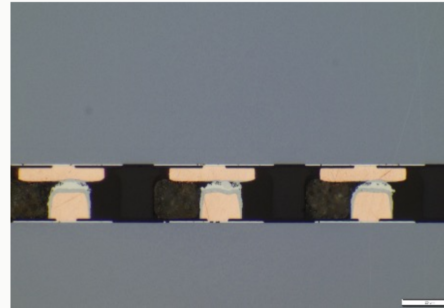
- Process evaluated for 20µm polymer layer thickness, measured bond layer thickness: 21µm (+/- 0.5µm across the wafer)
- Pillar height: 13…15µm (as plated) (tolerances across the wafer)
  Cu pad height: 5.5µm (+/- 0.5µm across the wafer)
- Thinning of top wafer to 80µm thickness possible
- Dicing of wafer stack possible
- Low adhesion between top and bottom chip after dicing (chips can be easily de-bonded)
- Large area solder transfer from CuSnAg-pillar (bottom chip) to Cu pad (top chip) visible after top chip debonding but some pillars are not connected to Cu pads (see cross section)

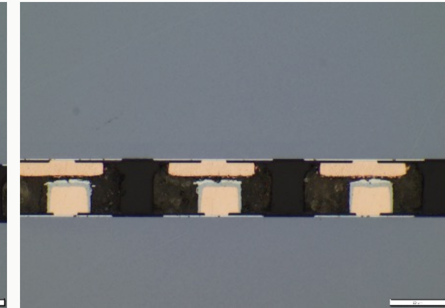


Full wafer IR image, details are to small for bond layer characterization



X-ray inspection of bonded chips: UBM pads - medium gray, pillar - dark gray; UBM and pillar are different in size





cross section after wafer to wafer bonding:
Left: slightly connected pillars, solder transfer to Cu pad (top) visible
Right: gap between pillar and pad, no solder transfer to Cu pad (top) visible

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W2W BONDING – PROCESS EVALUATION SUMMARY

Preliminary conclusions:

- Lateral dimension (x, y) of bonding structures are sufficient to handle the W2W alignment tolerances (pad-, pillar-, polymer-via diameter)
- Very narrow tolerances in z-direction: pad – pillar – polymer thickness
- Bonding strength has to be increased, investigation of source for low adhesion strength ongoing

Next steps and investigations:

- increase of polymer adhesion strength: double layer approach, pre-conditioning, …
- increase of solder amount on pillar: adjust electro-plating layer height ratio Cu-SnAg
- bonding process optimization: adjust pressure-, time-, temperature-profile of the bonding process
- Electrical measurement of daisy-chain structures of bonded chip stack (additional 80µm silicon etch of probe pad area required)

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CONCLUSIONS + NEXT STEPS

- Preparations for W2W with Timepix3 and passive CMOS sensor well progressing
  - Timepix3 wafer available and feasible for W2W bonding
  - Sensor wafer design finished and processing about to start
  - W2W bonding process setup with daisy chain at IZM well advanced but still some optimizations needed
- Next steps:
  - Finishing W2W process setup and optimization including electrical test results on daisy chain wafers
  - Processing of passive CMOS sensor wafer designed for W2W bonding with Timepix3 wafers