A Picosecond Trigger/Timing Logic Unit (TLU) for AIDAInnova

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Outline

- What is a TLU and why it is needed.
- What exists now
- Why it needs to be improved
- Possible implementation

Why a TLU?

- EUDET, AIDA, AIDA-2020 and AIDAInnova programmes aimed to provide a common interface (hardware, software) to beamline telescopes
- → Provide a TLU EUDET/AIDA/AIDA202/ AIDAInnova supported beam telescopes.
- In practice a box with trigger inputs, trigger and clock outputs and an FPGA.
  - Much value from integration with EUDAQ

Why a New TLU?

- Increasing need for more precise timing
  - (AIDA-2020 TLU has 1ns time-stamping)
- User requests for more trigger inputs
  - (Number of DUT interfaces can be increased in common clock mode using external fanout – up to 30 DUTs)
- A “PicoSecond TLU” being developed as part of the AIDAInnova programme.

Why a New TLU?

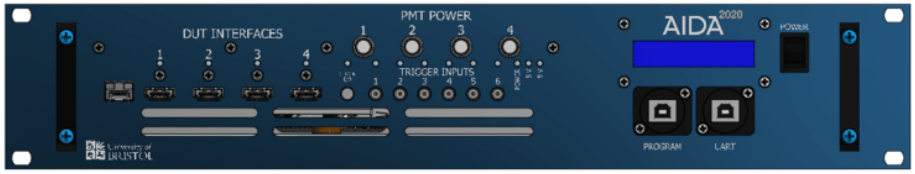
- From AIDAinnova grant agreement, part A:
  - "To provide a O (100) ps timing for particle hits, a dedicated timing layer as well as a trigger logic unit (TLU) with picosecond-timing support need to be developed, integrated and installed at both CERN and DESY. The precision timing layer will be provided by a TimePix4 plane, which will be fully integrated into the telescope hardware and the EUDAQ2 framework. We foresee having such planes available at all beam lines. To provide an ultimate timing resolution of 30 ps, an LGAD plane based on current developments for the HL-LHC will be included in the EUDET-style pixel telescopes. In order to benefit from this exquisite timing, the TLU needs to provide a stable clock with a 10 ps or better stable edge, which will be part of the AIDA TLU upgrade."
- NIKHEF/Nikhef, UNIVBRIS, CSIC-IFCA, DESY,UCL, USC

Picosecond TLU

AIDA-2020 TLU connected to beam telescope

- Timing specification:
  - Clock jitter < 10ps RMS
  - Timing-stamping of input signals O(10ps) RMS
- Backwards compatible with AIDA-2020 TLU
  - Same signals on DUT connections
    - trigger/busy/DUT-clk in EUDET-mode
    - Global-clk, trigger, busy, shutter, T0 in common-clock mode

Picosecond TLU - I/O



- Trigger inputs
  - Probably 8
    - (c.f. 6 for AIDA-2020 TLU)
  - CFD and/or ADC for time-walk correction
    - (c.f. threshold discriminator in AIDA-2020 TLU)
  - TDC with O(10ps) bins
    - Either implemented in FPGA or external PicoTDC (3ps bins)
  - Aim to contribute less to timing uncertainly than detector.
- Device Under Test (DUT) connectors
  - Compatible signal definitions as AIDA-2020 (also LVDS)
  - Move to “Display Port” from HDMI
    - Mechanically more robust.
    - Five good quality differential pairs (c.f. 4 in HDMI)
    - Passive adaptor to HDMI if needed
    - Opinions?

PicosecondTLU - Rate Capability

- Same goal for rate capability as AIDA-2020 TLU:
  - Instantaneous rate ~ 10MHz:
    - 50ns between hits (little pile up at 10MHits/s)
- Sustained rate ~ 1MHz
  - Internal buffer in current AIDA-2020 TLU only 4k events.
    - Aiming to expand to O(10M events)

Picosecond TLU - Optical Interface

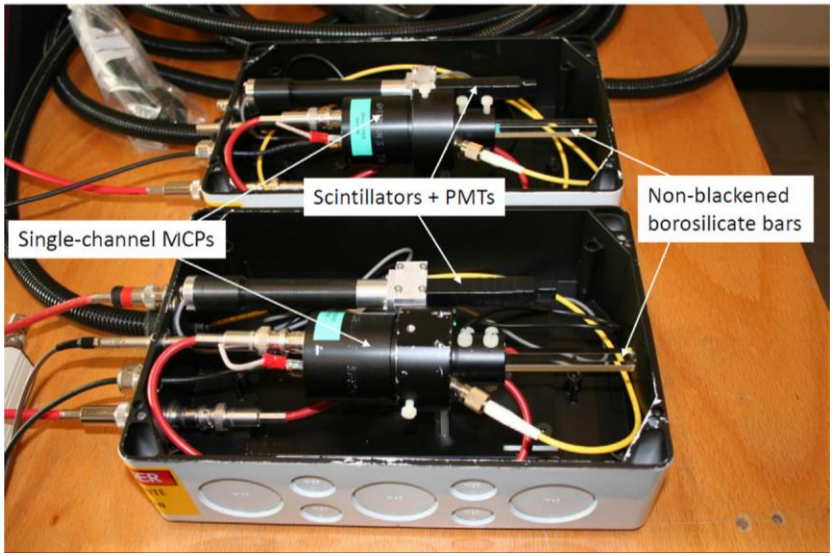
- Retain optical interface introduced in AIDA-2020 TLU
  - Can distribute timing information over fibre
  - Used for ProtoDUNE-SP
    - https://doi.org/10.1016/j.nima.2019.04.097
  - fibre bandwidth much larger than copper cable.
    - Possibility of more precise timing over longer distances
      - Clock jitter (endpoint w.r.t. master) of 12ps measured

Picosecond TLU - Timing reference

- Testing pico-second detectors requires pico-second time reference
  - TLU timing only as good as reference
- Some beam-line users will bring their own time reference detectors. Some would benefit from precise time reference at beam-line.
  - (Providing timing reference not part of WP3.3)
- Could use, e.g. Cherenkov light and high speed photo-detector
  - Used for “TORCH” LHCb upgrade beam-tests
  - MCP-PMT single photon jitter 66ps FWHM
    http://www.photek.co.uk/pdf/datasheets/detectors/DS006%20Photomultiplier%20Tube%20Datasheet%20issue%202.pdf
  - Many photons --> timing precision ~ 10ps

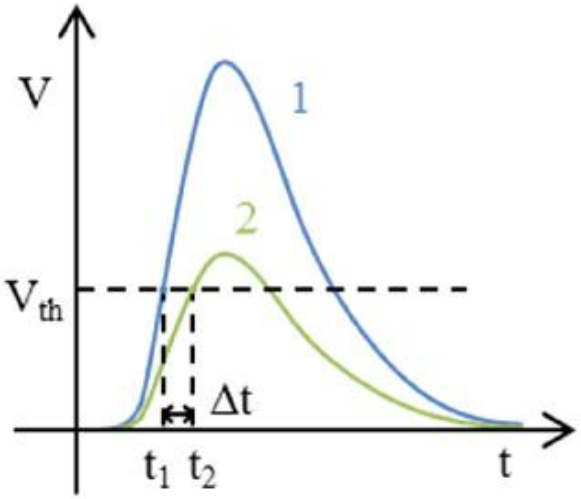
Bare MCP-PMT module
(photo-cathode facing down)

Taken from
http://dx.doi.org/10.1016/j.nima.2016.06.087

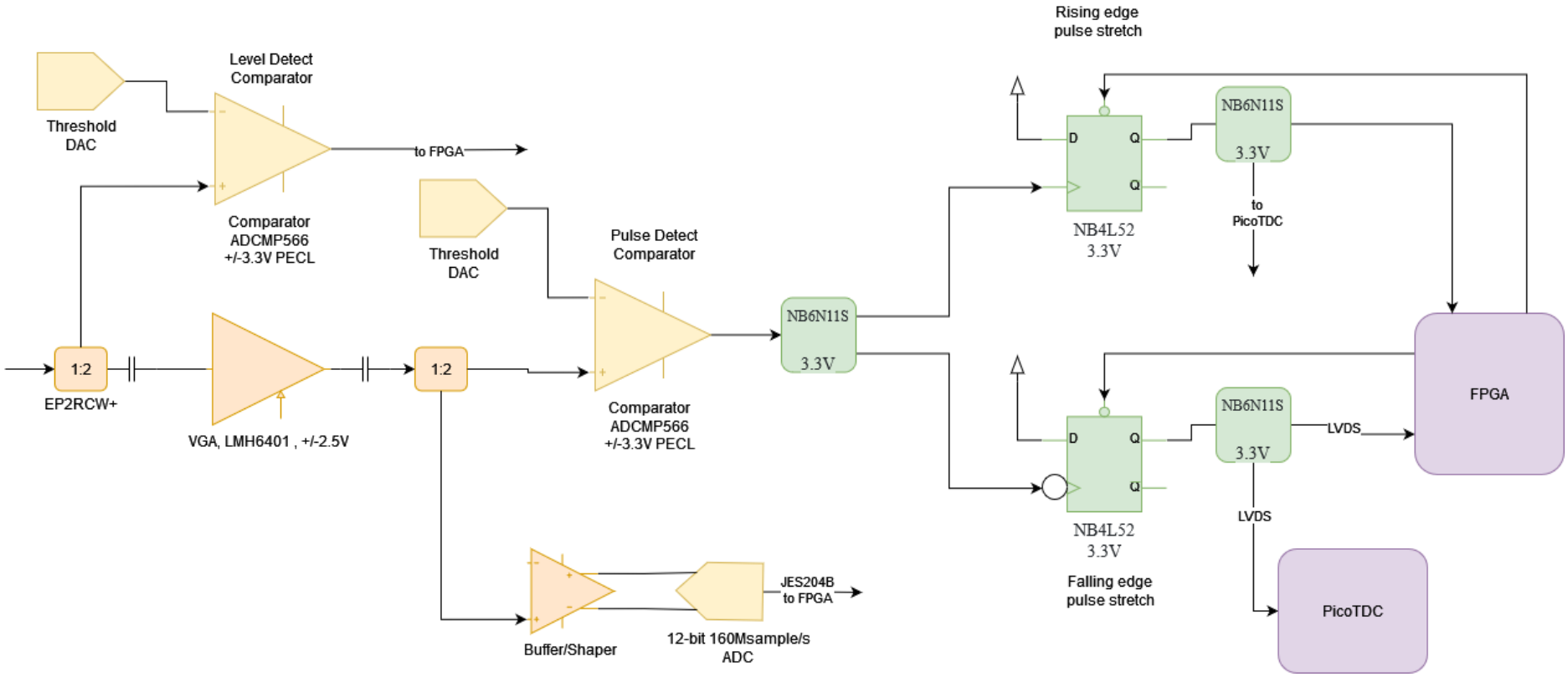


Trigger Inputs

- Prototyping analogue part:
- Two comparators:
- DC-coupled for level detection
- AC-coupled with variable gain amplifier for (possibly small) pulses. Combine threshold comparator with 160MSample/s ADC for time-walk correction
- Pulse stretching on rising and falling edges.
- CERN PicoTDC ASIC for time-stamping (investigating carry-chain TDC in FPGA)
- Optimizing timing resolution for small amplitude fast rise signals.
- Use case: single-anode MCP-PMT used as a timing detector



Trigger Inputs



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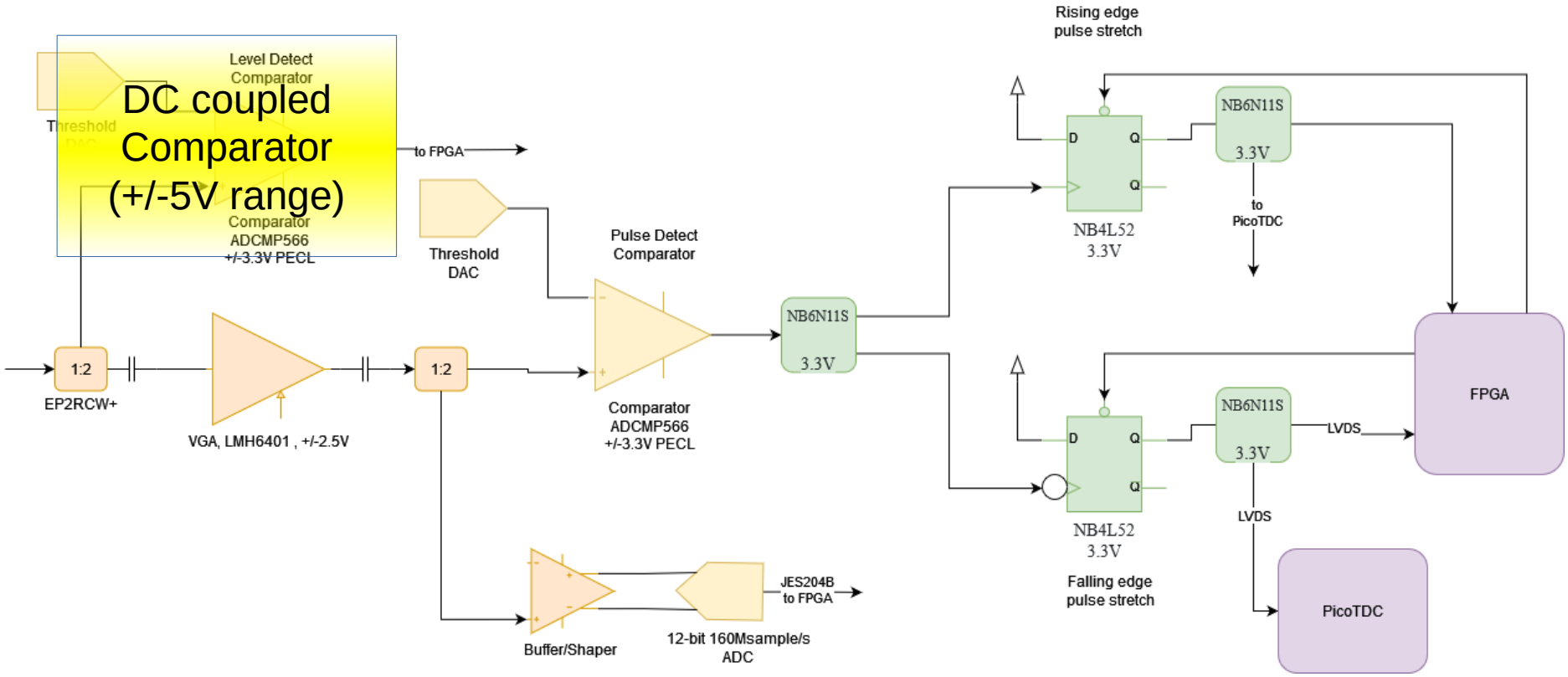

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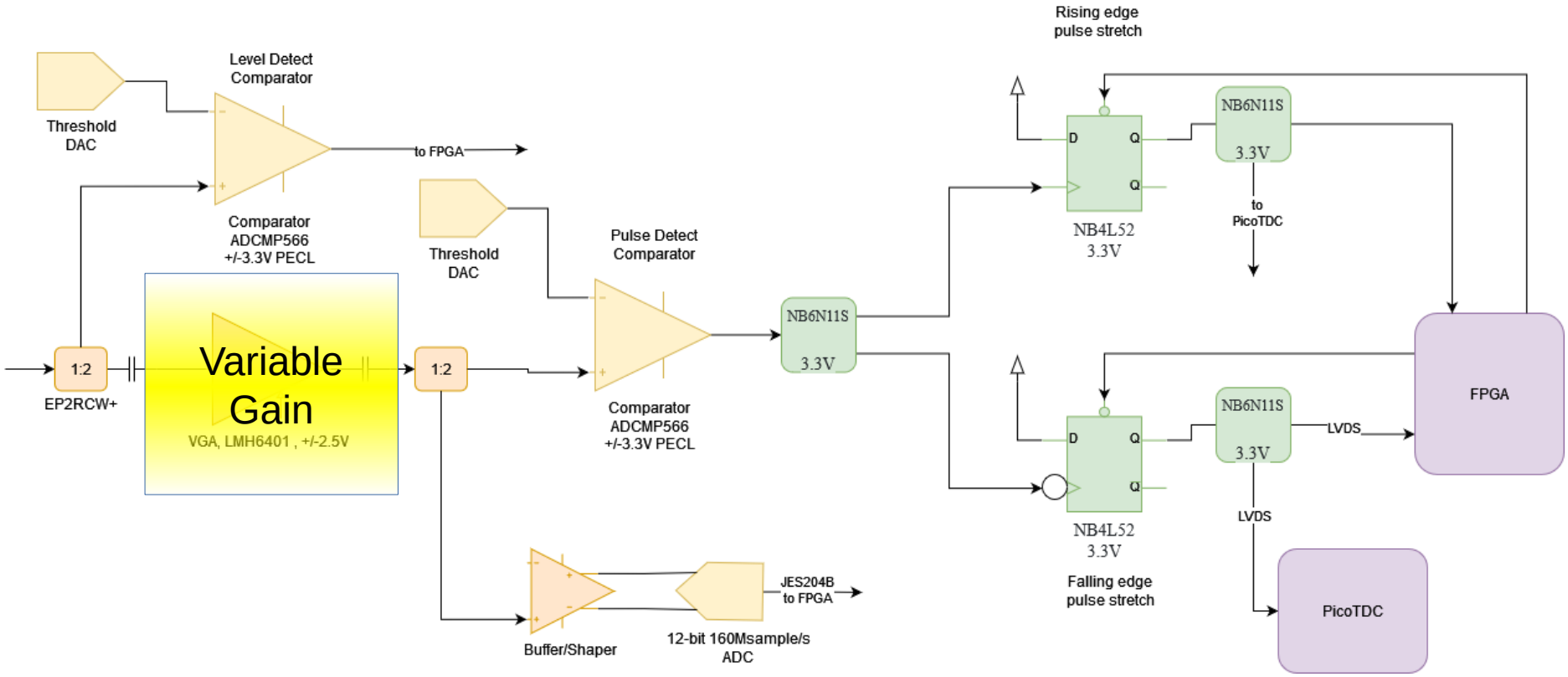

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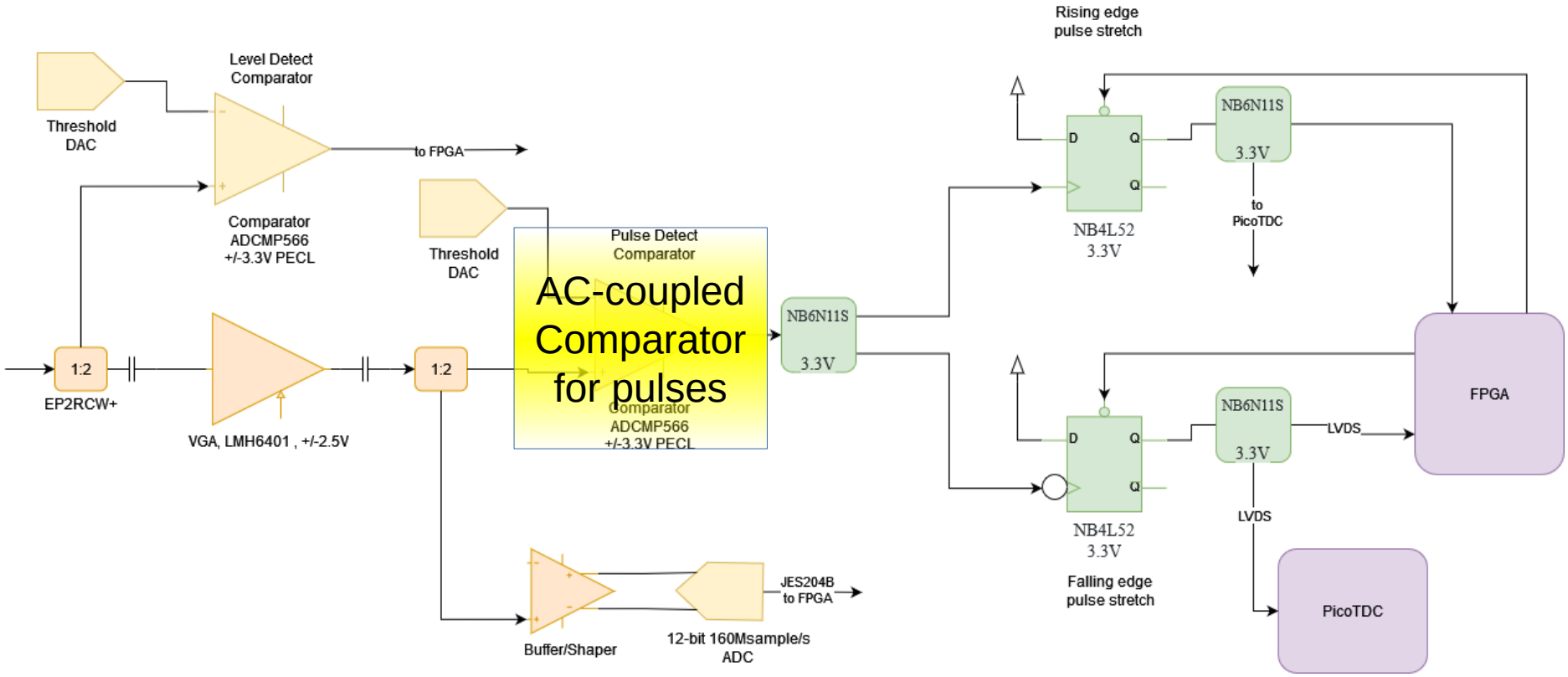

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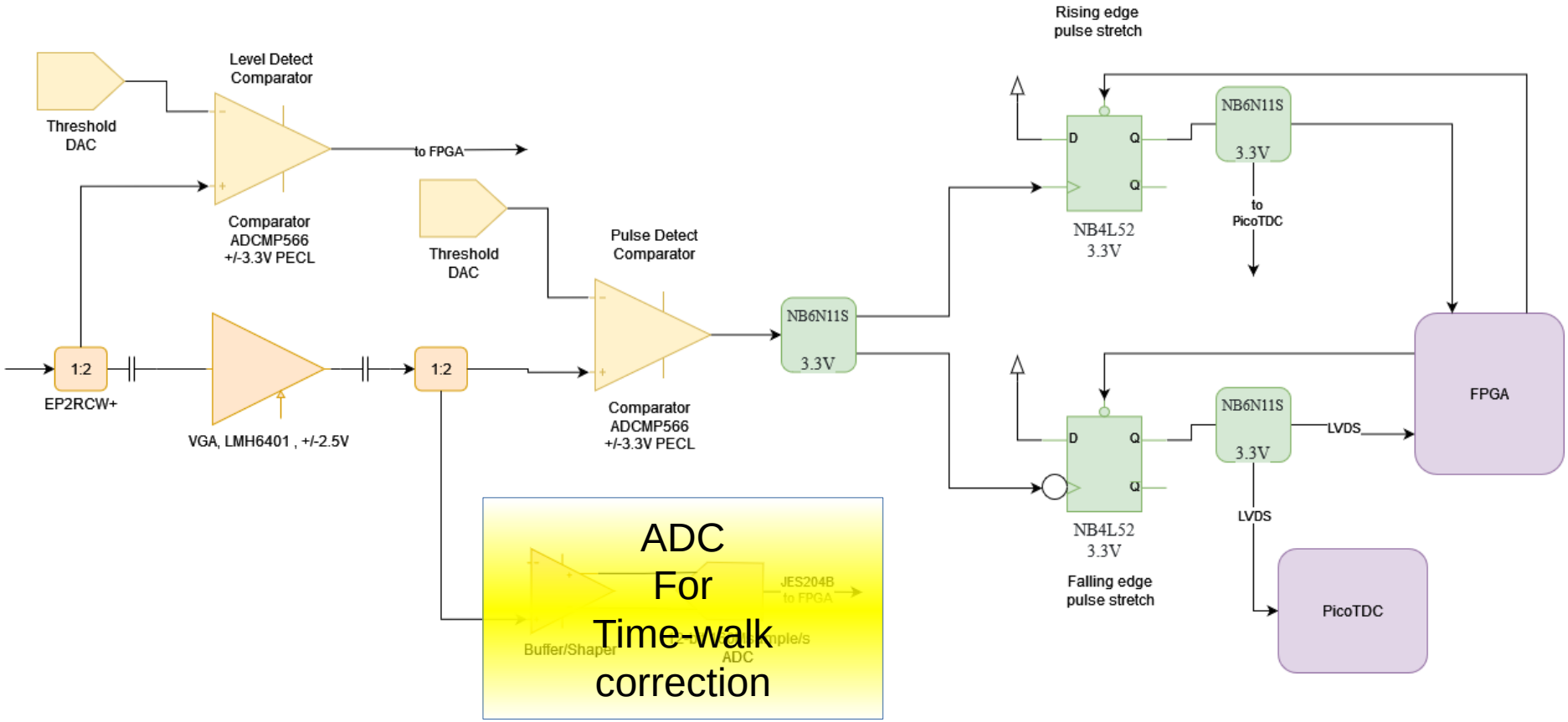

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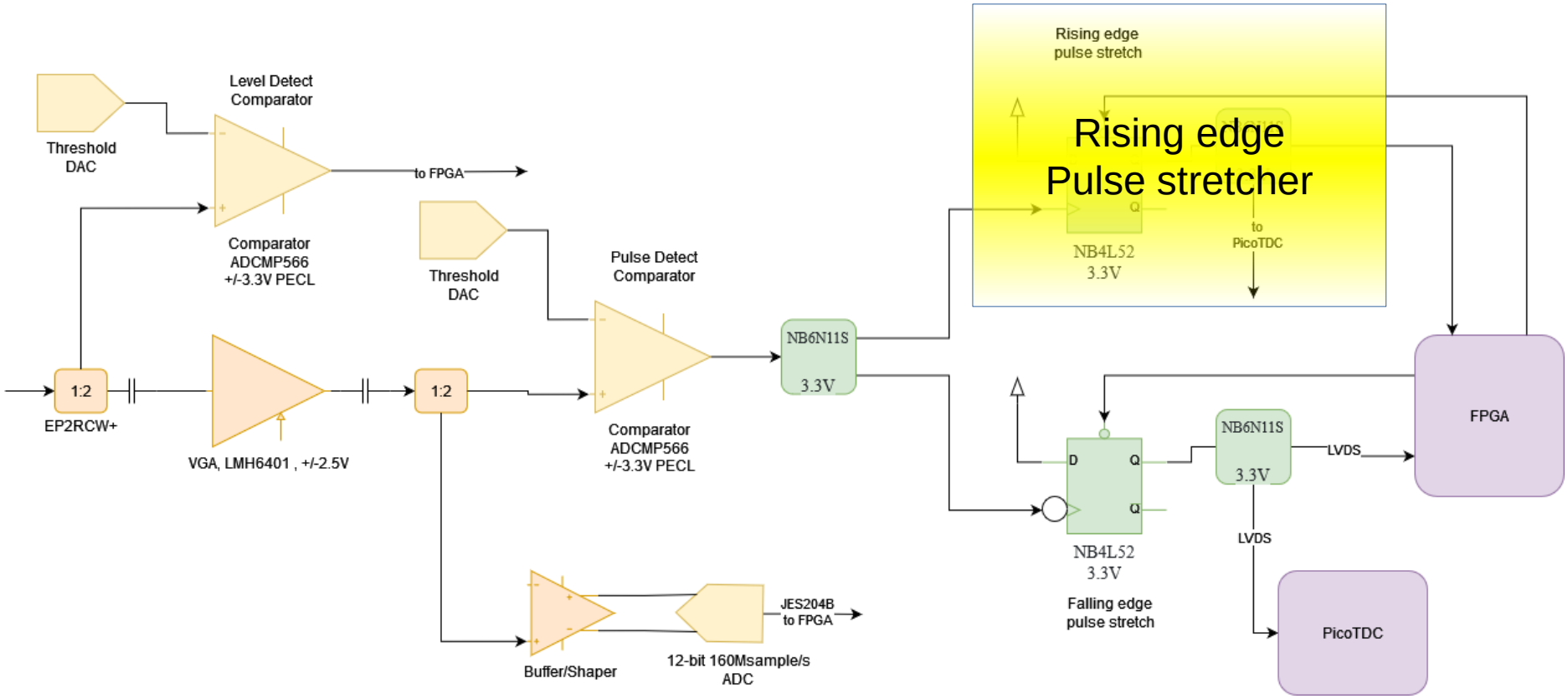

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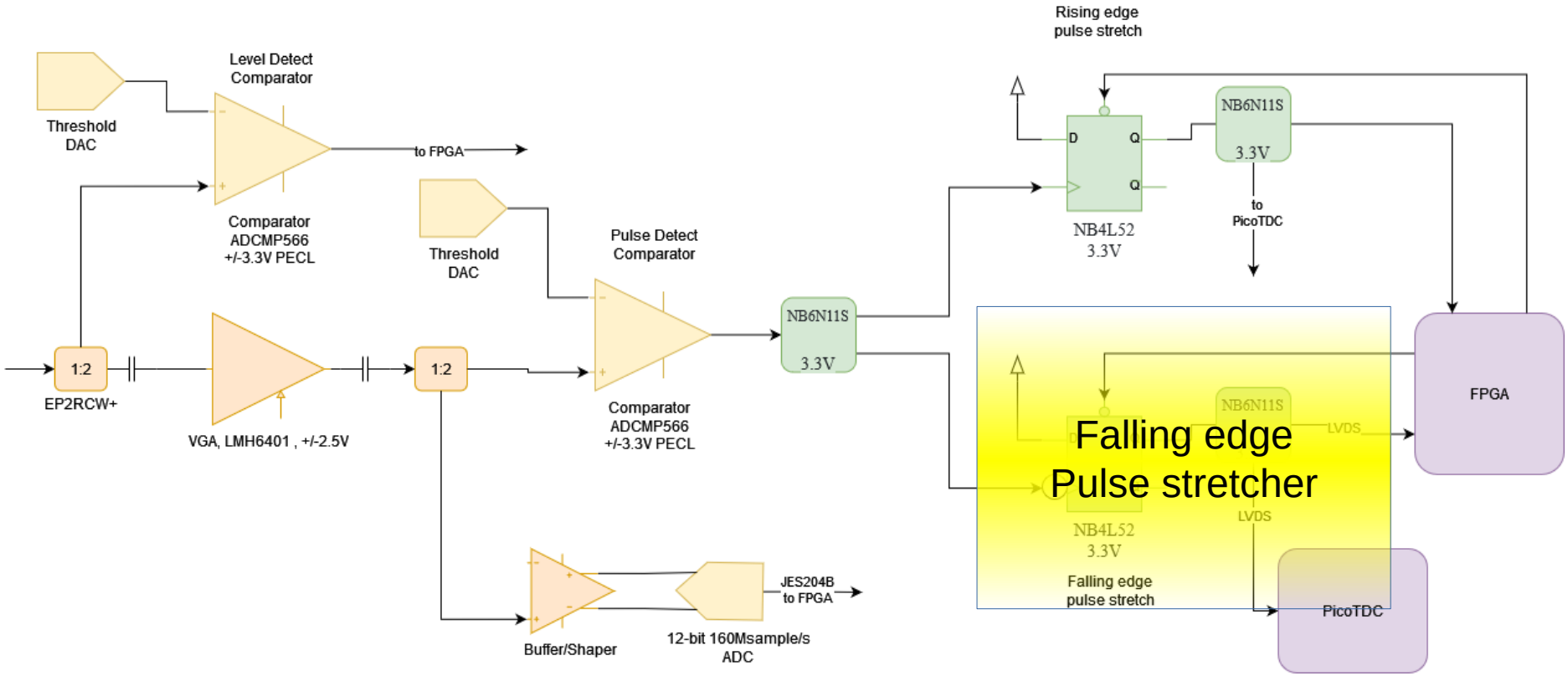

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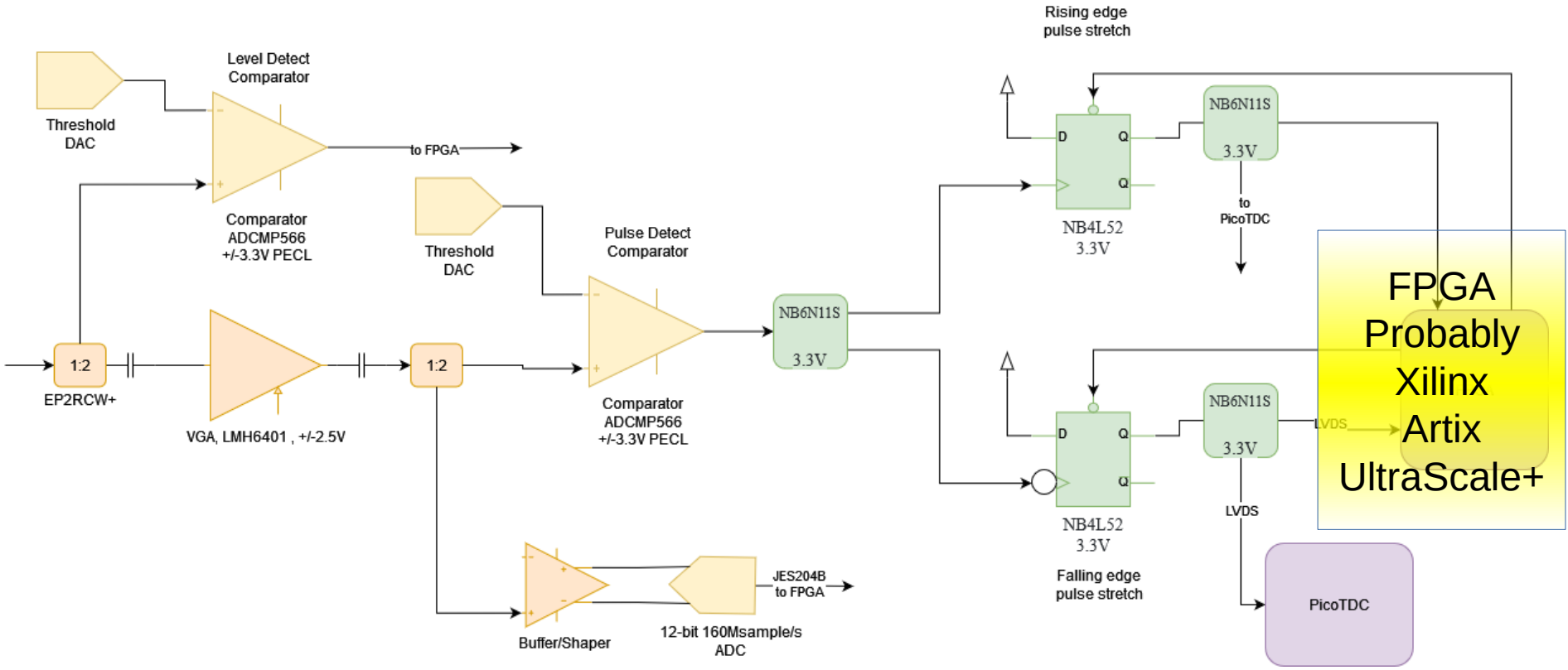


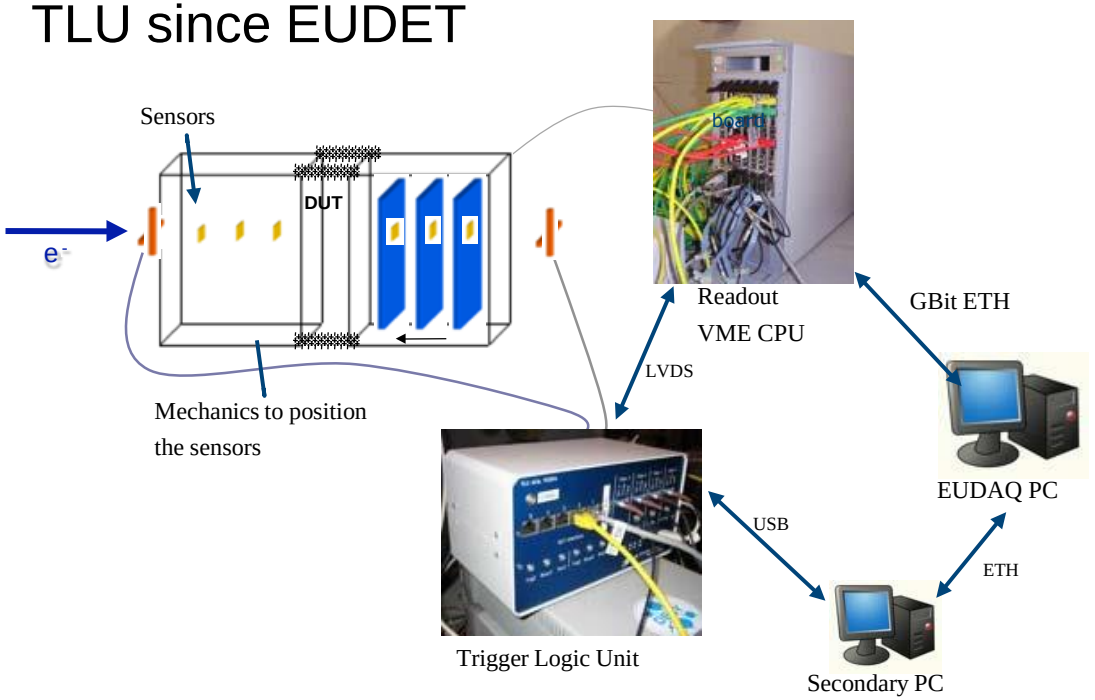
Summary

- The AIDA(-2020/Innova) TLU provides a common hardware and software interface to beamlines
- Pico-second detectors need pico-second infrastructure
  - AIDAInnova Aiming for < 100ps timing
- AIDA-Innova TLU backwards compatible at the hardware signal level with EUDET / AIDA-2020 / AIDA TLU
  - Needs passive adaptor for RJ45 , HDMI
  - Data format different – will be “hidden” by EUDAQ

Backup

Why?

- Beam Telescope with “Detector Under Test”
  - Need to correlate data from a single particle in all detectors
  - Match tracks in telescope with hits in your DUT
  - TLU since EUDET



From: Infrastructure for Detector Research and Development towards the International Linear Collider. https://arxiv.org/abs/1201.4657

This project has received funding from the European Union’s Horizon 2020 research and innovation programme under grant agreement No 654168.

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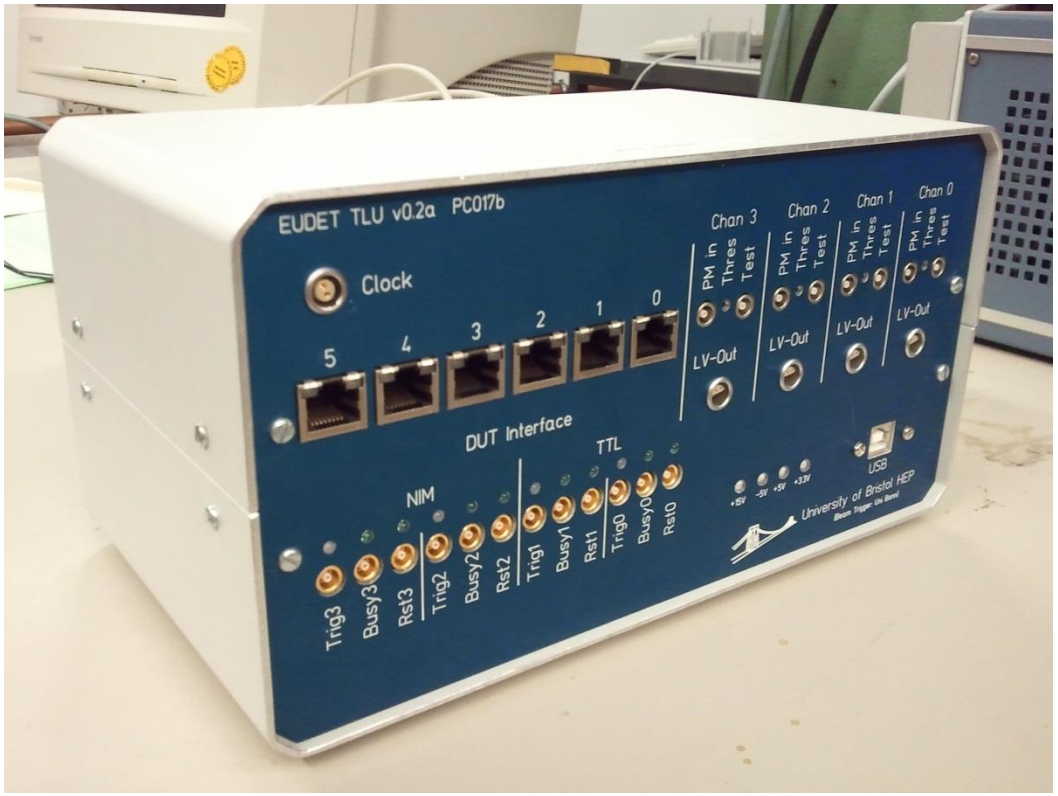
How?

- Sensors in beam to detect passage of particles.
  - Electrical signals conditioning binary signal
- Combine binary signals from one or more beam sensor to produce a “trigger”
- Two choices:
  - Distribute a trigger signal to beam telescope and DUT readout systems.
    - Correlate data based on trigger number
  - Distribute central clock/time-stamp to beam telescope and DUT
    - Correlate based on timestamps.
  - … can mix time-stamping and triggering: TLU records both trigger-number and time-stamp
- Implementation: Box with signal conditioning and an FPGA
- Make available to use in home labs – ease integration at beam-line

History - EUDET

- EUDET TLU
  - Supporting beam tests for linear collider detector development at DESY
    - Low rate (< 10kHz)
    - Modest time precision
    - RJ45 for trigger/busy
      - LVDS
  - See https://www.eudet.org/e26/e28/e42441/e57298/EUDET-MEMO-2009-04.pdf
  - Many still in beam-lines and HEP institutes



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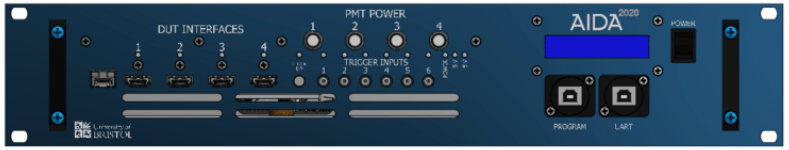
History - AIDA-2020

- Current production version
- 6 trigger inputs
- 4 DUT connections
  - LVDS on HDMI
    - But direction of each line can be swapped in hardware to allow different firmware mapping
- Low jitter clock
- Hardware permits optical distribution of clock/trigger
- In small desktop case or rack-mount case



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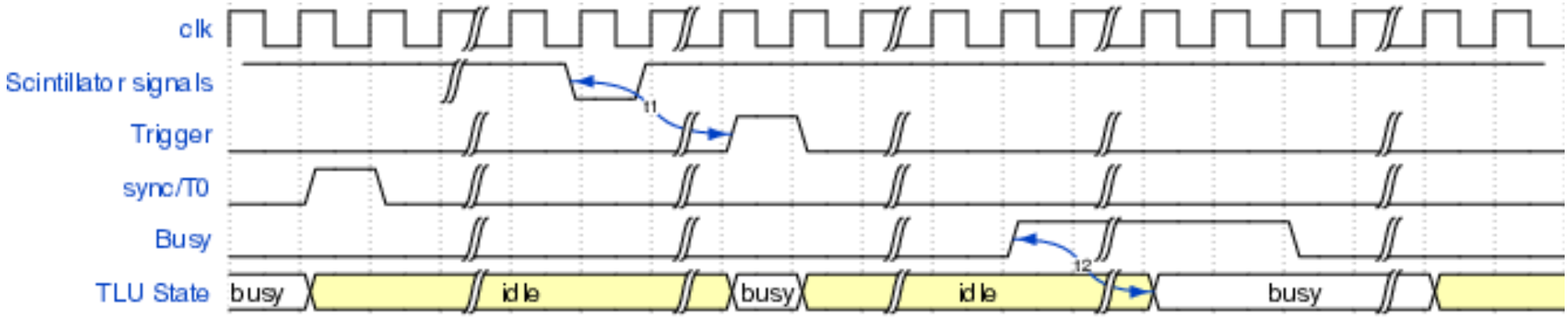
AIDA-2020 TLU – DUT Interfaces

- Two interface mode between TLU and DUT:
  - “EUDET mode”
    - No common clock between TLU and DUT.
    - Trigger/Busy handshake
    - DUT can read out trigger number from TLU – event-by-event checking
- Common clock
  - Permits higher trigger rate
    - No event-by-event handshake. Cross-check on trigger timestamps.



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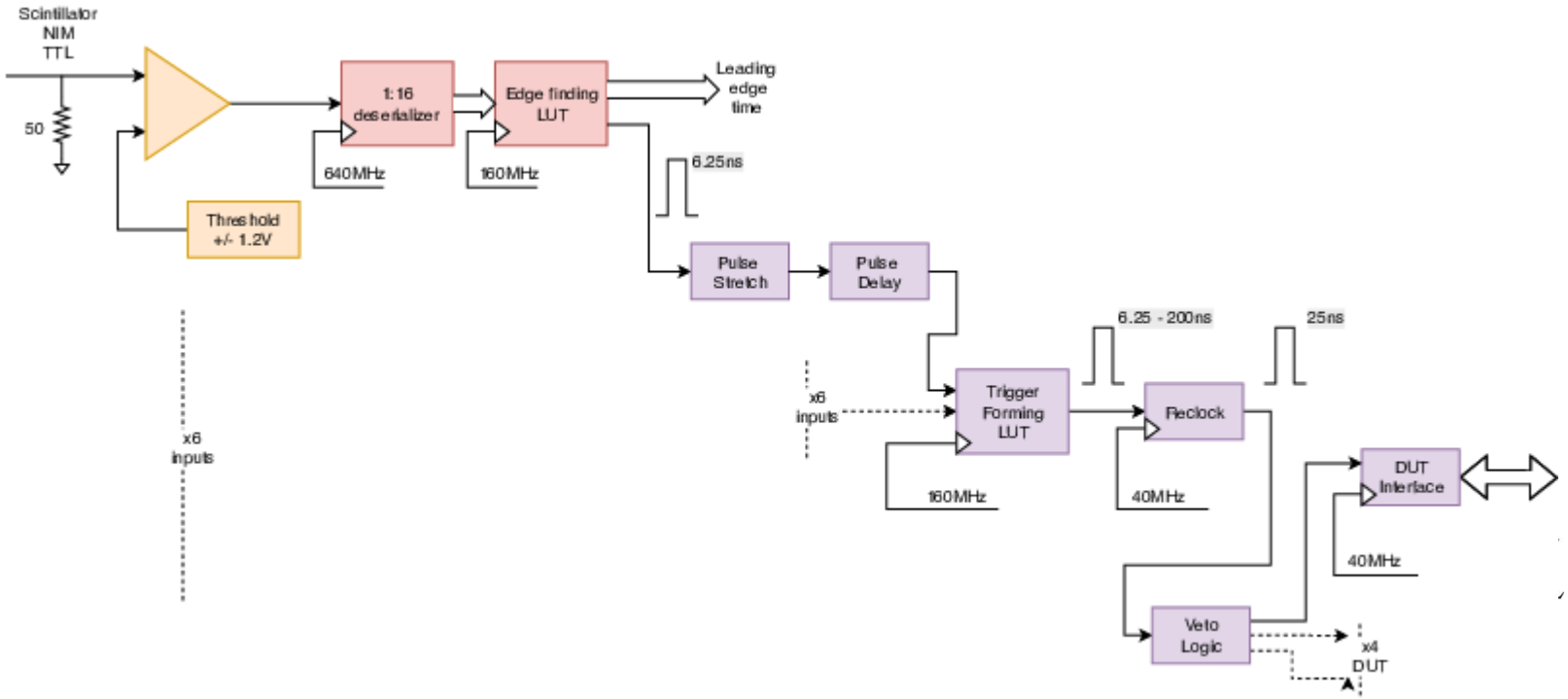
Trigger Logic

- Inputs clocked at 160MHz (nominal)
- Input signals can be delayed and/or stretched in units of 1/160MHz
- Signals from the 6 inputs fed into a look-up table
- LUT programmed with which combinations produce a trigger
- Trigger output moved to clock fed to DUT (40MHz nominal)
- State of all inputs recorded at point that trigger “fires”
  - Can be used to tag events – e.g. Cherenkov information.



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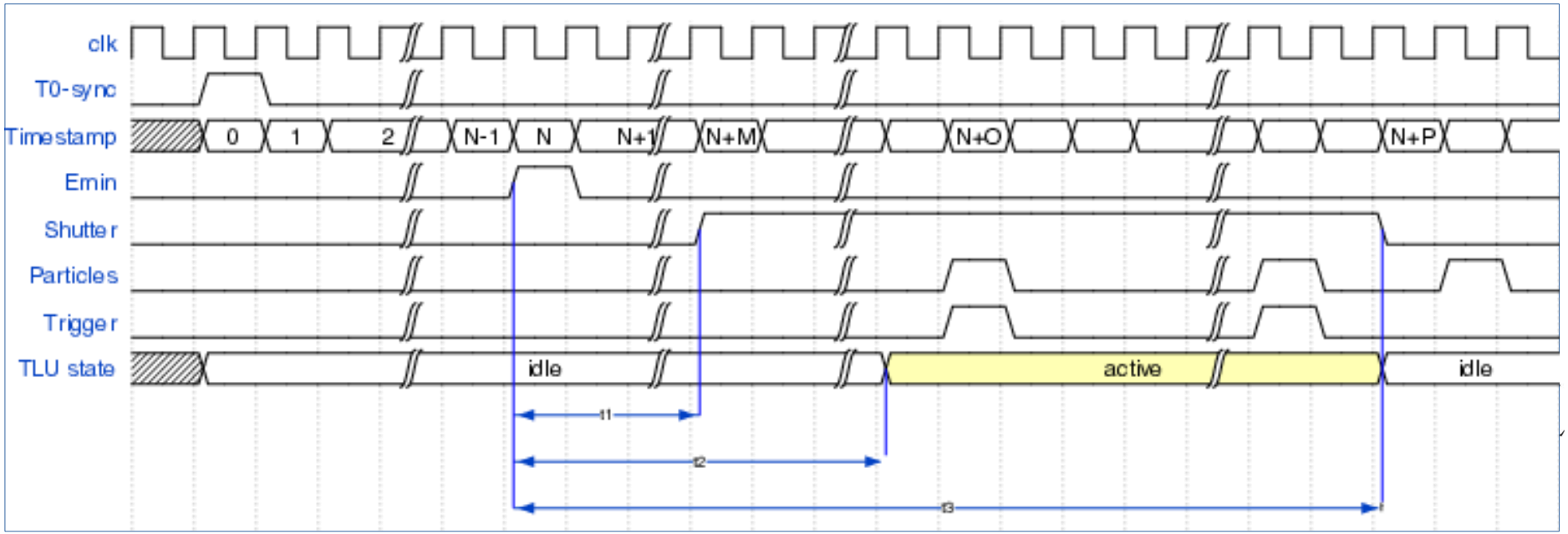
AIDA-2020 TLU DUT “Shutter”

- Some detectors can only capture data with a low duty cycle
- In many beam-lines particle are only present a certain times
  - DESY – 50Hz cycle
  - CERN – SPS cycle
- Detectors active period should occur when particles are present
- → Signal from accelerator can be used to generate a “shutter” signal sent to DUT



Documentation

- https://doi.org/10.1088/1748-0221/14/09/p09019 "The AIDA-2020 TLU: a flexible trigger logic unit for test beam facilities" , JINST
- Open Hardware project "AIDA-2020 TLU"
  - https://ohwr.org/project/fmc-mtlu
  - Hardware design files https://ohwr.org/project/fmc-mtlu-hw/
  - Firmware source code https://ohwr.org/project/fmc-mtlu-fw/
- User manual https://ohwr.org/project/fmc-mtlu/blob/master/Documentation/Main_TLU.pdf

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Firmware

- IPBus for control and readout of time-stamps
  - UDP/IP 1 Gbit/s Ethernet
- Ipbb build system
  - Scriptable build. Working on CI
- Open Source
  - https://ohwr.org/project/fmc-mtlu-fw/

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Software

- All versions of TLU integrated with EUDAQ DAQ software.
  - Run control
    - Configuration
    - Monitoring
  - Readout of trigger timestamps

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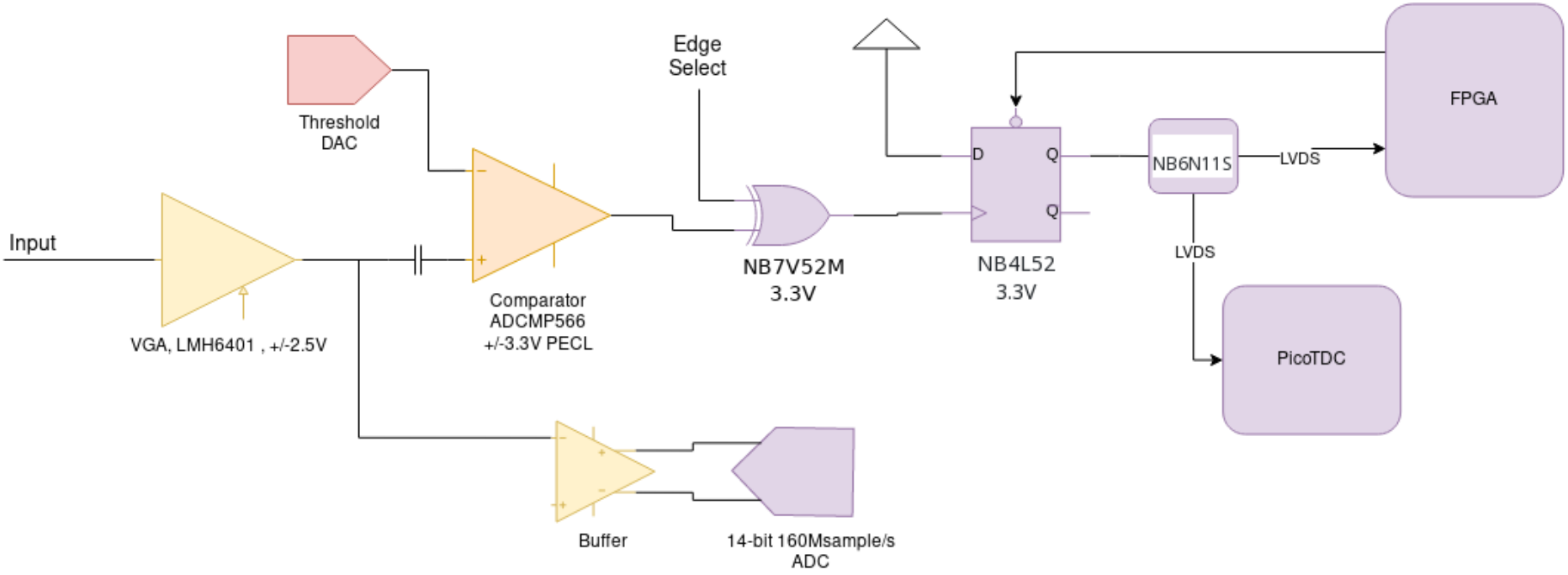
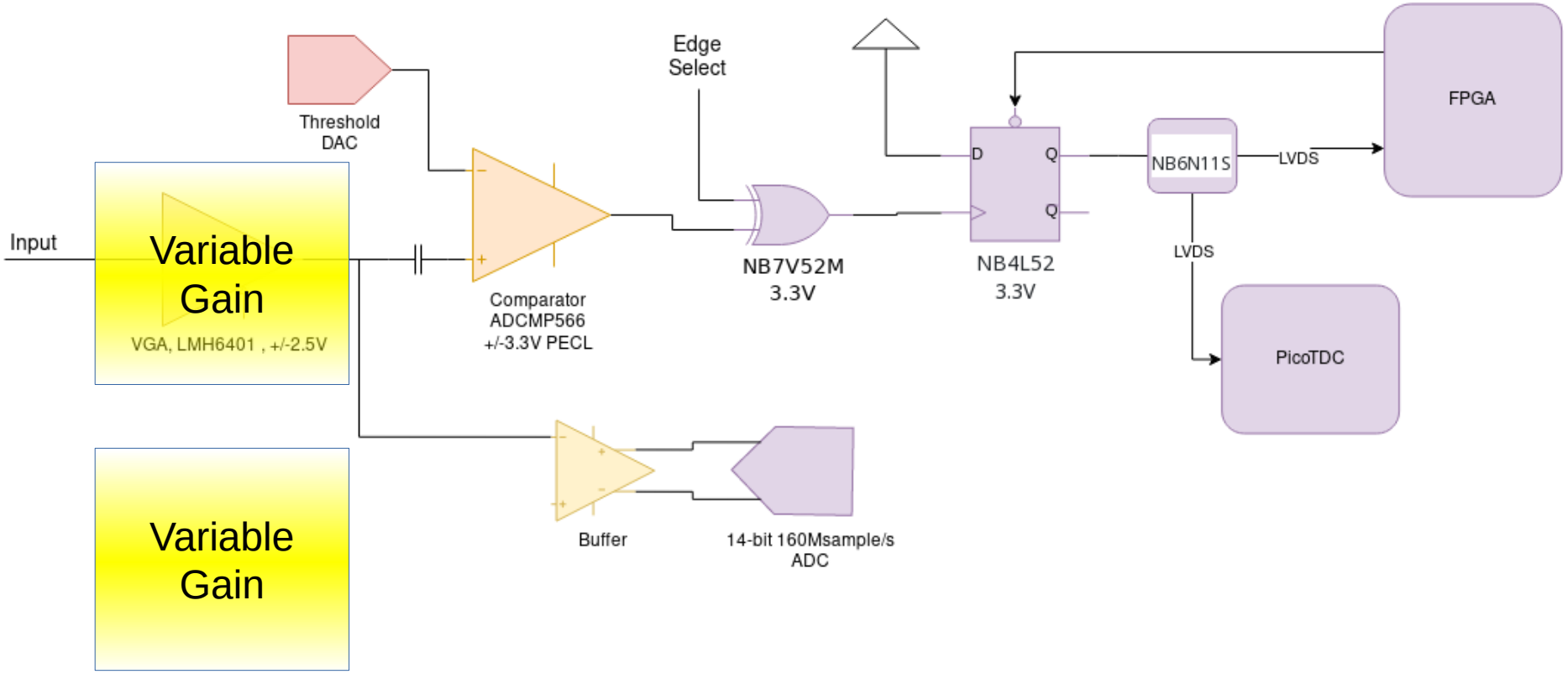
Trigger Inputs (Superseded)



Trigger Inputs



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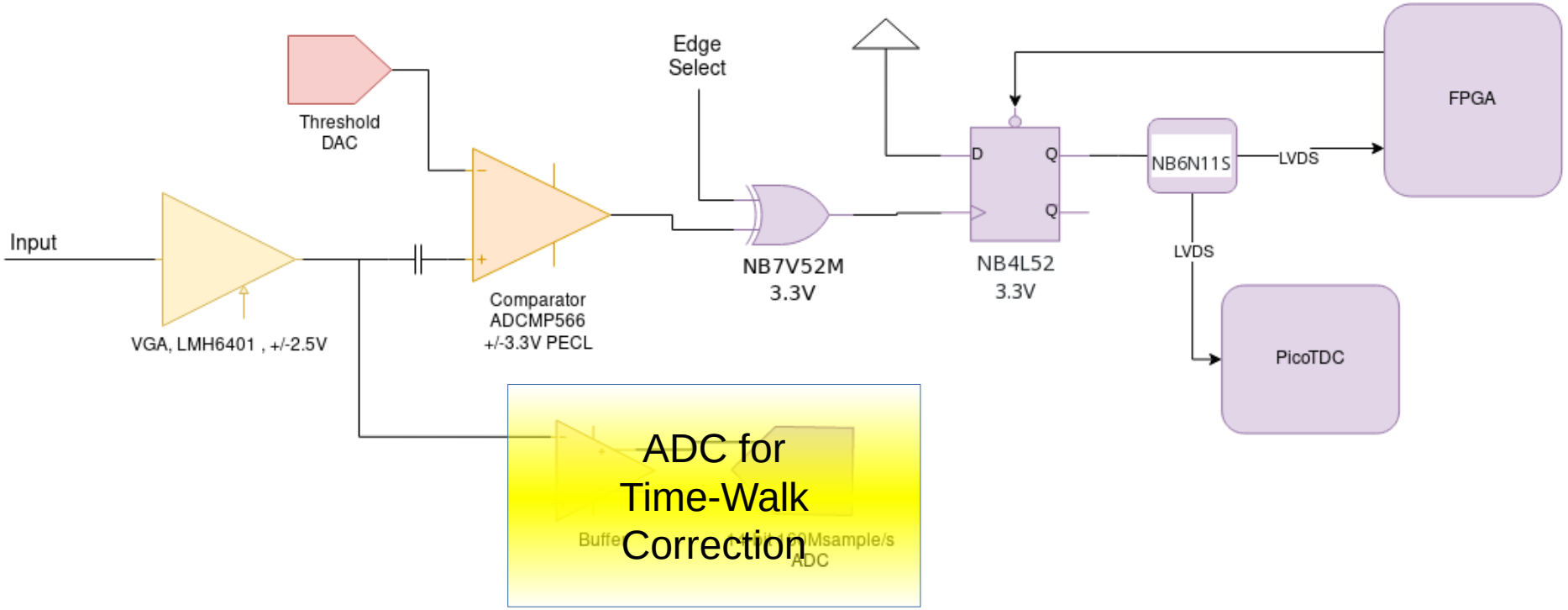

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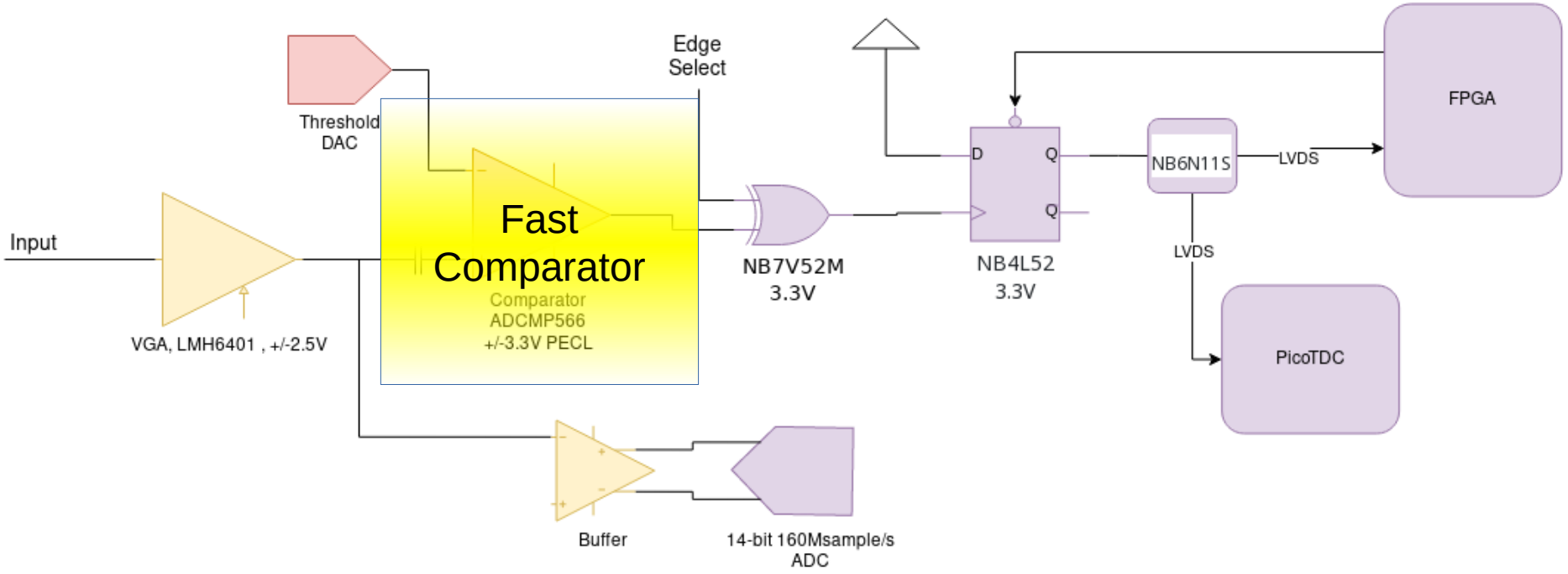

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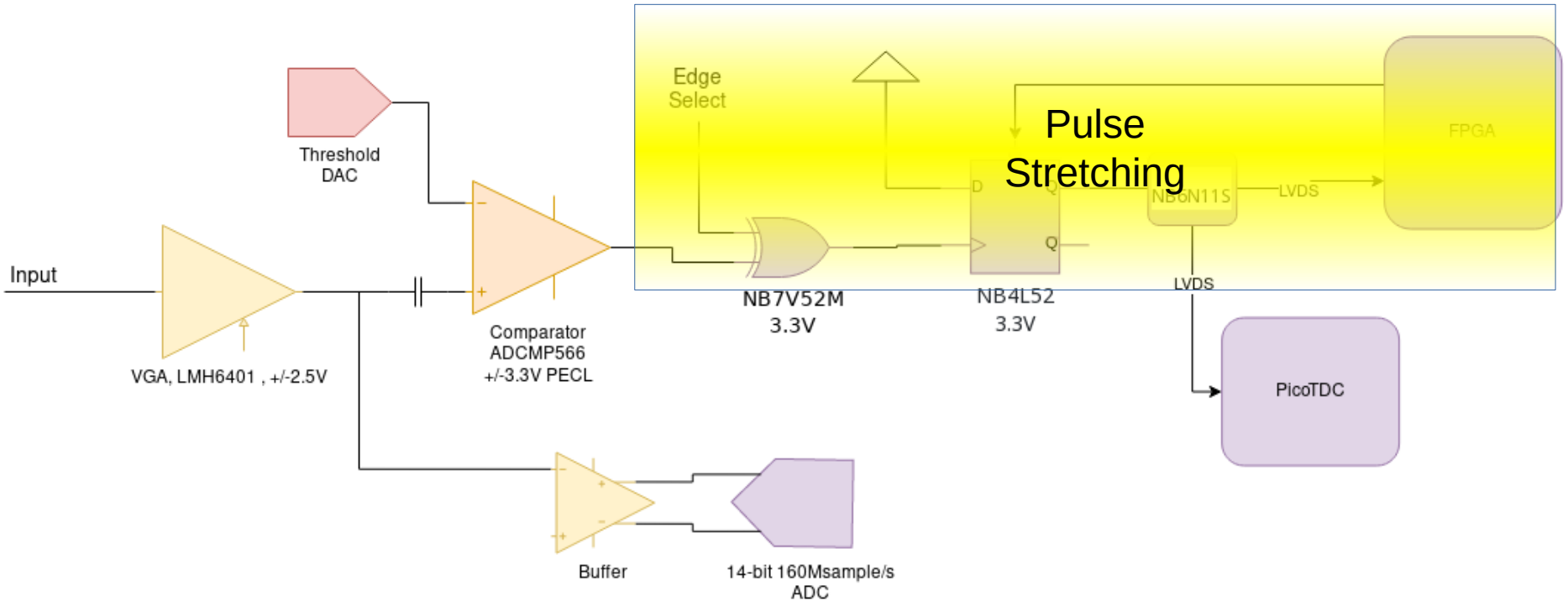

Trigger Inputs