OMEGA contribution in WP 11.3

AIDAinnova

Damien Thienpont

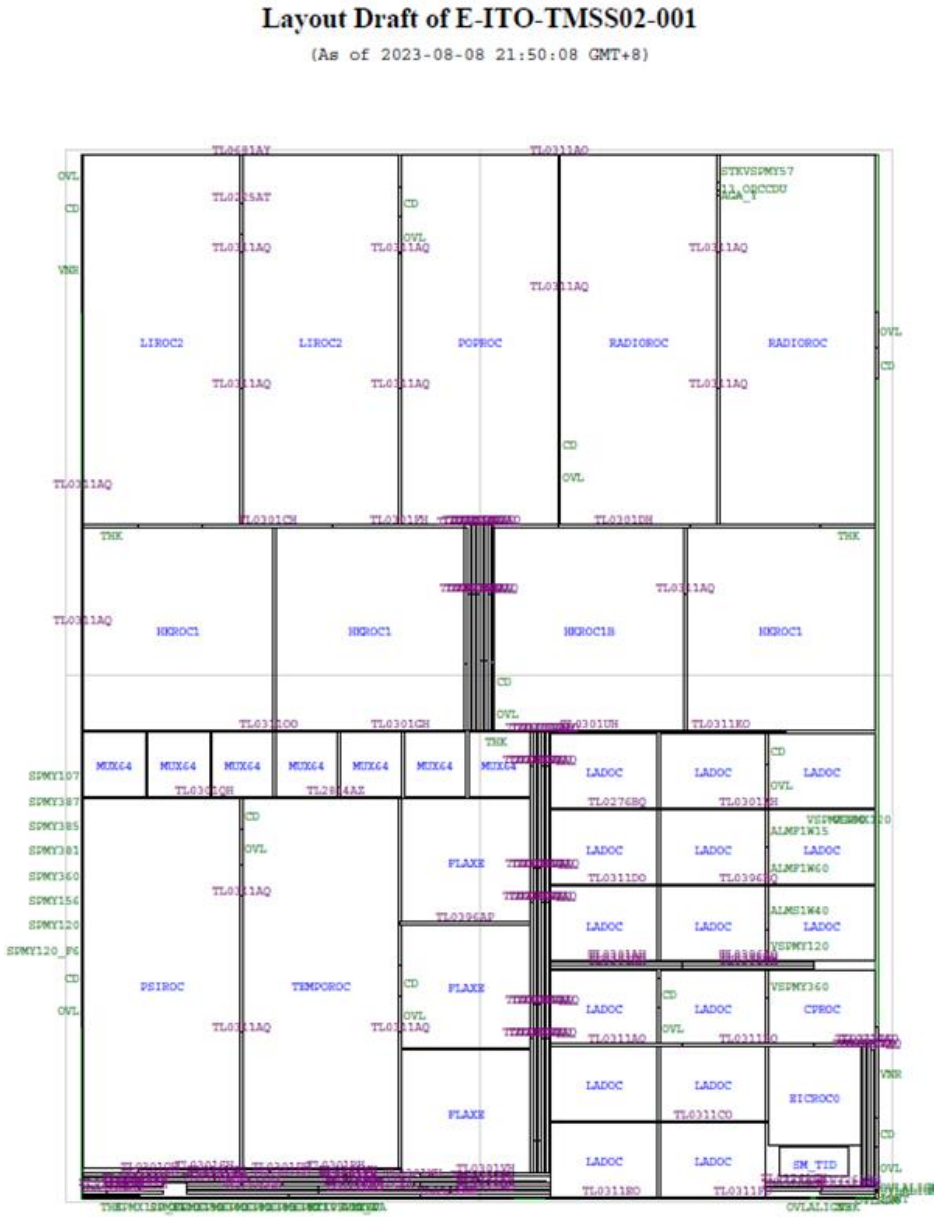
March 18, 2024

Organization for Micro-Electronics desiGn and Applications

Engineering run submitted in April 2023

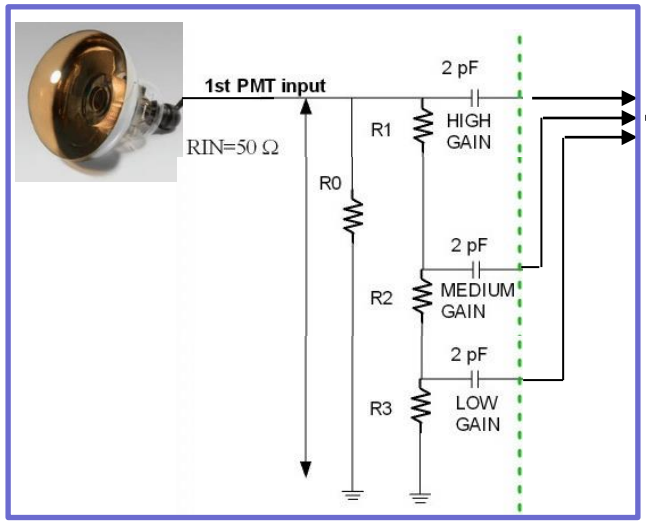
- TSMC 130 nm
- 10 chips have been submitted
  - From OMEGA, AGH, IJCLAB, WEEROC
  - C4 (16 wafers) and WB (4 wafers), 90 chips/wafer
  - In fab at TSMC in November 2023 only!
    - New reticle requirement from TSMC, DRC violations, …
  - Wafers received last month, presently in packaging
- HKROC1B, EICROC0 and CPROC

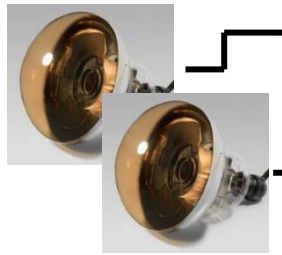
chip	x	y		lab
HKROC1B	5,96	6,16	C4	OMEGA
LADOC2B	3,243	2,142	WB	IJCLAB
LIROC2	11,244	4,919	C4	OMEGA
POPROC	11,244	4,919	C4	WEEROC
PSIROC	11,244	4,919	C4	WEEROC
RADIOROC2	11,244	4,919	C4	WEEROC
TEMPOROC2	11,244	4,919	C4	WEEROC
FLAXE	4,02	3,7	WB	AGH
EICROC0	2,89	3	WB	OMEGA
CPROC	3,243	2,142	WB	OMEGA
Total				

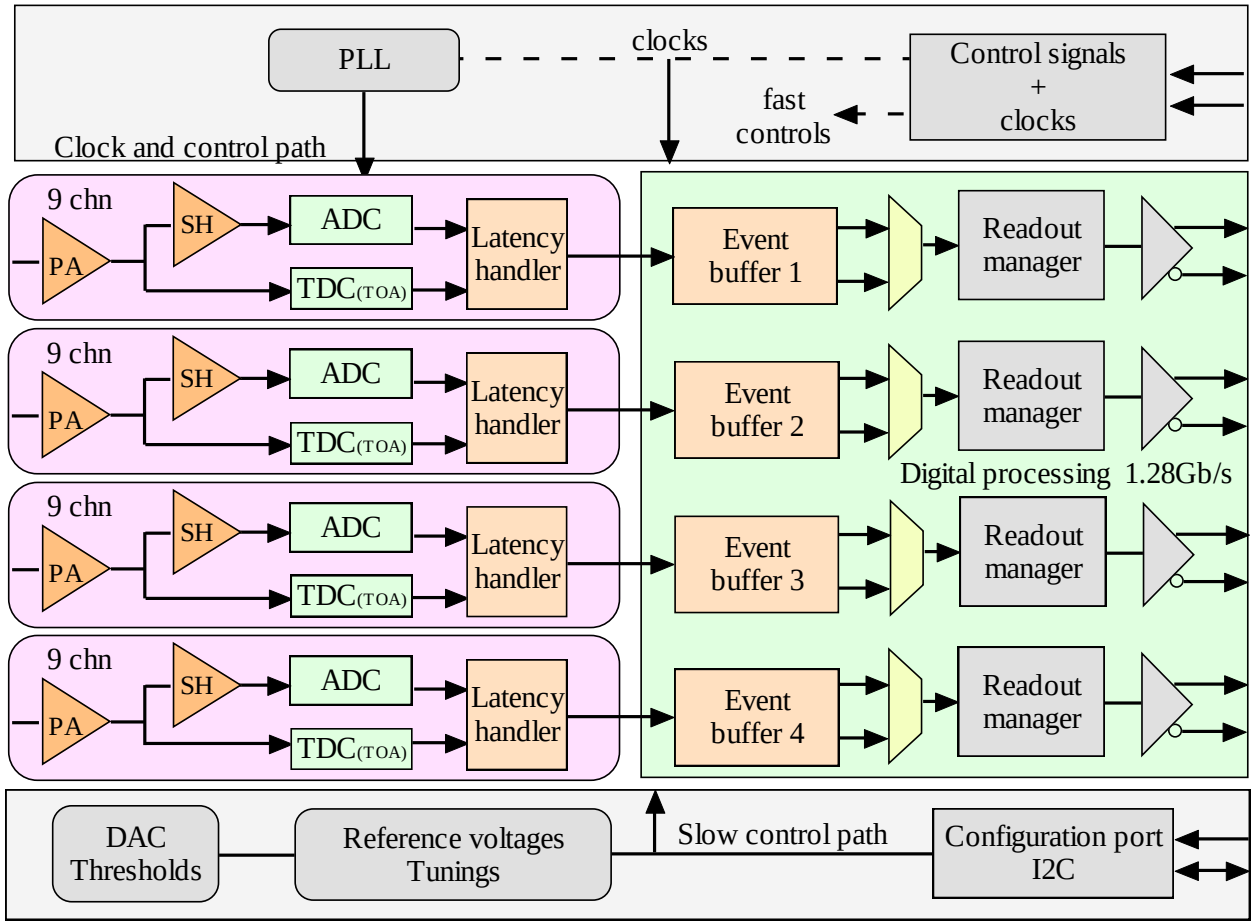


HKROC main features

- HKROC has 36 channels: 12 PMTs with High, Medium and Low gain
  - Or 36 PMTs with one gain



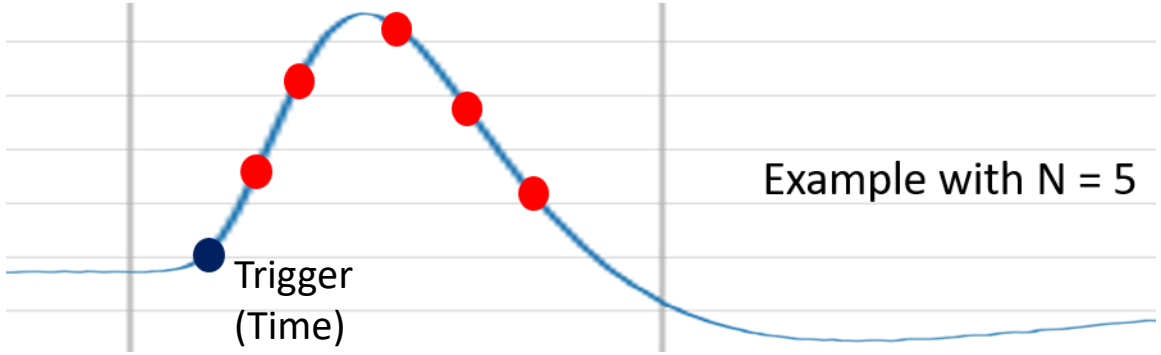




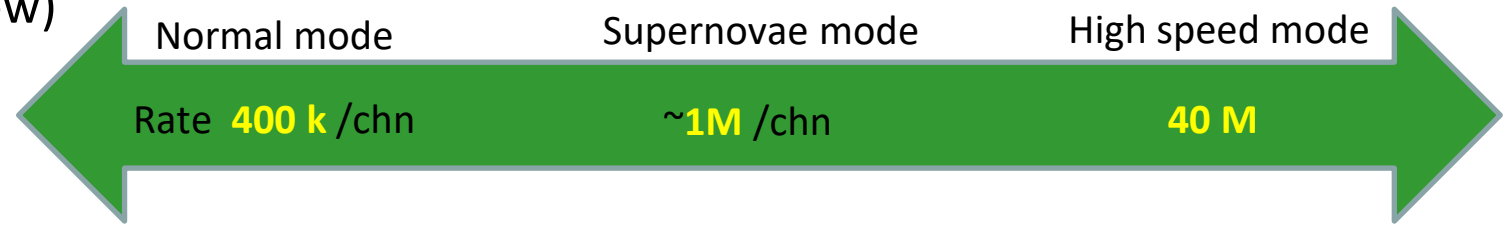
- ASIC in TSMC 130 nm node
- Low power: 10 mW per channel
- Large charge measurement with 3 gains (up to 2500 pC), < 1% linearity
- Integrated timing measurements (25 ps binning)
- Readout with high speed links (1,28 Gb/s), Hit rate up to ~40 MHz
- HKROC is a waveform digitizer with auto-trigger

HKROC: waveform digitizer with auto-trigger

- HKROC is waveform digitizer working @ 40 MHz
  - Number of charge sampling points from 1 to 7
  - Fast channel for precise timing (25 ps binning)
  - Charge reconstruction algorithm in FPGA
    - 5% resources of a modern XILINX FPGA



- When using 3 gains / PMT (high, medium, low)
  - Hit rate capability up to 400 kHz / PMT
  - Increased up up to 1 MHz by focusing on high gain
    - Dynamic selectable by the user
  - Average values only limited by readout speed



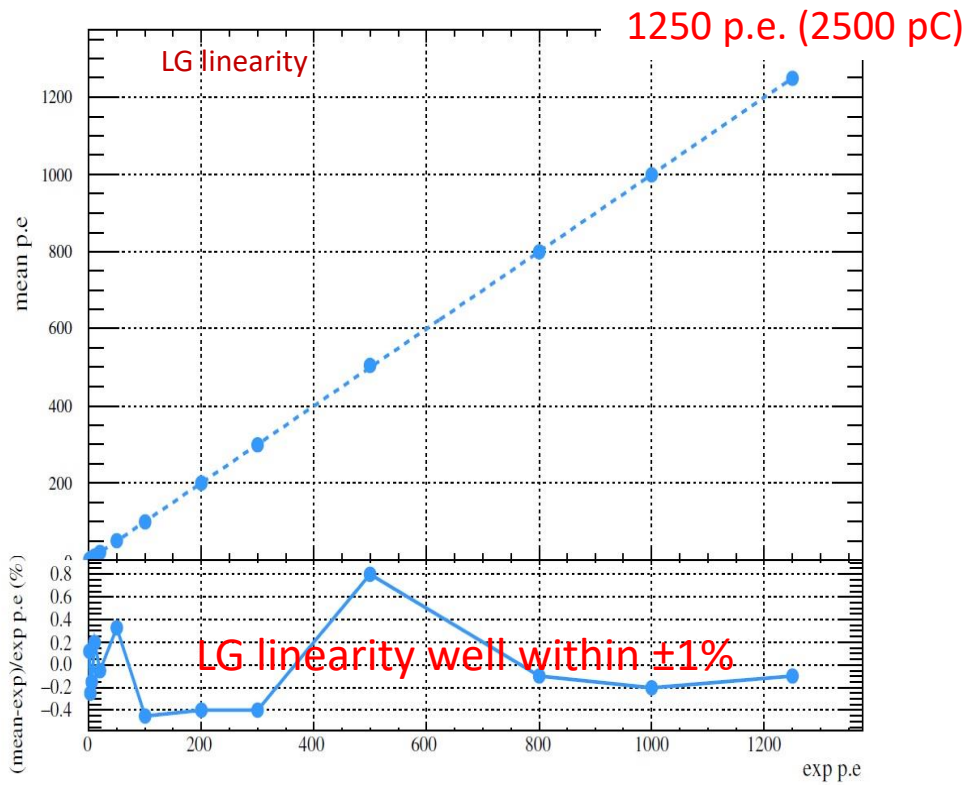
HKROC can accept consecutive events (separated by ~30 ns)

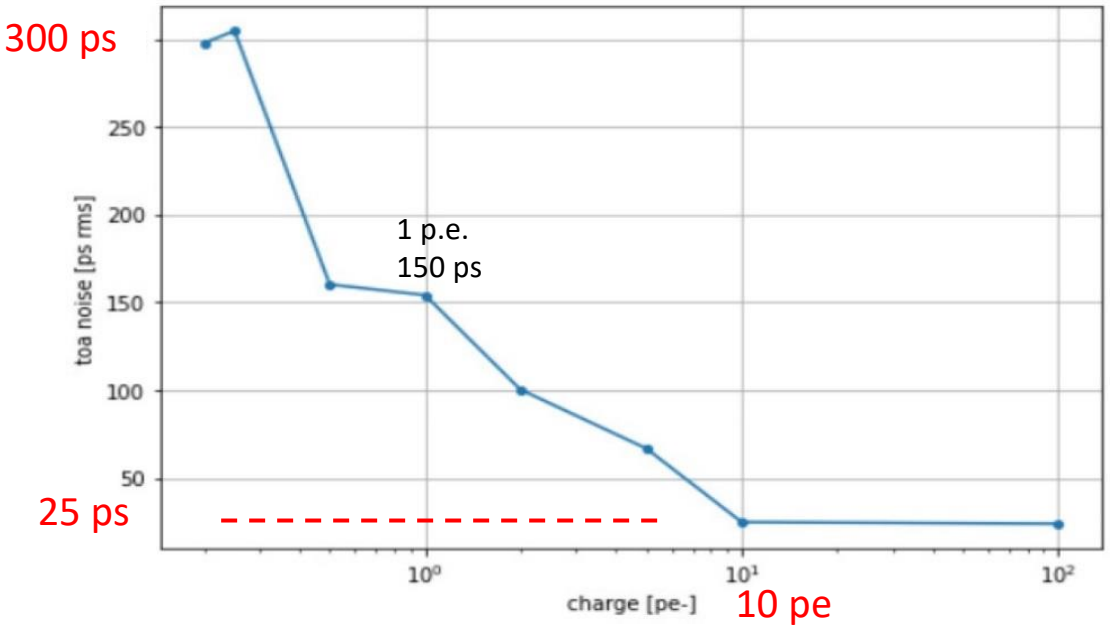
Internal HKROC memory writing is without dead time

Readout speed is only limited by serial link bandwidth (average values above)

Main experimental results with HKROC0 – Charge and Time

- Measurement with the full chain (analog + digital and reconstruction)
  - Signal auto-triggered with threshold





Charge resolution :

< **0.1 p.e (200 fC)** at ≤ 10 p.e

< 1 % otherwise

Charge linearity < **±1%** from 1 to **1250 p.e. (2500 pC) across the 3 gains**

TDC characterization with **1/6 p.e. threshold**

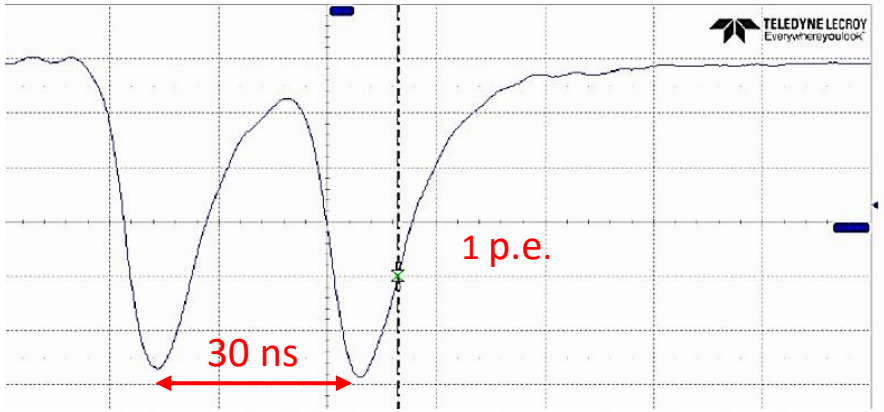
TDC resolution :

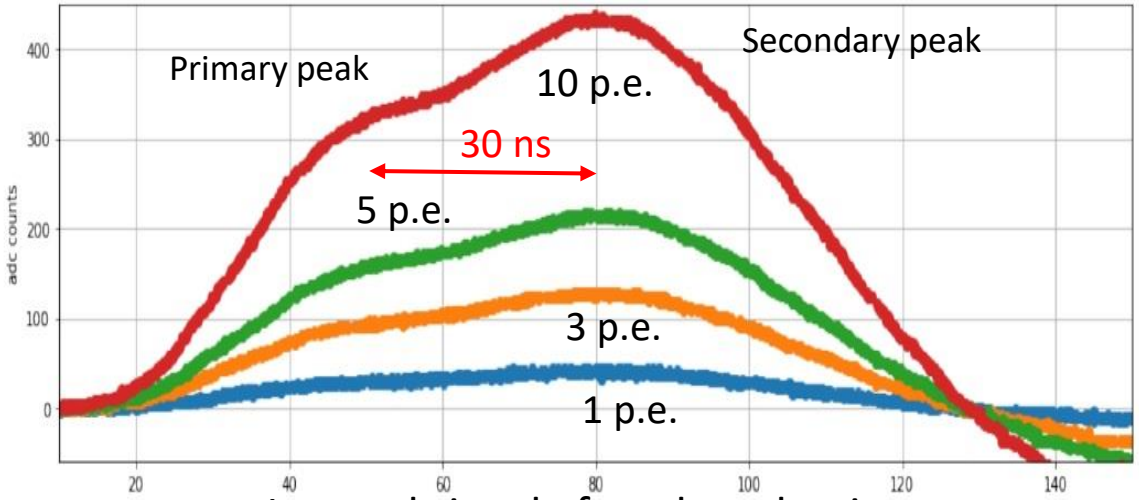
150 ps rms @ 1 p.e

≤ 25 ps rms @ 10 p.e

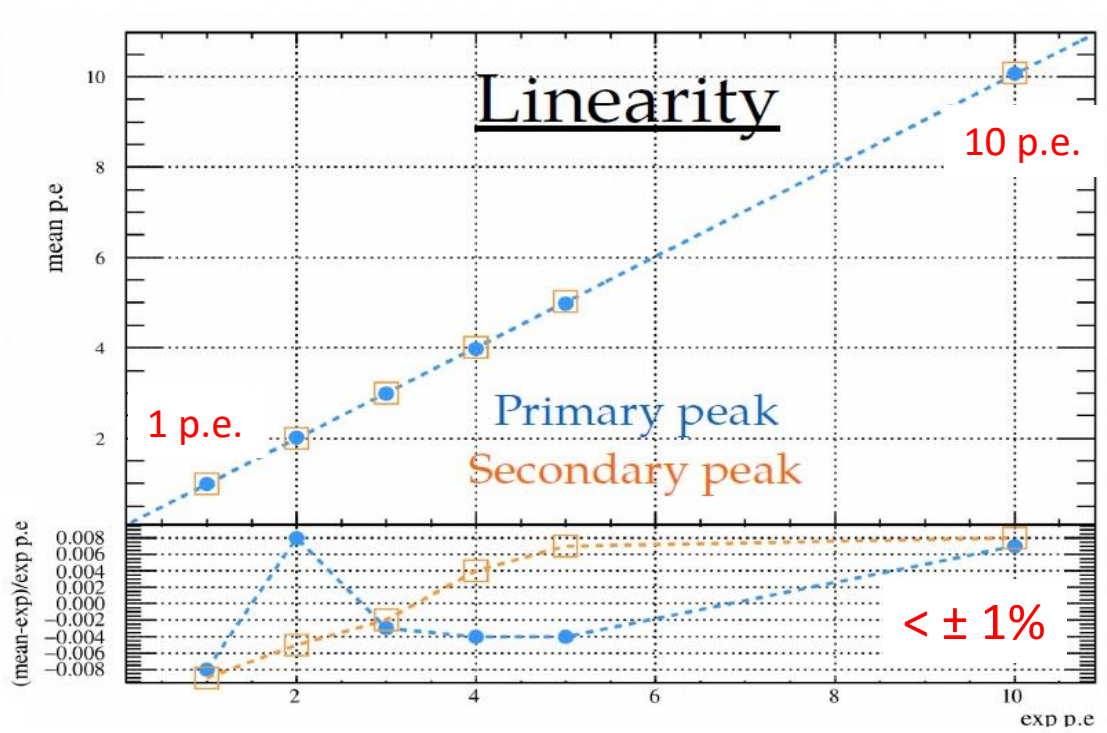
Main experimental results with HKROC0 - Pile-up

- Measurement with 2 events separated by ~30 ns (full chain: analog, digital and reconstruction)
  - Signals auto-triggered (internal programmable threshold)





Internal signal after slow shaping



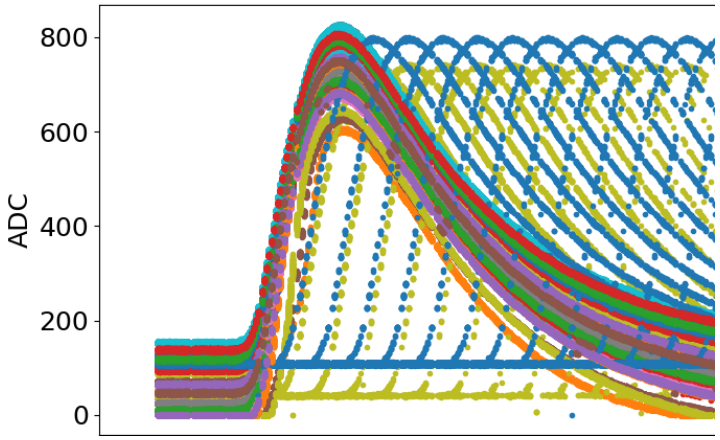
Charge reconstruction algorithm of the two peaks

Good linearity of reconstructed pile-up events

We can reconstruct both peaks properly !

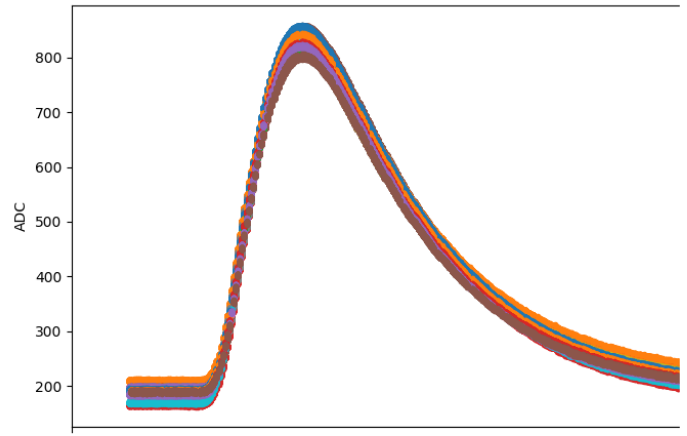
Improvements with HKROC1 - Yield and crosstalk

HKROC0 ADC yield was > 95%

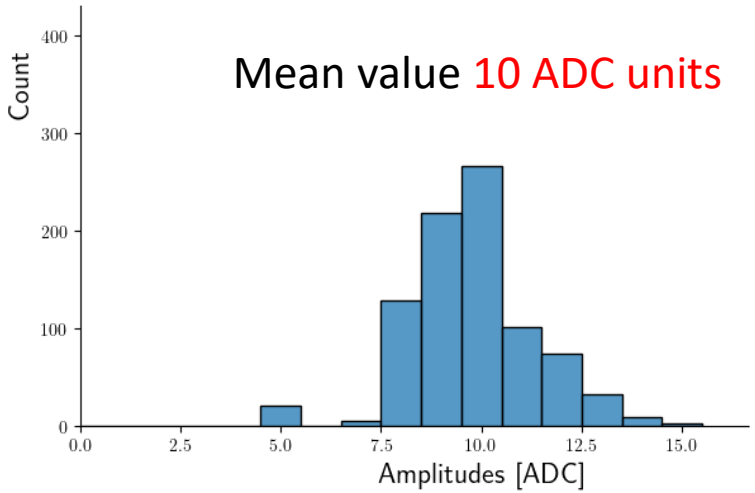


CMS-HGCROC improvement included in HKROC1b ADC

HKROC1b, 100% operating channels



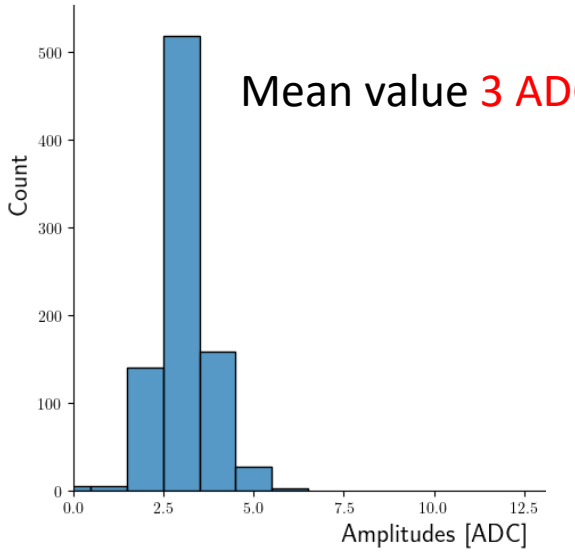
HKROC1 measurements



Mean value 10 ADC units

Reduction of the crosstalk of large signal on other channels

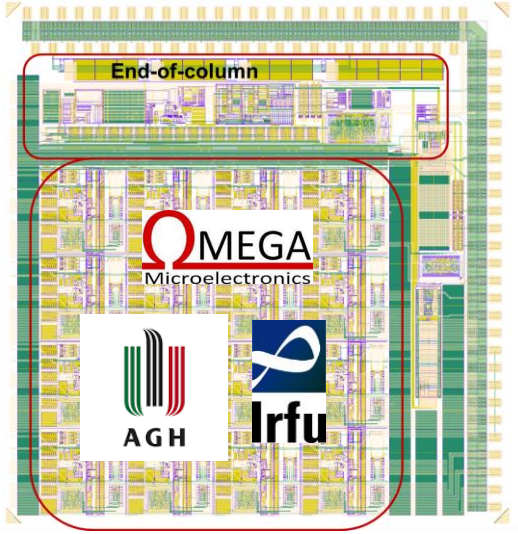
Reduction of x3
(1 pe is ~ 30 ADCu)

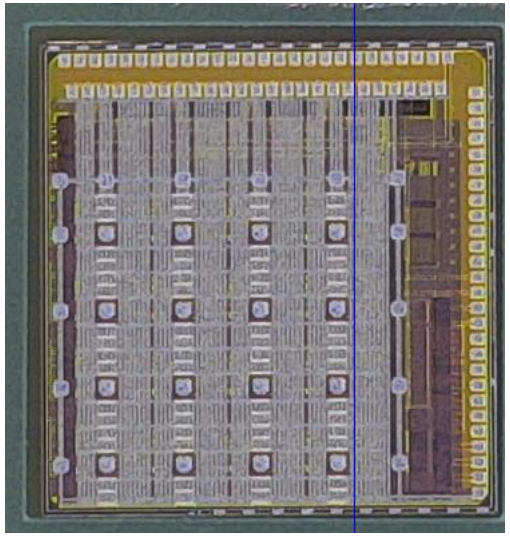


Mean value 3 ADC units

EICROC0 overview

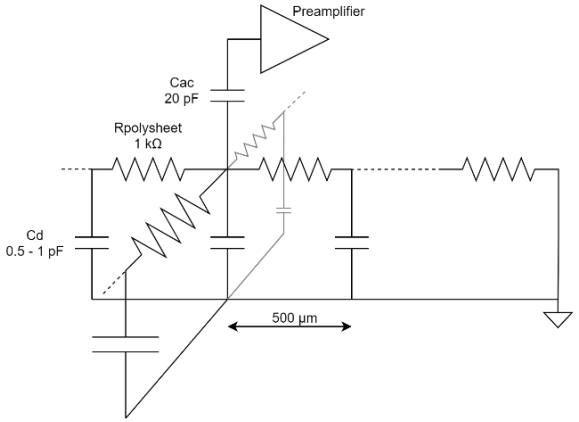
- EICROC0 is a 16-channel testchip for AC-LGADs at EIC
  - Based on ALTIROC (ATLAS HGTD) front-end and HGCROC (CMS HGCAL) ADC/TDC
  - Reads 500x500 µm pixels for sensor evaluation
  - Readout designed for testbeam (not EIC)
  - Fabricated in march 2022, received beg july 2022
  - now under test at IJCLAB and OMEGA
  - New submission in AIDA innova eng. run

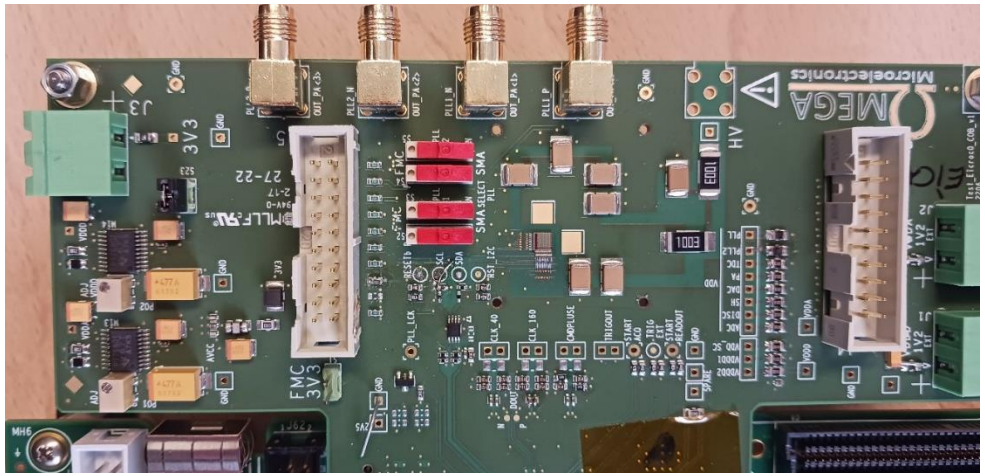




New concept of sensor [N. Cartiglia et al.]

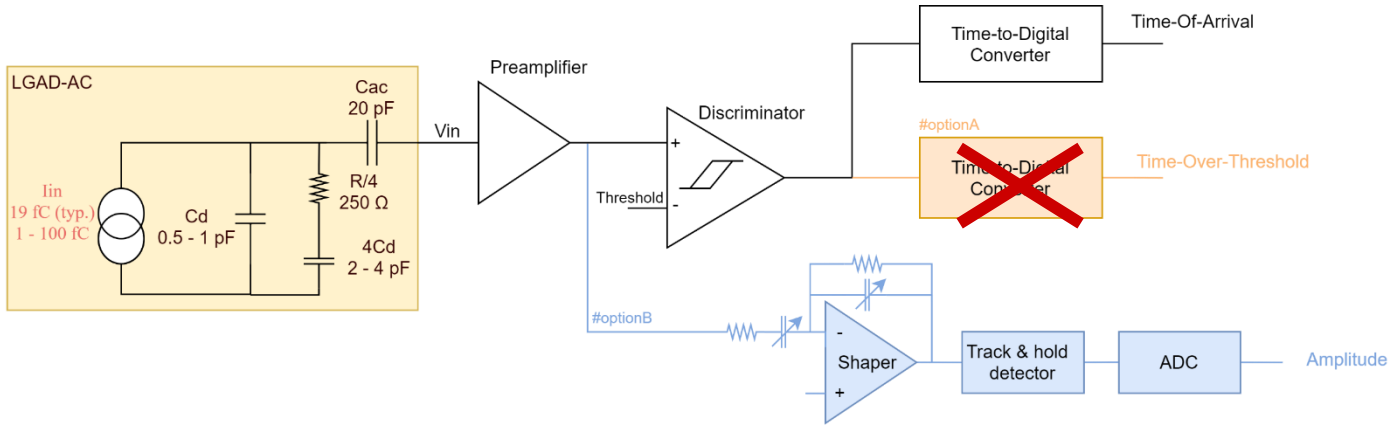
- AC coupled LGAD: **large signal and fast timing**
- Resistive layer for charge sharing: high position resolution
- « Large » pixel allows implementation of **ADC and TDC pixel-wise**

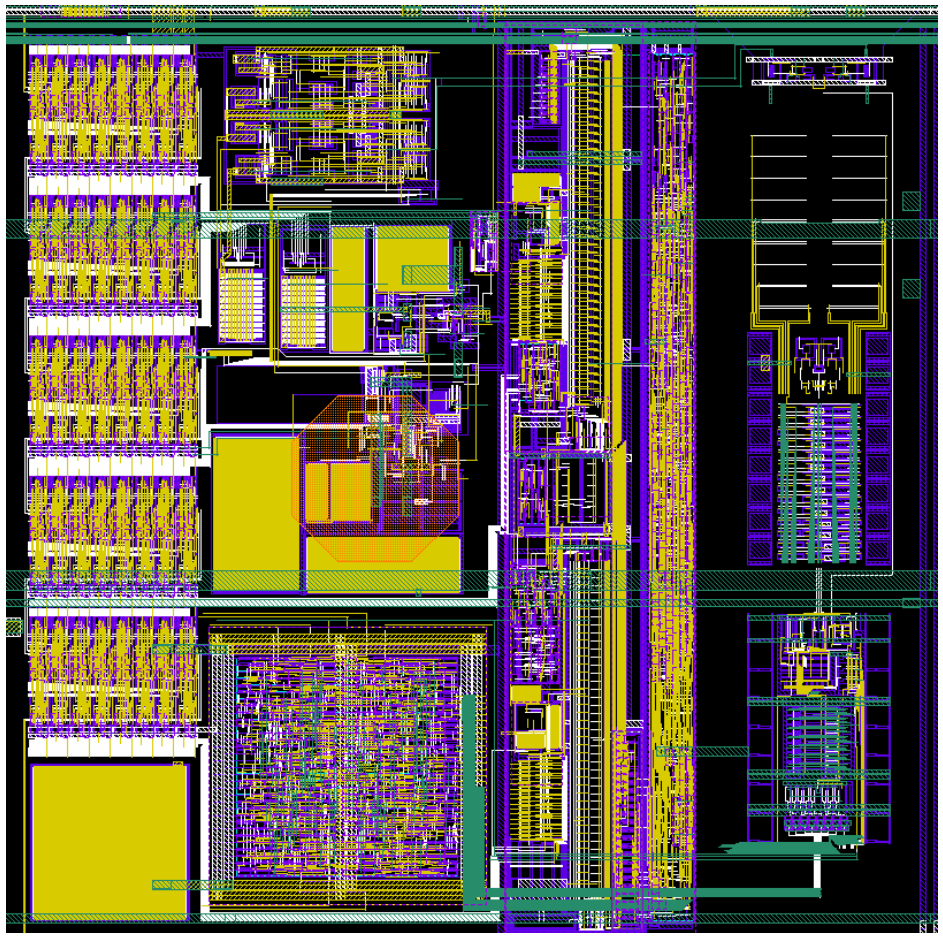




EICROC0 : one pixel overview

- One pixel design
  - Preamp, discri taken from ATLAS ALTIROC
  - I2C slow control taken from CMS HGCROC
  - TOA TDC adapted by IRFU Saclay
  - ADC adapted to 8bits by AGH Krakow
  - Digital readout : FIFO depth 8 (200 ns)
- 5 slow control bytes/pixel
  - 6 bits local threshold
  - 6 bits ADC pedestal
  - 16 TDC calibration bits
  - Various on/off and probes





Slow control

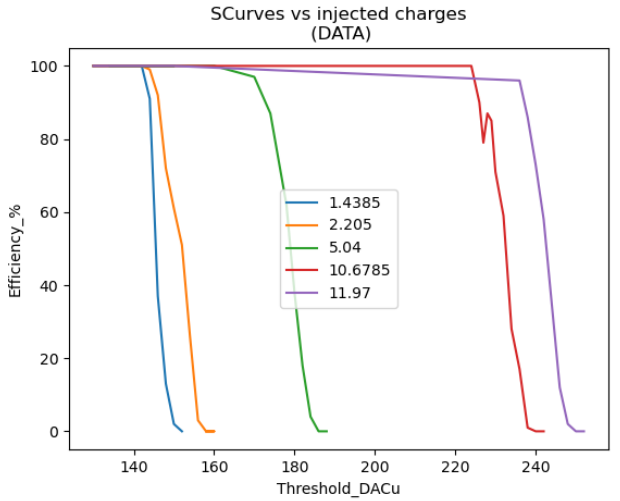
PA +discri

TOA TDC

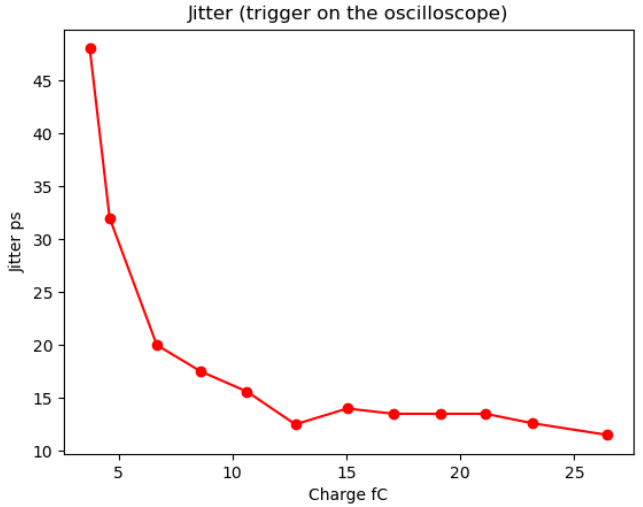
8b 40M ADC

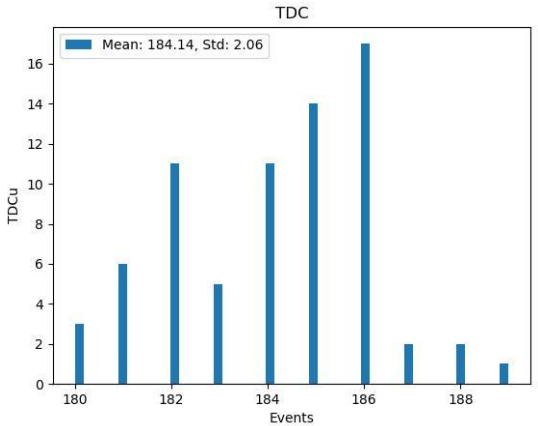
Trigger efficiency

- Measurements with DAQ (clocks on)
- Minimum threshold ~ 2 fC
- Noise from s-curve ~0.2 fC
- Better from what is observed with analog probe (~10fC clock noise)
  - Probe picks up clock noise



- Scope measurement from discriminator output : 15 ps @ 10 fC
- TDC measurements ~50 ps
  - Still large correlated noise under investigation



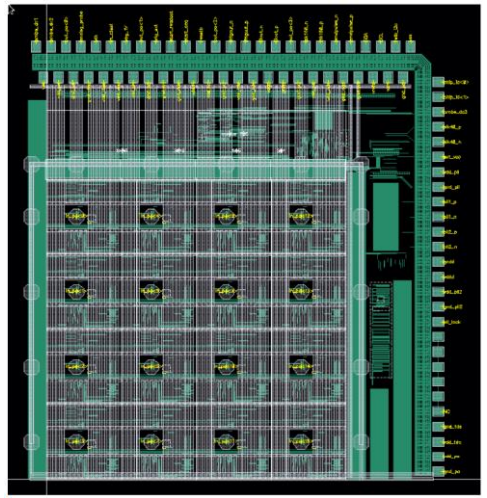


Evolution of EICROC

- EICROC0 is a testbeam prototype => sensor characterization
  - Triggered readout
  - all data shipped out : 16 ch * 8 samples ADC + TDC
  - Present power ~2 mW/ch + 4*20 mW « analog probe preamp »
  - ADC power + shaper/driver to be reduced from ~1 mW to 100 µW/ch => EICROC0A

- EICROC1 will address larger dimensions 4x16 or 8x16 or 4x32
  - Address floor planning and power distribution
  - Selective readout : hit + 9 neighbouring channels

- EICROC2 final size : 32x32



- CPROC (Central Processing unit in ReadOut Chip)
  - TSMC 130 nm
  - Exploratory R&D: programmable, needs of more and more intelligence in chip
  - Based on the RISC-V

Summary

- An engineering run has been submitted last year
  - 10 chips from OMEGA, AGH, IJCLAB and Weeroc

- HKROC:
  - The second version, HKROC1, has been submitted this April
  - Bugs fix: ADC, TDC, DRAM
  - Lower crosstalk
- EICROC
  - A new chip dedicated for testing AC-LGAD has been submitted
  - TSMC 130 nm MPW run by 31st of March 2022
  - 4x4 matrix of 500x500 μm^2 pixel size
  - 8b SAR ADC per pixel for charge measurement up to 100fC
  - 10b TDC for timing measurement (25 ps binning)
  - ~ 1 mW/pixel
- CPROC
  - First chip with a RISC-V embedded
  - New exploratory R&D

Backup

Hyper-Kamiokande detector and HKROC chip

The next generation of **neutrino** observatory in Japan (HyperK) will be built in **2026** with **260 kton** water Cherenkov detector**.** It will study **neutrinos** from **various sources**: solar, atmospheric, accelerator and Supernova neutrinos

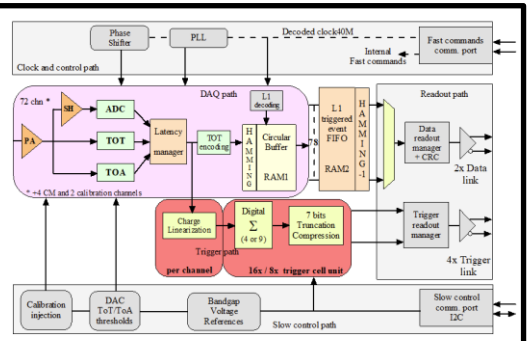
Based on HGCROC, HKROC will provide a versatile, low-power and fully integrated solution for large neutrino experiments

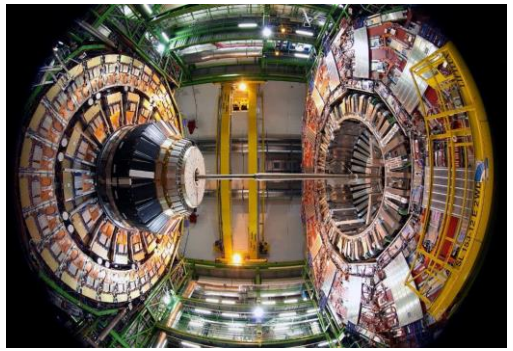
HGCROC for the CMS endcap calorimeter ar HL-LHC

6M of Silicon channels
(+ 240k of SiPM)

Radhard (200 Mrad)
Low Power (15 mW per chn)
Precise timing (25 ps)

Total of 150k ASICs needed
Pre-prod this year
Project started in **2017**

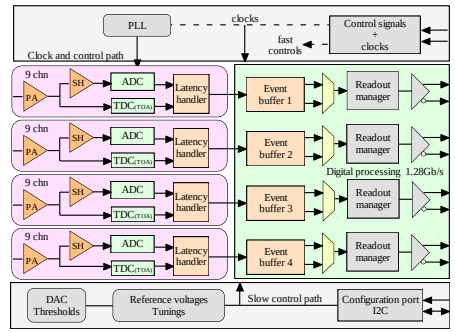


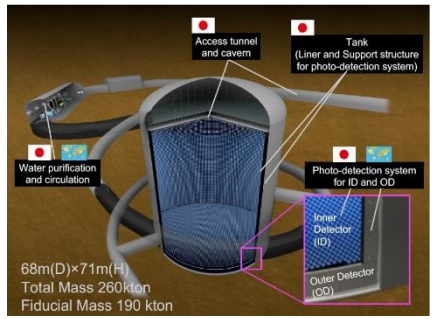


HKROC was developed in < 6 months

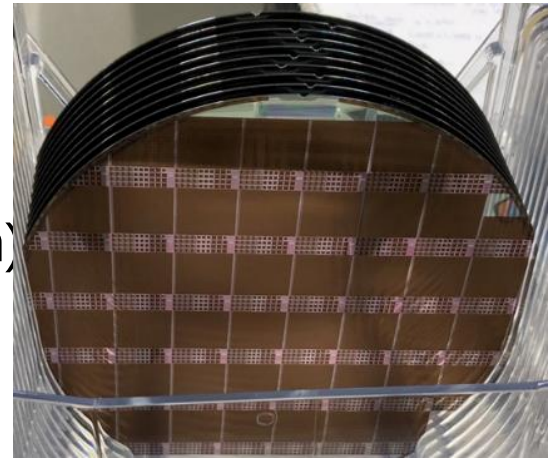
Same ASIC structure (floorplan)
Same ADC and TDC
Same readout

New preamplifier
New digital processing



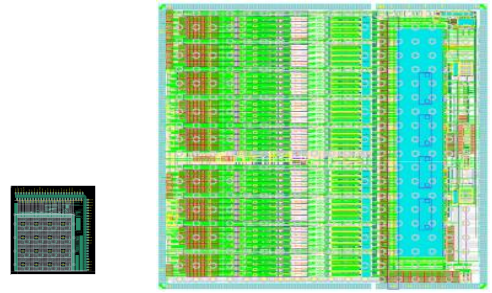


Plans for 2024

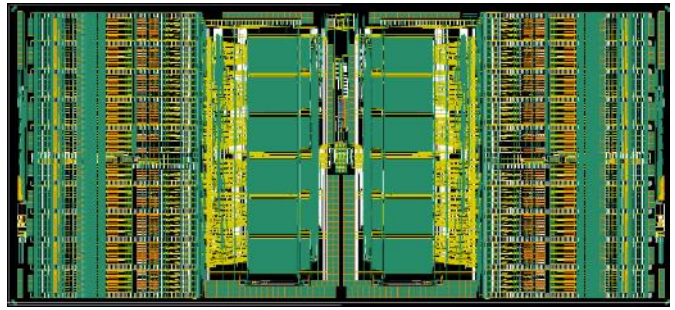


- CALOROC = H2GCROC (SiPM) for EIC
  - Analog part = H2GCROC, backend EIC specific
  - Need to choose HGCROC pin-pin compatibility (64 ch) or HKROC size (32ch)
  - 2 versions : conservative (ADC/ToT), improved (multi-gain)
  - Cost in MPW : 2 * (50 or 100 mm²) * 2 k€ > Engineering run = 250 k€
  - Mid/fall 2024 tbd

HKROC



- EICROC
  - Possibly EICROC0A with improved digital noise and low power ADC
  - EICROC1 (4 or 8)*16 channels with possible column « flavours »
  - Probably not yet with EIC readout
  - Area : 20 - 35 mm²
  - Mid/fall 2024 especially if Engineering Run chosen



Trends for calorimeter readout

- On-detector embedded electronics, low power multi-channels ASICS
  - CALICE SKI/SPI/HARDROC, FLAME, CMS HGCROC, FCC Lar, FATIC…
  - Challenges: # channels, low power, digital noise, data reduction, timing capability

- Develop readout ASIC family for DRD6 prototype characterization
  - Inspired from CALICE SKIROC/SPIROC/HARDROC/MICROROC family
  - Targeting future experiments as mentionned in ICFA document (EIC, FCC-ee, ILC, CEPC…)
  - Addressing embedded electronics and detector/electronics coexistence + joint optimization
  - Detector specific front-end but common backend
  - Allows common DAQ and facilitates combined testbeam

- Start from HGCROC / HKROC: Si and SiPM
  - Reduce power from 15 mW to few mW/ch
  - Allows better granularity
  - Remove HL-LHC-specific digital part and provide flexible auto-triggered data payload
  - Several improvements foreseen in the VFE and digitization parts
  - 130 nm or 65 nm ?

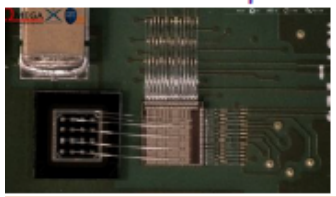
Status of EICROC0 Test Bench at IJCLab

RC2 | RC3

Preliminary studies [board w/ EICROC0, no AC-LGAD]

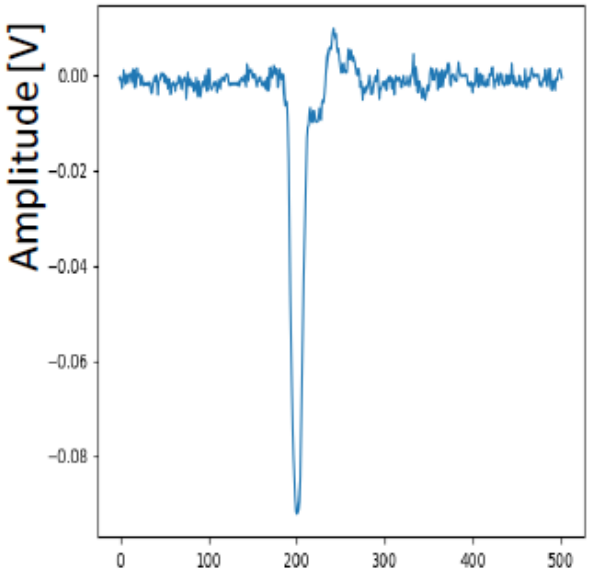
- TZ Pre Amplifier output signals
  - SNR > 70 for 12.5 fC input ; SNR > 6 for 1 fC input)
  - Jitter evaluation: < 20 ps (≥ 6 fC) ; 8 ps (25 fC)
- TDC performance (alone):
  - quantification step (~25 ps) in fair agreement with design
  - observation of a large noise coupled to 160 MHz clock
  - Time of Arrival resolution estimated to 14 ps (25 fC)
- ADC performance (alone) functional, 8-fold noise structure observed
- Evaluation of cross-talk between channels underway
- Further nvestigation of noise / clock couplings (**TDC and ADC**)

Short term plan: to evaluate performances of the existing board w/ **EICROC0 + AC-LGAD** (4 x 4)



Wire-bonding by Brookhaven National Laboratory

Typical **PA output signal** (12.5 fC input)

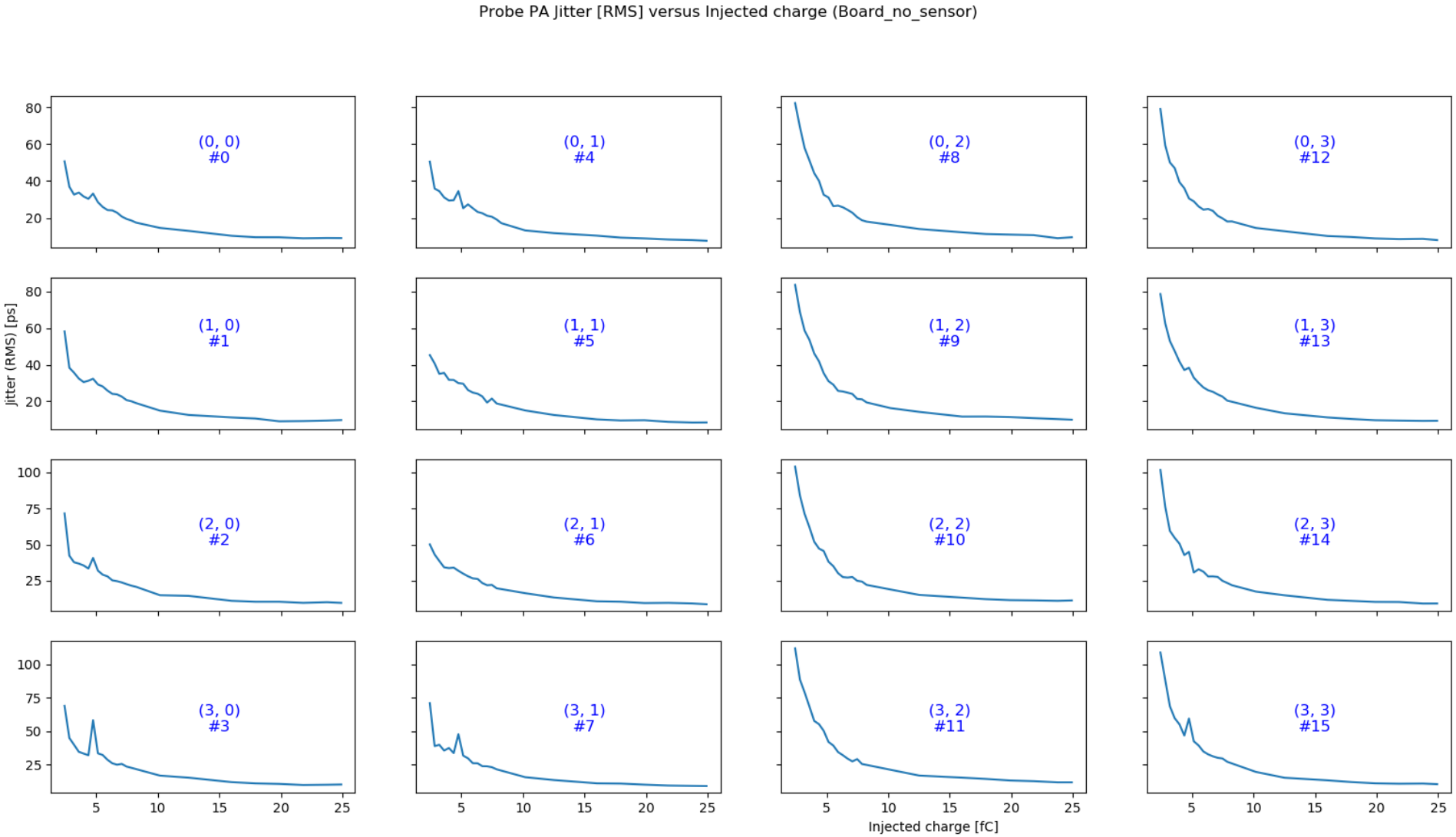


|Max. Amplitude| 95.5 mV

RMS 0.6 ns

Rise (Fall) Time **0.7 ns**
computed between
10% and 90% of |Max. Ampl.|

Jitter on analog probe_pa output (clocks off) [Dominique]



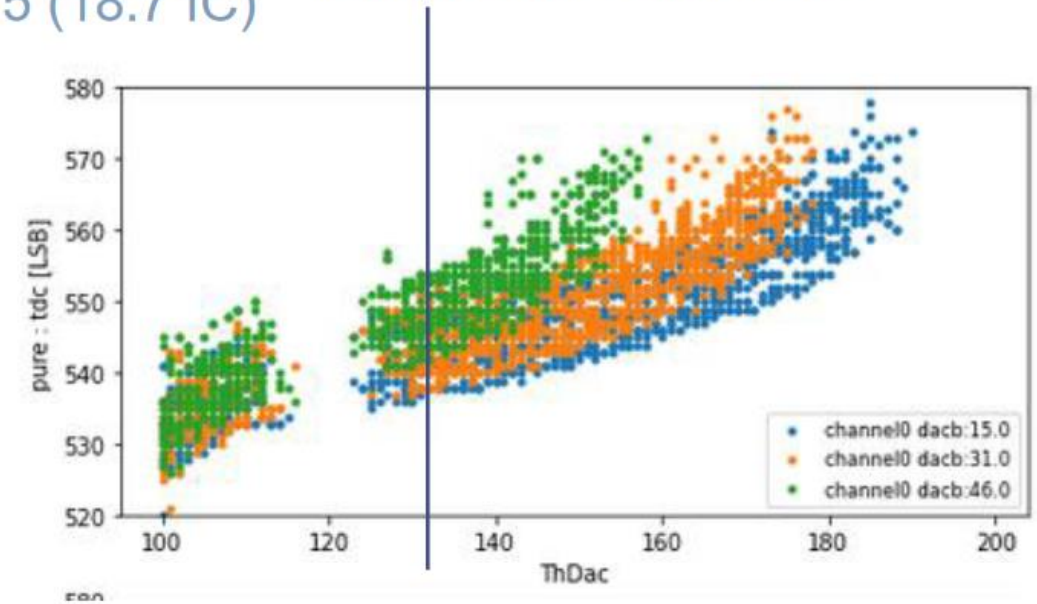
More TDC measurements [Florent]

- Threshold ~2 fC
- Noise ~3 TDCU = 75 ps

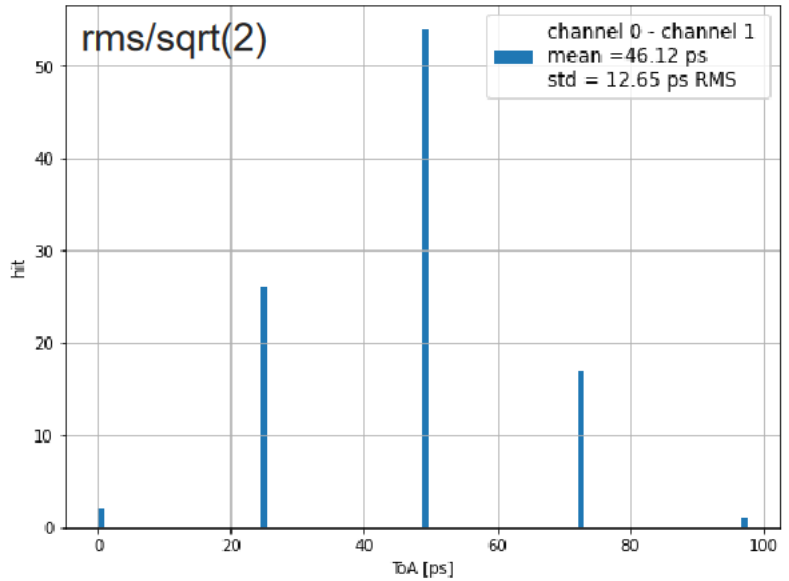
dacb_pulser :

- 46 (6.2 fC)
- 31 (12.5 fC)
- 15 (18.7 fC)

Estimated noise floor : 2 fC ?



ThDac : 130 :

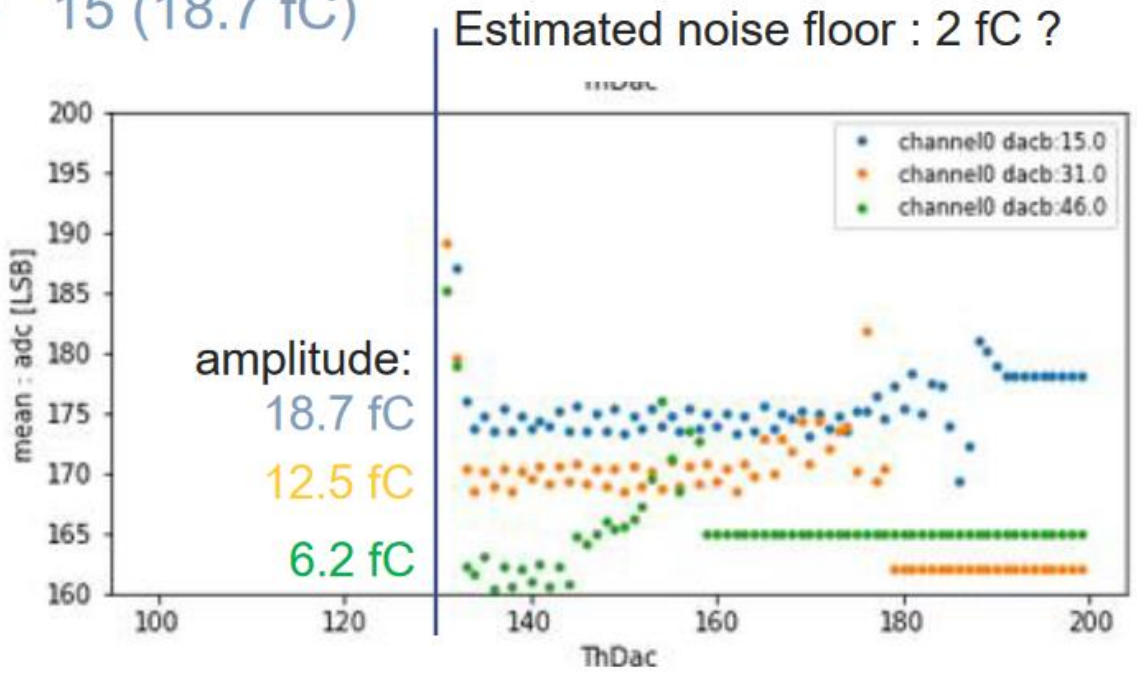


Distribution of the time difference

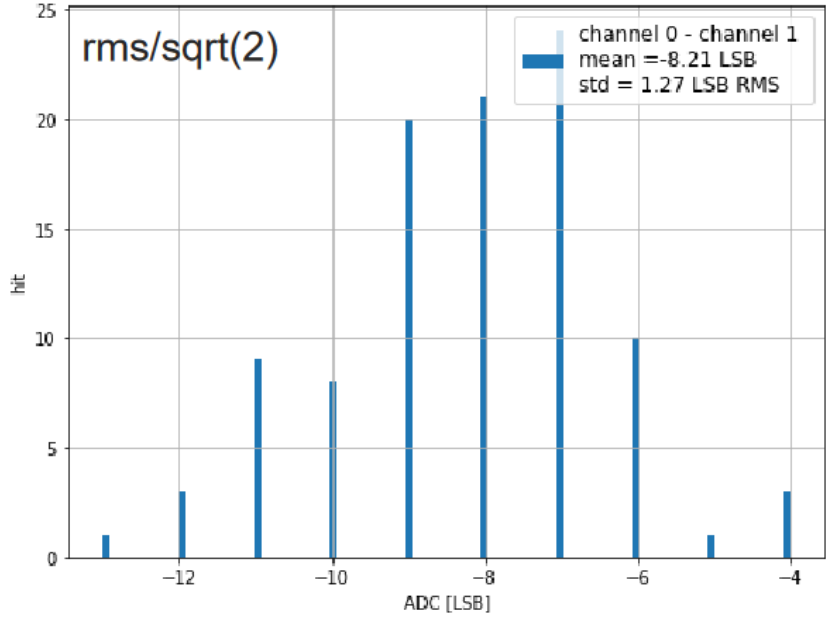
Preliminary ADC measurements [Florent, Laurent]

- ~large ADC noise (~10 UADC) under investigation
- Mostly coherent

dacb_pulser :
- 46 (6.2 fC)
- 31 (12.5 fC)
- 15 (18.7 fC)



ThDac : 150 :



Distribution

Noise near 1.2 LSB RMS

jsc is removed