AGH University of Science and Technology

Update from AGH activities in WP11.3 – CMOS 130/65 nm

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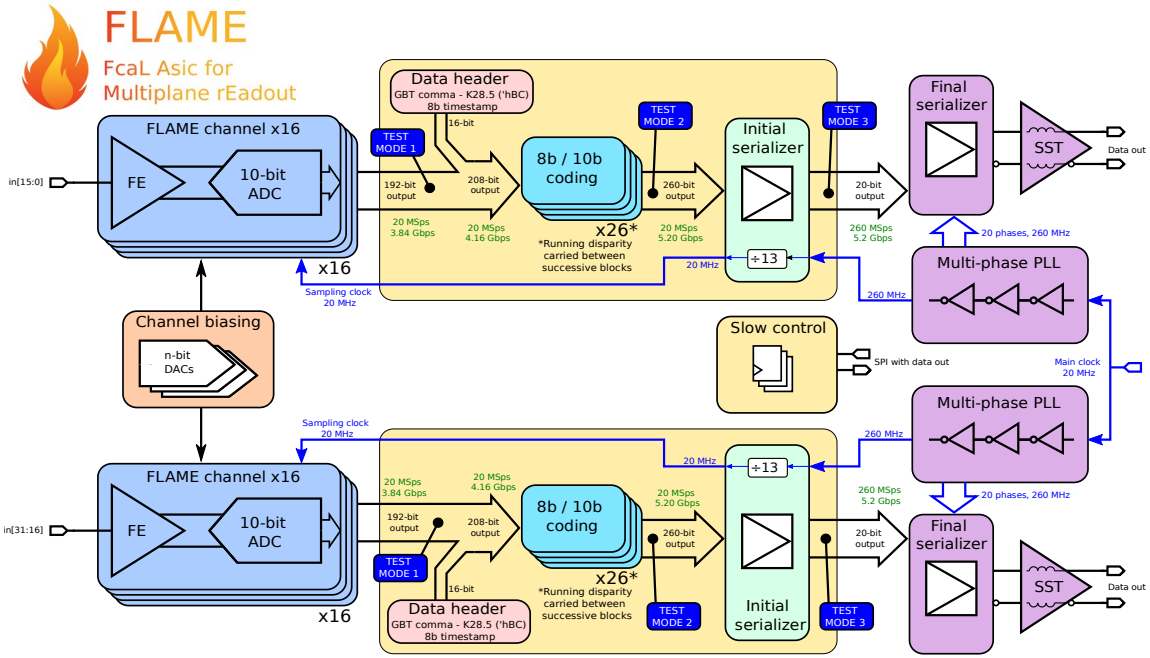
AIDAinnova 3rd Annual meeting, 18-21 March 2024, Catania, Italy

Outline

- Activities in CMOS 130/65 nm
  - FLAME/FLAXE ASICs for calorimetry and LUXE experiment in CMOS 130nm
  - R&D on precise TAC-based TDC in CMOS 130nm
  - R&D on 10-bit ADC with internal threshold in CMOS 130nm
  - Publications about completed designs in CMOS 130/65 nm
  - Still waiting for man-power resources...
    - Fast Serializer&Transmitter in 130nm and 65nm
    - Test setups for ADCs in 130nm and 65nm

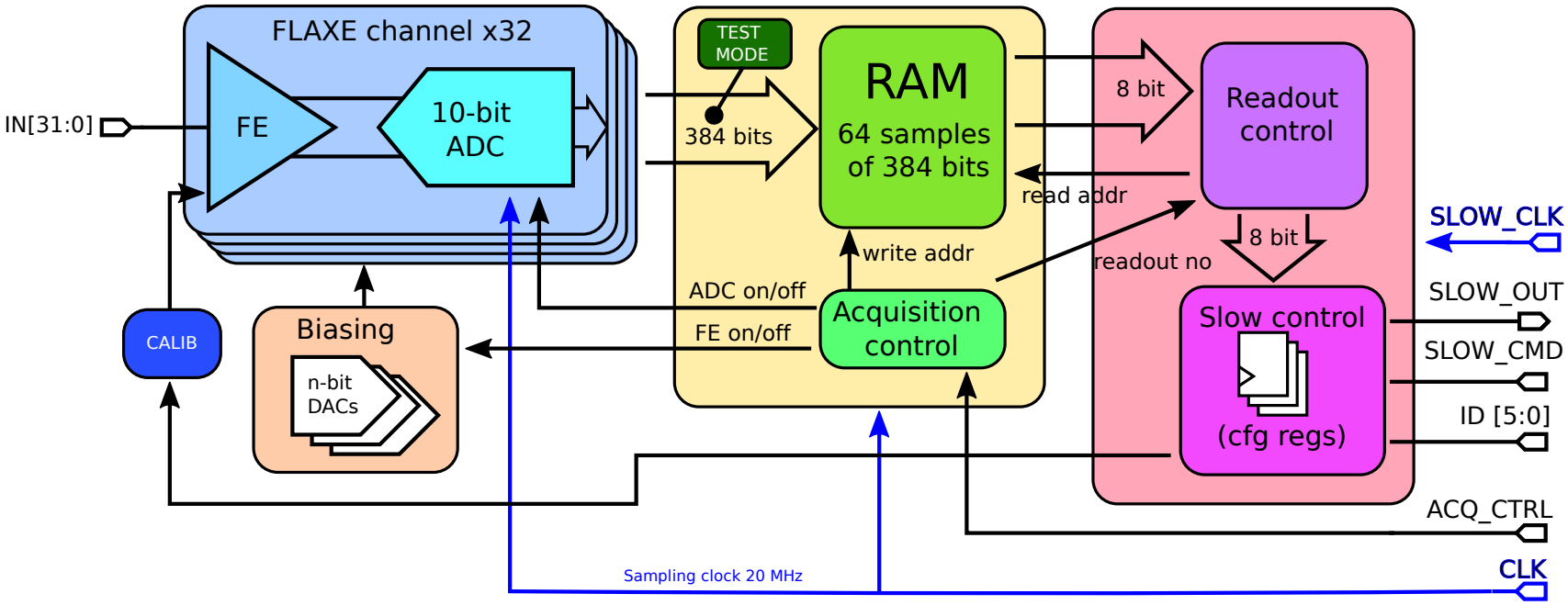
Activities in CMOS 130nm FLAME ASIC for calorimetry



- 32-channel ASIC in CMOS 130nm
- In each channel
  - analog front-end (T_{peak}~50ns, switched gain
  - 10-bit ADC (f_{sample}=20MHz)
- two fast 5.2 Gbps serializers and data transmitters

Presently FLAME chips are used for first LUXE test-beams. In the test-beam at DESY, 11-18 September 2022, a 4-chip front-end board (128 channels) was used to study the performance of Si and GaAs sensors and shower development. Analysis of the collected data are ongoing and publication is being prepared.

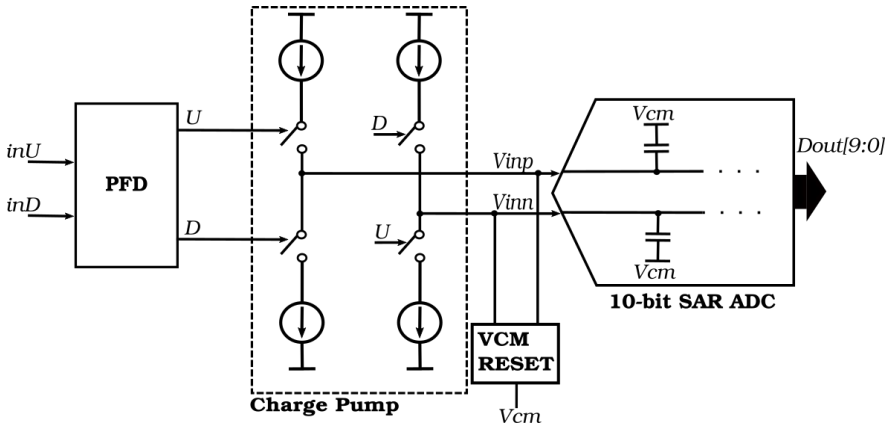
Activities in CMOS 130nm
FLAXE ASIC for ECAL-p in LUXE experiment

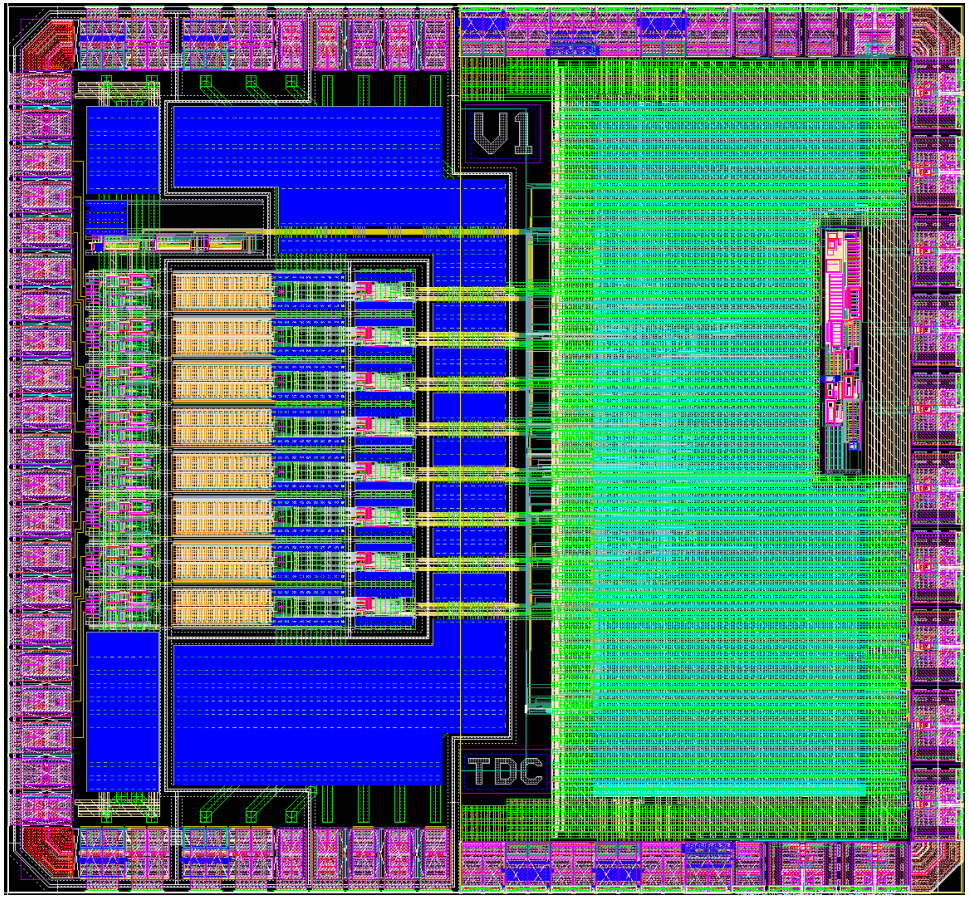


- FLAXE is a modified 32-channel FLAME in CMOS 130nm without high speed serialisers&transmitters – readout rate in LUXE ~10 Hz
- More than 1000 FLAXE chips were produced. Sent for dicing and packaging recently…

Activities in CMOS 130nm
R&D on precise TDC – TAC+ADC architecture

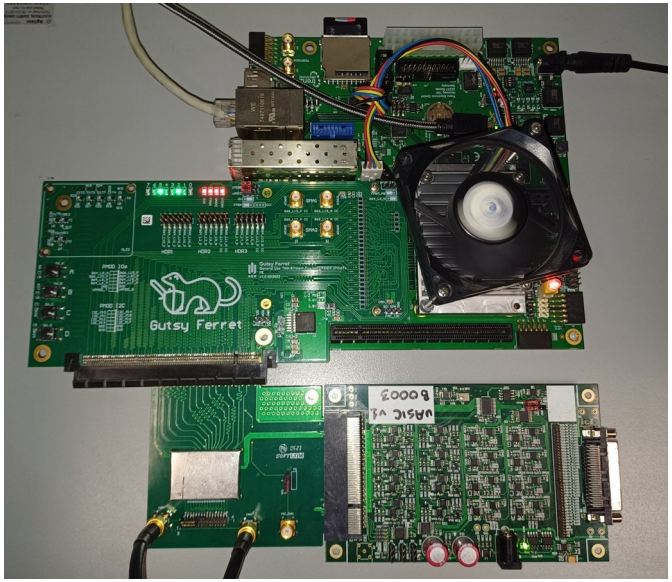
Single TDC channel



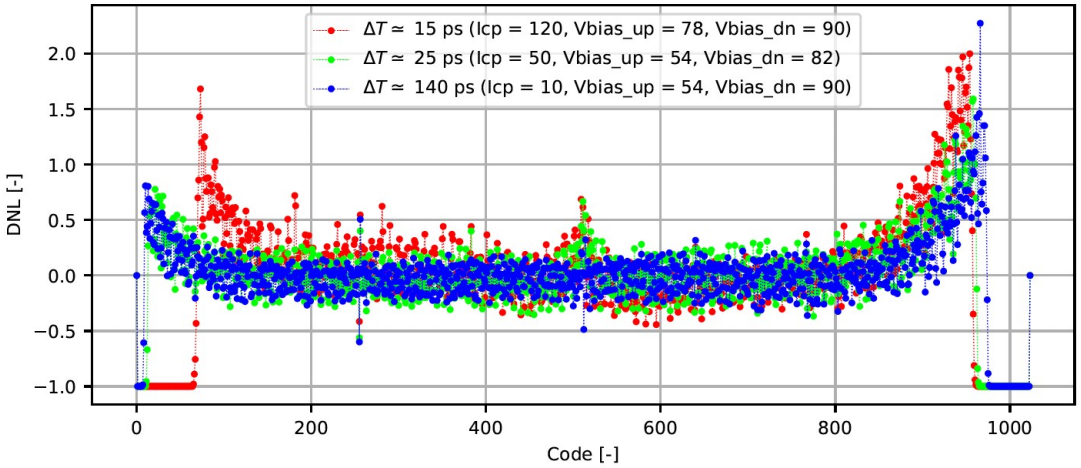


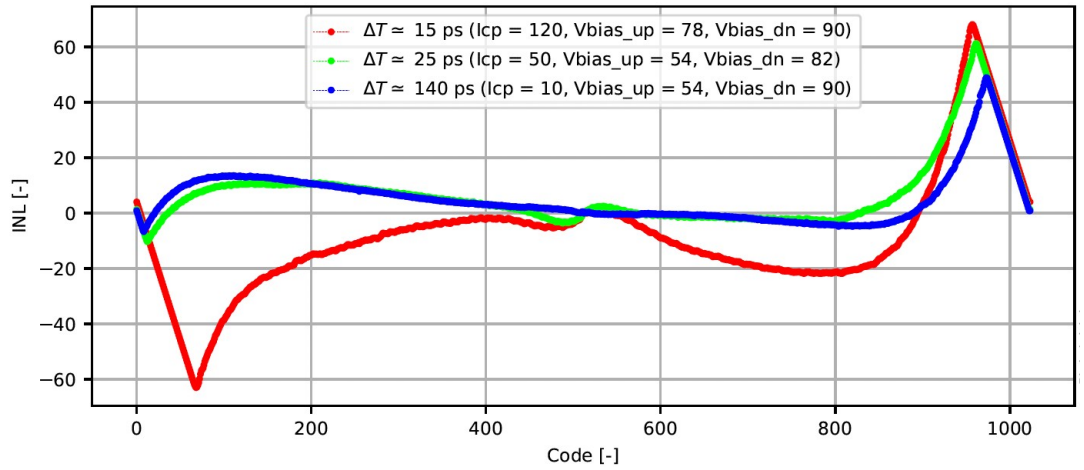
- New TAC-based TDC aiming at timing measurement precision of ~10ps, consuming ~1mW
- As ADC the existing 10-bit SAR is used
- 8-channel prototype TDC chip was fabricated in 2022

Activities in CMOS 130nm
R&D on precise TDC - 1st measurements



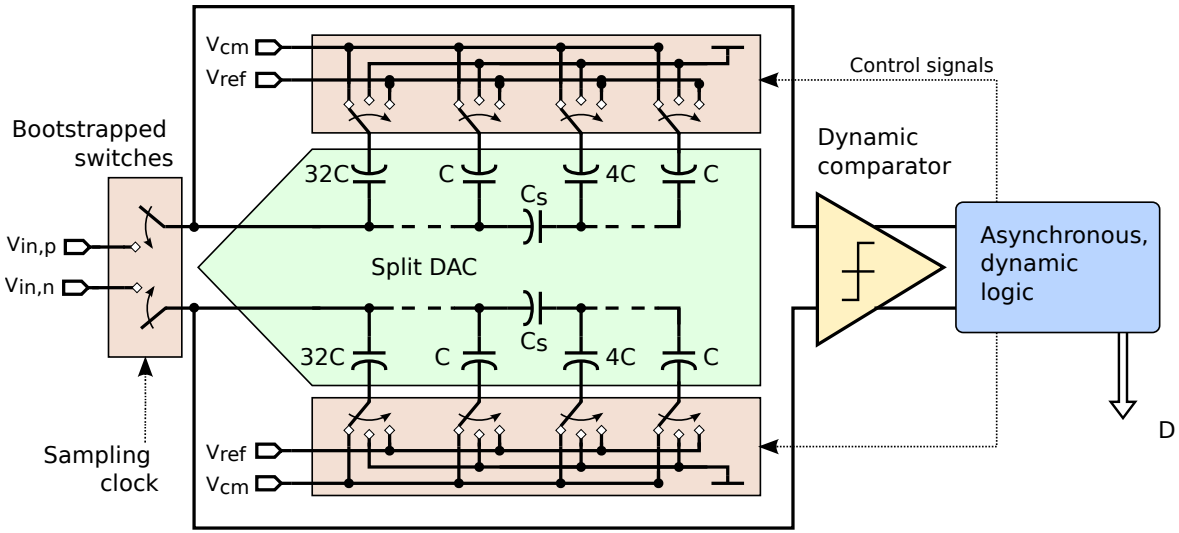
- TDC works!
- Good DNL <1LSB
- INL rather high – to be understood
- Jitter < 1LSB





Activities in CMOS 130nm
R&D on 10-bit ADC with internal threshold

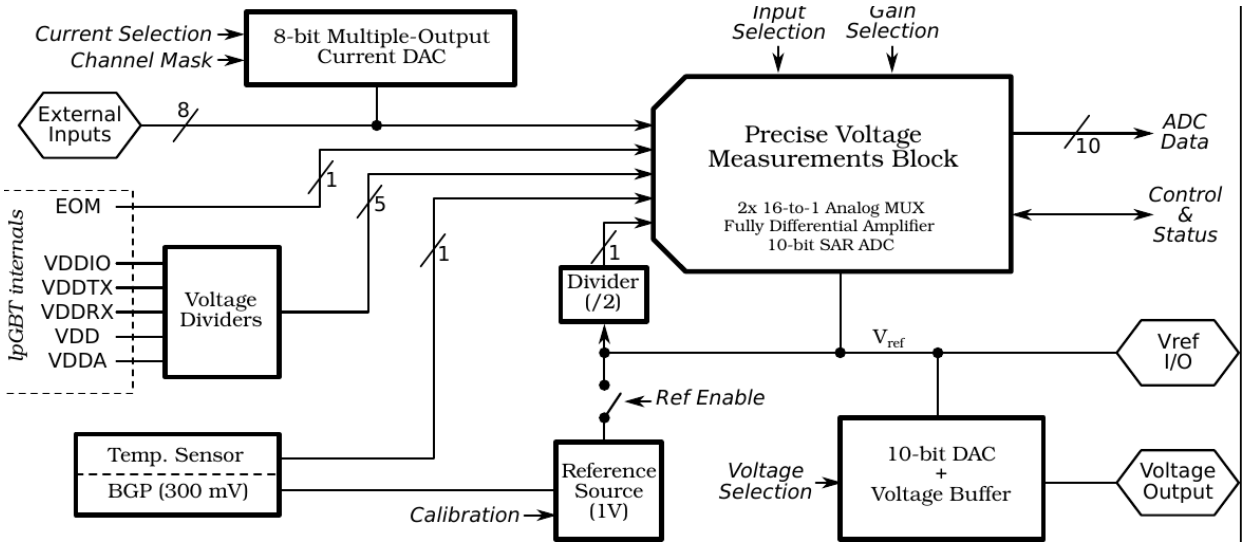
Our existing 10-bit ADC
- power 680uW@40MSps
- works up to 50MSps



- To decrease power consumption even further, we are introducing additional comparison with threshold (MSc thesis)
  - If signal (>Vth) - 11 comparisons are done instead of 10
  - If NO signal – 2 comparisons and ADC reset is done
- The result is that ADC is slightly slower
- Estimated power for low occupancy ~ one third of the current one
- Schematic done, layout in progress...

Publications
lpGBT monitoring system in CMOS 65nm

- **An lpGBT subsystem for environmental monitoring of experiments**, M. Firlej, T. Fiutowski, J. Fonseca, M. Idzik, S. Kulis, P. Moreira, J. Moroń, K. Świentek, Journal of Instrumentation 2023 vol. 18 art. no. P06008



Publications
10-bit SAR ADCs in CMOS 130nm and 65nm

An ultra-low power 10-bit, 50 MSps SAR ADC for multi-channel readout ASICs, M. Firlej, T. Fiutowski, M. Idzik, S. Kulis, J. Moroń, K. Świentek, Journal of Instrumentation 2023 vol. 18 art. no. P11013

This ADC in CMOS 130 nm is used in HGCROC chip for HGCAL and TOFHIR chip for MTD, both for CMS Upgrade

Ultra-low power 10-bit 50-90 MSps SAR ADCs in 65 nm CMOS for multi-channel ASICs, M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Świentek, Journal of Instrumentation 2024 vol. 19 art. no. P01029

This ADC in CMOS 65 nm is used in lpGBT monitoring subsystem and is considered for MagnetStation and SciFi readout in LHCb Upgrade

Activities in TSMC 130/65 nm
Still waiting for man-power resources...

- Serializers&Transmitters
  – prototype Serializer&Transmitter in CMOS 130nm (~5Gb/s) and CMOS 65nm (~10Gb/s) were designed and fabricated long time ago.
- ADCs
  – Prototype 12-bit SAR ADCs in CMOS 130nm and 65nm, and improved 10-bit SAR ADC in CMOS 65nm were designed and fabricate long time ago
  – Dedicated setup is partially done, PCB for tests are being designed...