AGH University of Science and Technology

Update from AGH activities in WP11.3 – CMOS 28 nm

Marek Idzik for AGH-UST

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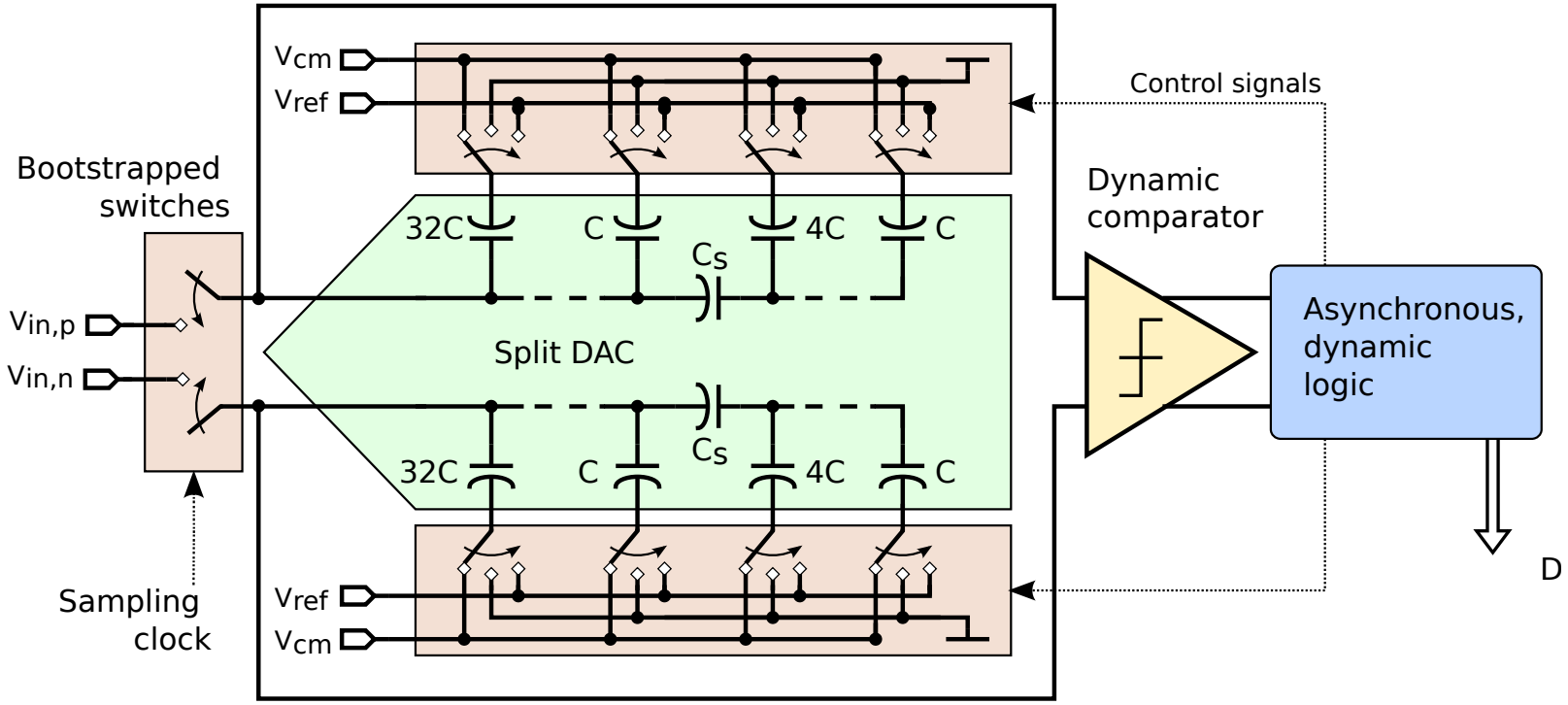
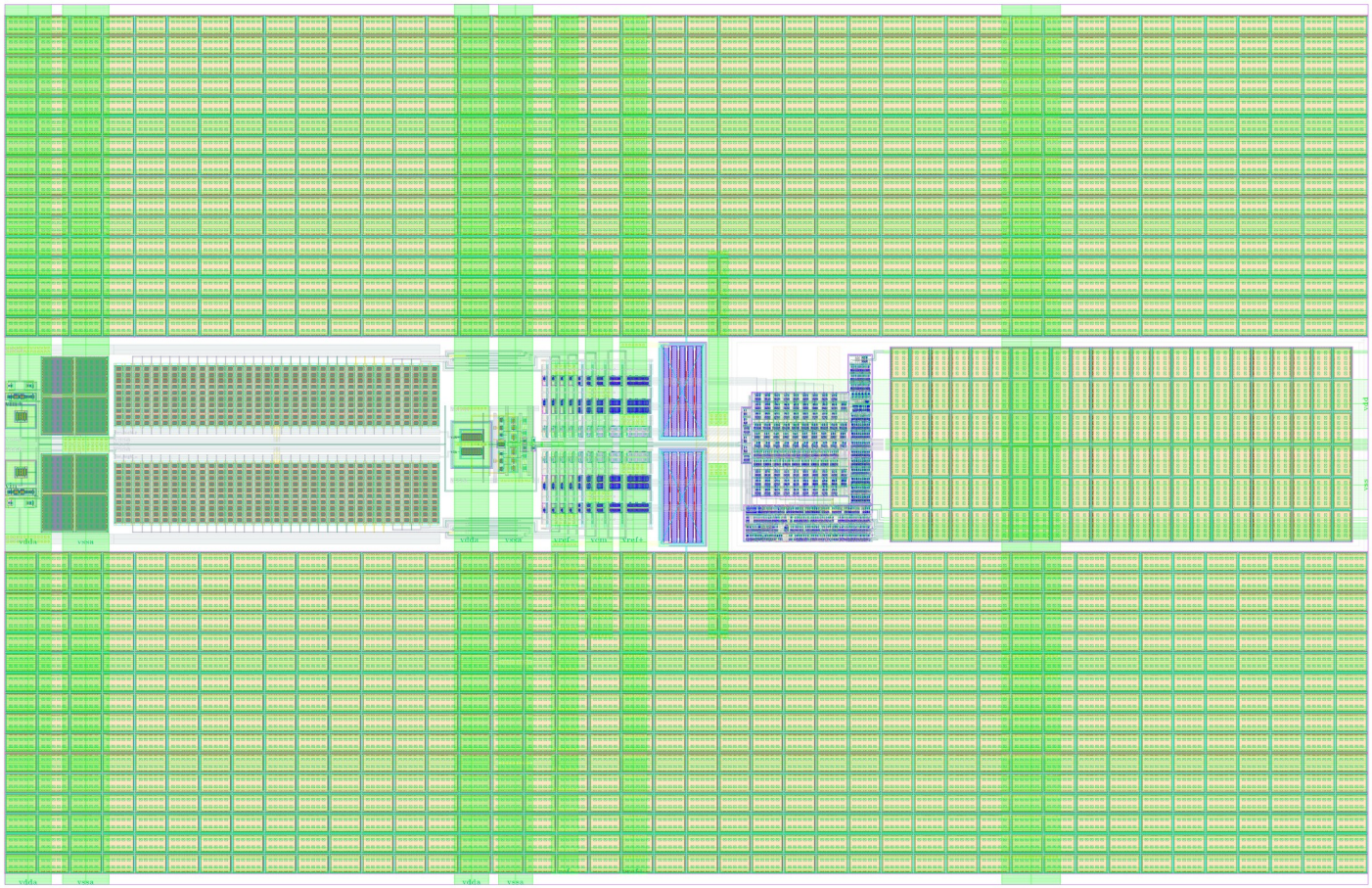
Design of fast ultra-low power 10-bit SAR ADC in CMOS 28nm

- SAR architecture already verified in CMOS 130/65 nm
  - Fully differential, MCS switching, dynamic comparator, asynchronous logic



- The goal → the ultra-low power and the highest sampling rate

Fast ultra-low power 10-bit SAR ADC in 28nm
Status of ADC integration



279um x 110um

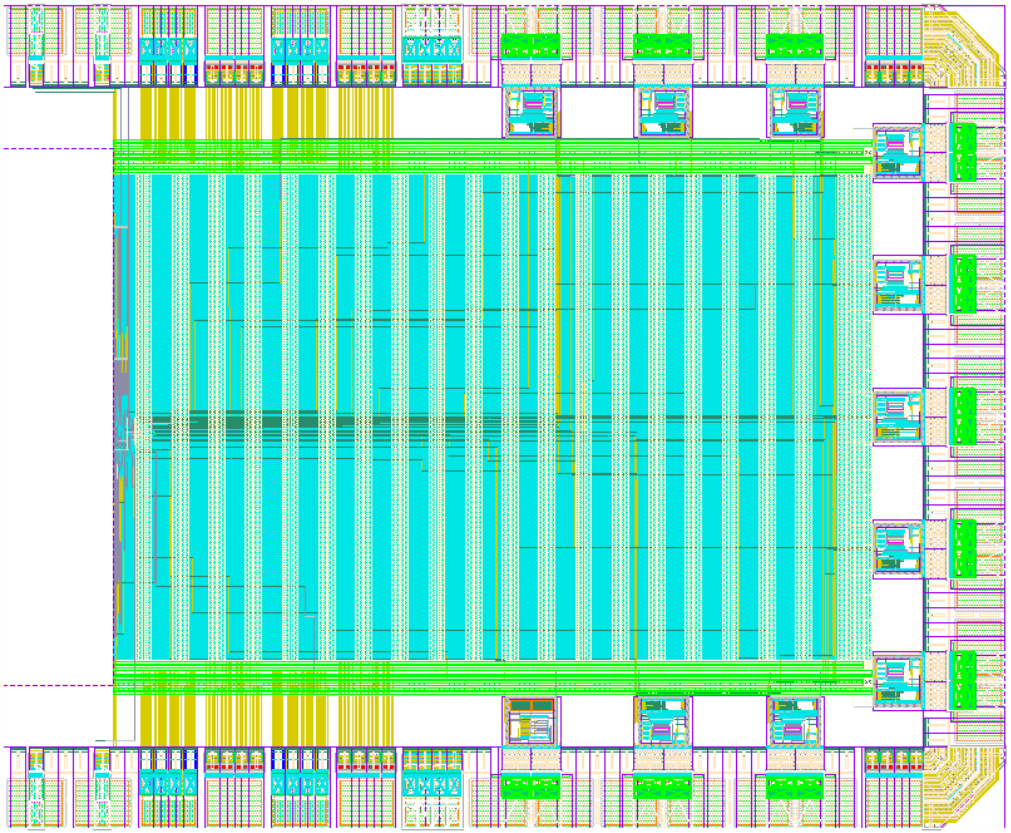
- Layout ready, extracted, post-layout simulations done

Simulation results of 10-bit SAR ADC
Comparison to ADC prototypes in 130/65 nm

CMOS [nm]	Verification	Power @40MHz [uW]	Max fsample [MHz]	
130	Prototype ASIC	680	50	M. Firlej et al. JINST 18 P11013 (2023)
65	Prototype ASIC	440	50-60	M. Firlej et al. JINST 19 P01029 (2024)
65	Prototype ASIC	~550	80-90	M. Firlej et al. JINST 19 P01029 (2024)
28	Post-layout simulation	<150 ?	~180 ?	

- Post-layout simulations show a great improvement in power consumption and sampling frequency, compared to 130/65 nm
- How realistic the post-layout simulations are ?

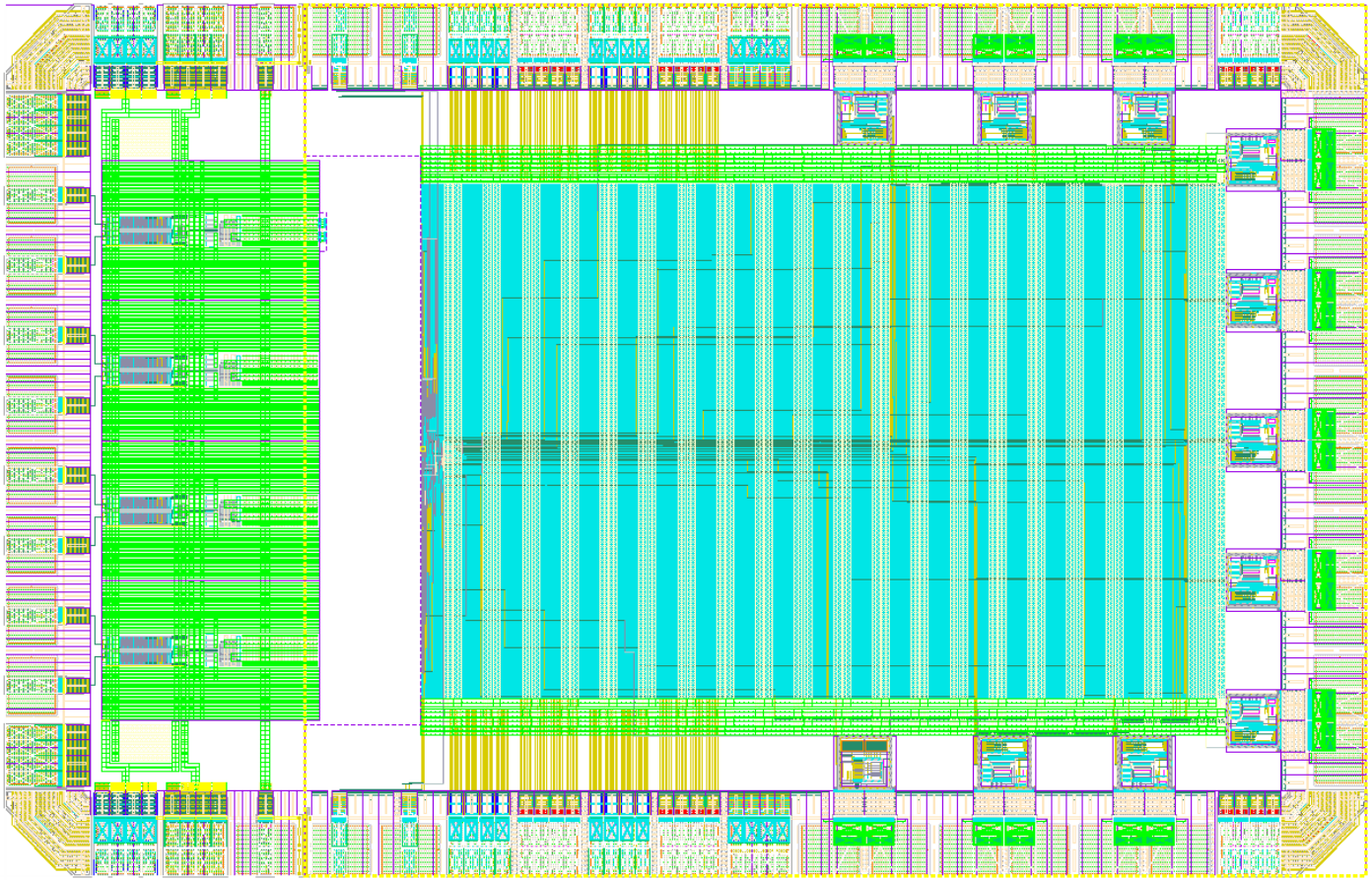
Fast ultra-low power 10-bit SAR ADC in 28nm
Status of digital part



- Supply delivered also to ADC digital circuitry via digital grid
- Data outputs in SLVS standard

- Digital part is pad-limited
- No show stoppers, but few issues to solve

Fast ultra-low power 10-bit SAR ADC in 28nm
Status of chip integration



1750um x 1120um

- Integration of 4-channel ADC ASIC in progress
- Should be ready for submission in 1-2 months